Semiconductor Wafer Test Conference (SWTest) 2024
Keynote Presentation

Known Good Die as a Key Enabler for Advanced Packaging in a Disaggregated World

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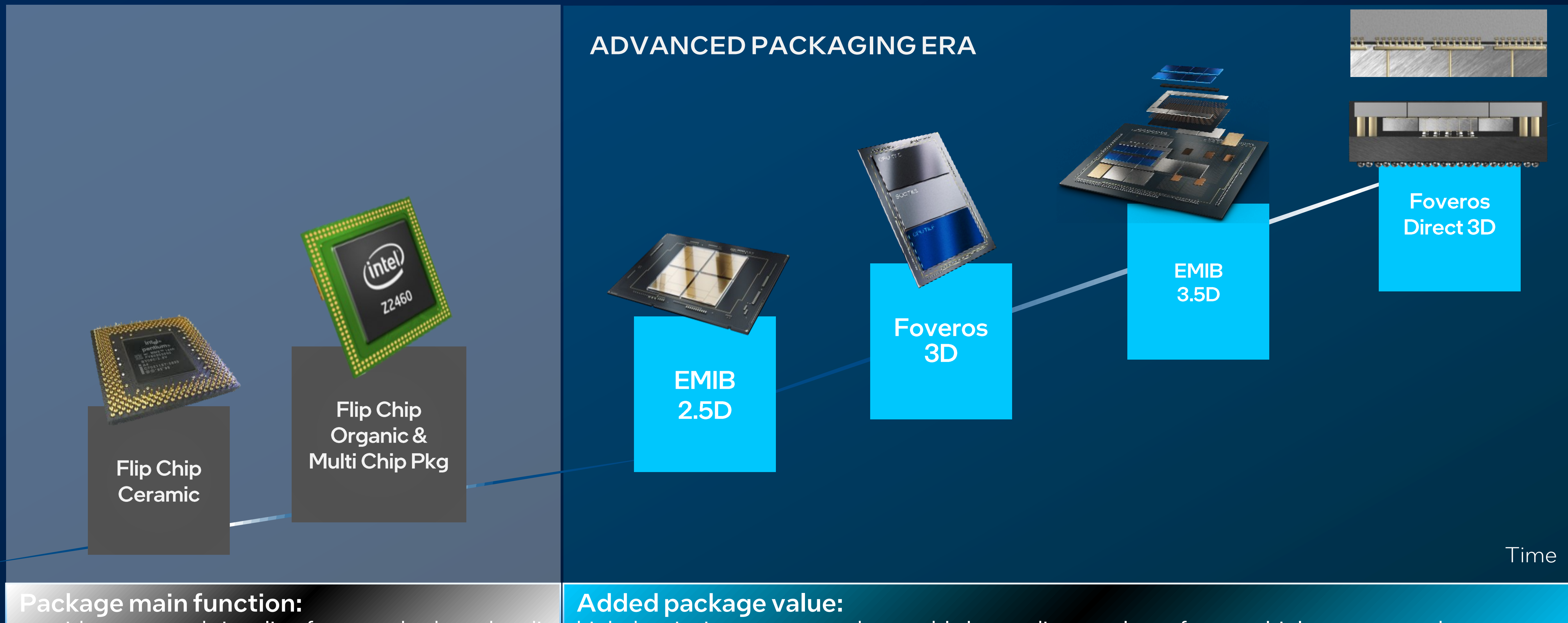
Agenda

- Advanced Packaging Trend
- Known Good Die in Disaggregated World
- Singulated Die Sort (SDx) Capability at Intel
- Summary

Intel Package Technology – Expansive Ecosystem

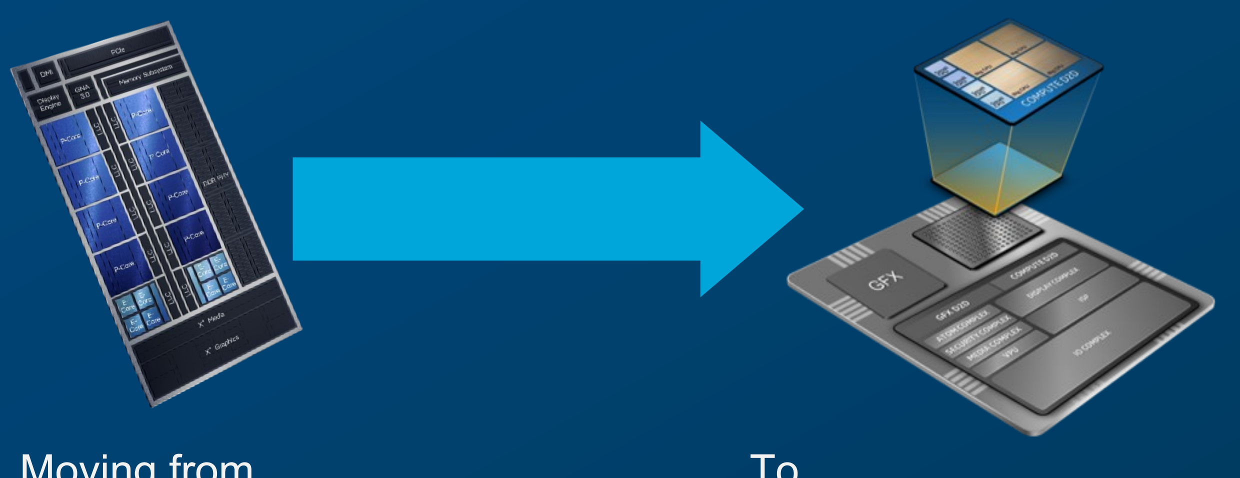


Package main function:
provide power and signaling from motherboard to die

Added package value:
high density interconnects that enable larger die complexes from multiple process nodes

Wafer Level Assembly and Advanced Packaging are an intrinsic part of most compute roadmaps

Disaggregated Flow Advantages

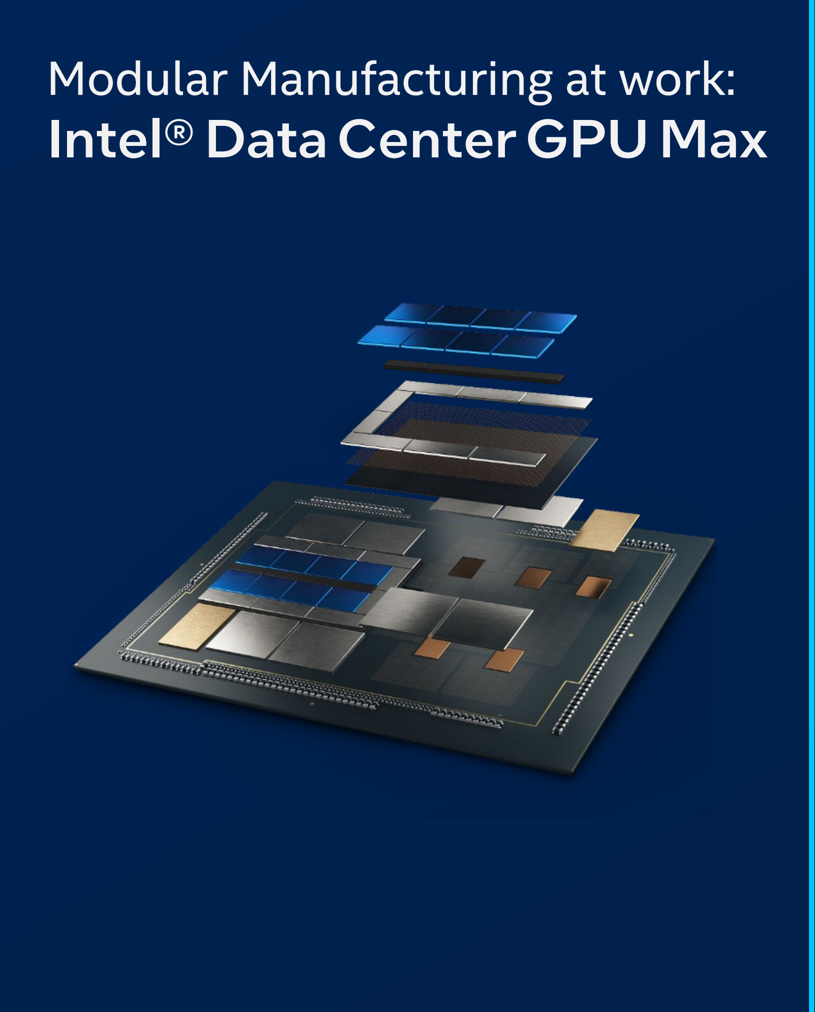


Moving from
System on Chip

To
System on Package

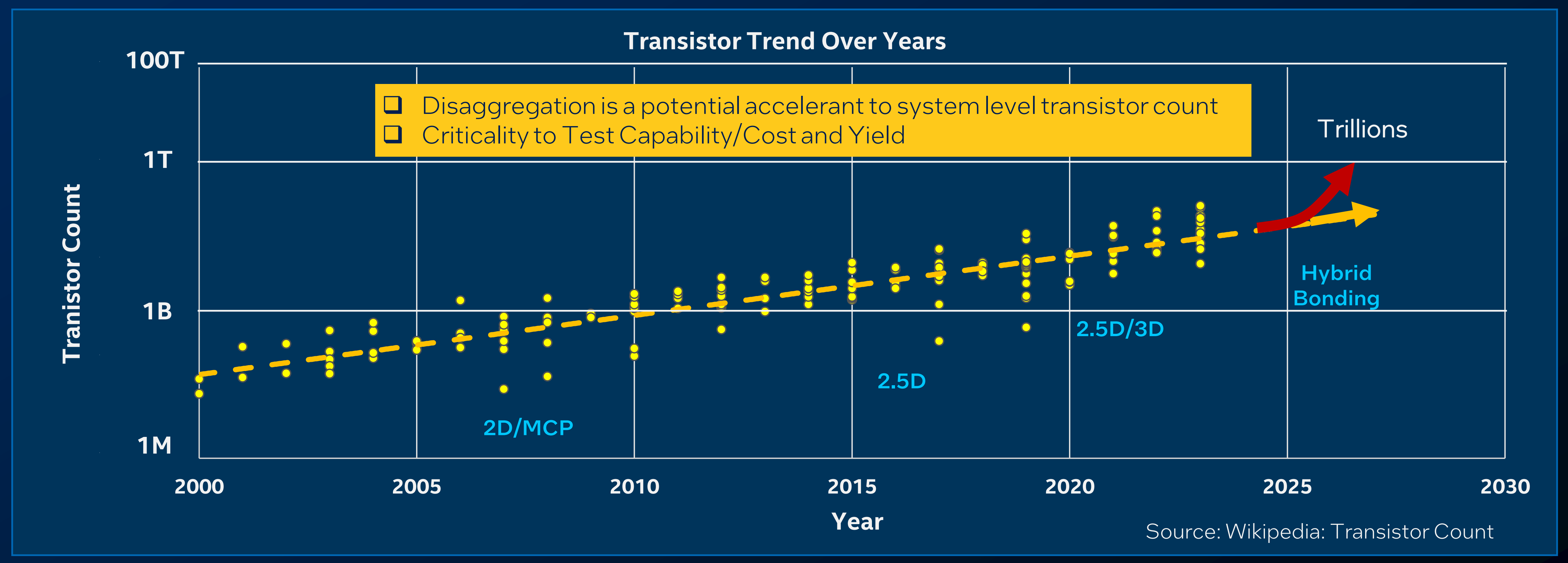
- Flexibility of packaging external and internal IP's to deliver Leadership Products
- Re-use of product design / tiles between products
- Opportunity for improved product yields
- Equivalent or Better Cost Structure vs. Monolithic

Modular Manufacturing at work:
Intel® Data Center GPU Max



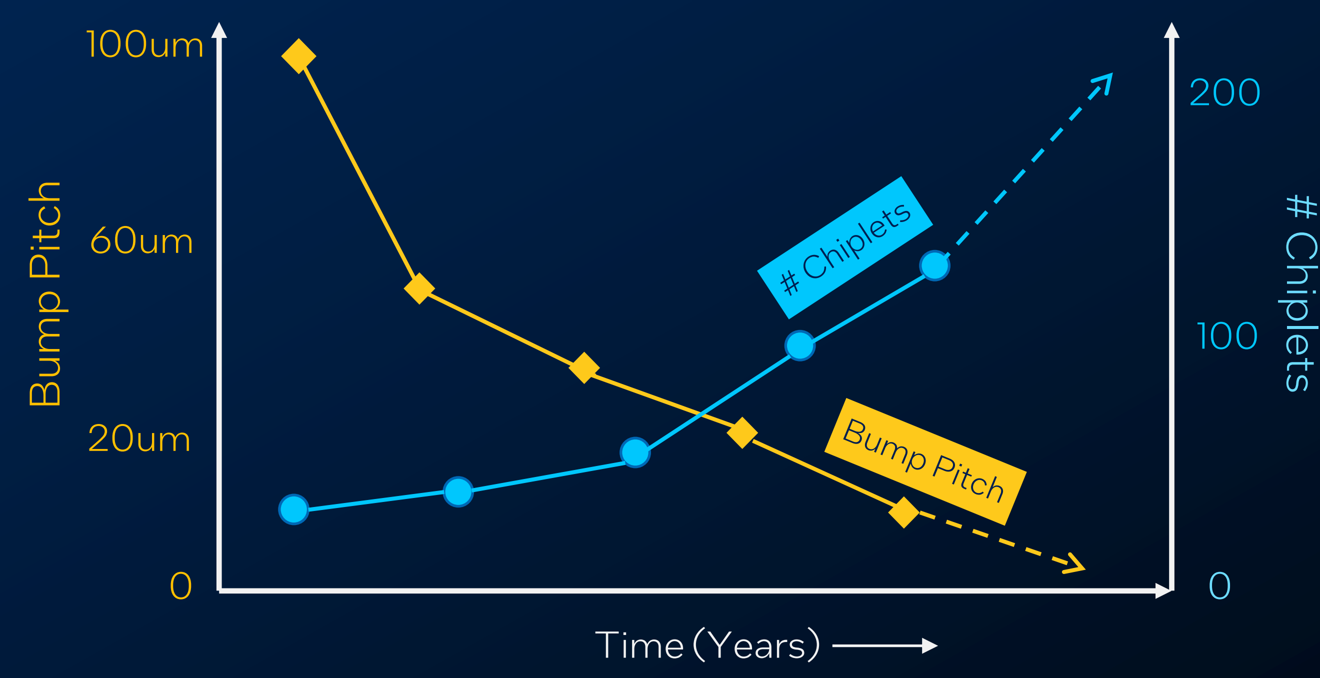
Transistor Trend: Importance of Test

Trending to hit > 1 Trillion transistors per package by middle of this decade



Challenges in Disaggregation Era

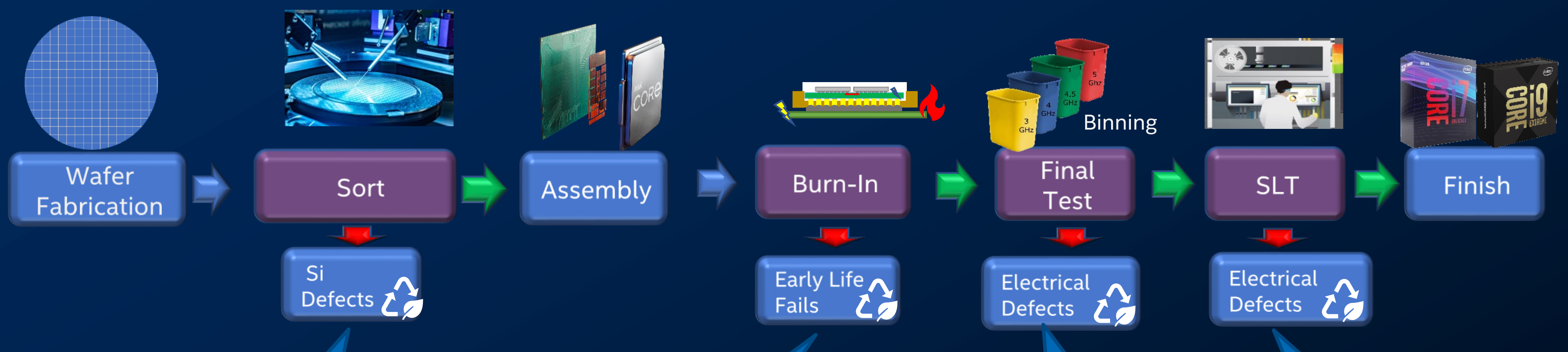
- Bump pitch continues to scale down to <10um with hybrid bonding
- Chiplet count continues to increase
- Plenty of technical challenges to be addressed in the disaggregation world
  - Chip to wafer vs wafer to wafer
  - 3D stacking, memory integration
  - Bump to bump connection: warpage/accuracy
  - Chiplet placement & stacking speed
  - Testing for interconnect quality/reliability



What are the possibilities and the challenges as we look into the future?

Role and Importance of Test in the Advanced Packaging Era

Typical Test Flow



Sort designed to screen majority of silicon defects prior to package

Burn-in designed to accelerate latent defects (voltage/temperature)

Final test screens fully-packaged units at use conditions (high temp, at use speed)

System level test (SLT) screens units for DPM-level defects using configurations similar to customer

Role of Test in Disaggregated World

Easy Example: Single die into a package

Sort

Yield

Assembly

Burn In

Top Die

Substrate

Final Test

Top Die

Substrate

System Level Test

Top Die

Substrate

Any ***missed*** screening at sort directly impacts U/D

Yield
Cost risk

Yield ~ HIGH

Assbly/Pkg $ lost

Role of Test in Disaggregated World

2 Die into a package (classic MCP)

Sort

Yield

Yield

Assembly

Burn In

Final Test

System Level Test

Top Die

Substrate

Top Die

Substrate

Top Die

Substrate

Now, ***each*** die contributes to missed screening

Yield
Cost risk

Yield ~ GOOD

For each mis-screened die:
1 good die lost

- **more wafer for each die**
- **Still lose Pkg**

Role of Test in Disaggregated World

What about Four Die ?

Sort

Yield

Yield

Yield

Yield

Assembly

content

Burn In

Top Die

Substrate

Final Test

Top Die

Substrate

System Level Test

Top Die

Substrate

Only way to solve this is to bring stress and full class content to sort. So-called, **Known Good Die.**

Yield
Cost risk

Yield ~ OUCH!

For each mis-screened die:
3 good die lost

- **more wafer for each die**
- **Still lose Pkg**

Beyond classic industry KGD moniker

- “Known Good Die” is testing/screening die prior to assembly & packaging, for all defects and parametric issues in silicon

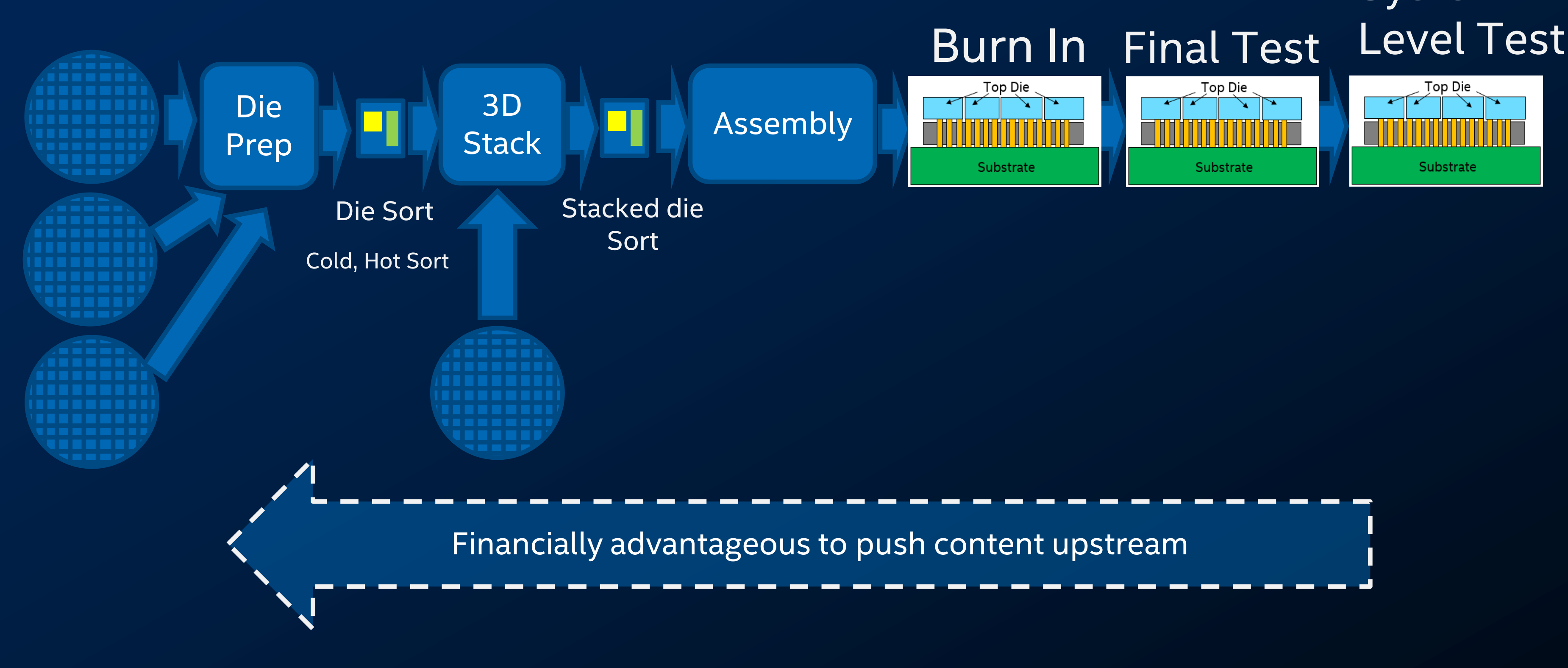
- KGD is the result of die-level testing under the following conditions
  - Total emulation of the final test done on packaged chip, by bringing it at the die-level
  - High Thermal stress to catch latent defects
  - High Electrical stress (high voltage, frequency) to screen defective die

KGD = Passing Die under stress from all the test conditions

Intel's Unique Test Method in Disaggregated World

<u>Disaggregated Flow</u>:

Multiple die (top & base) stacking & integration into package

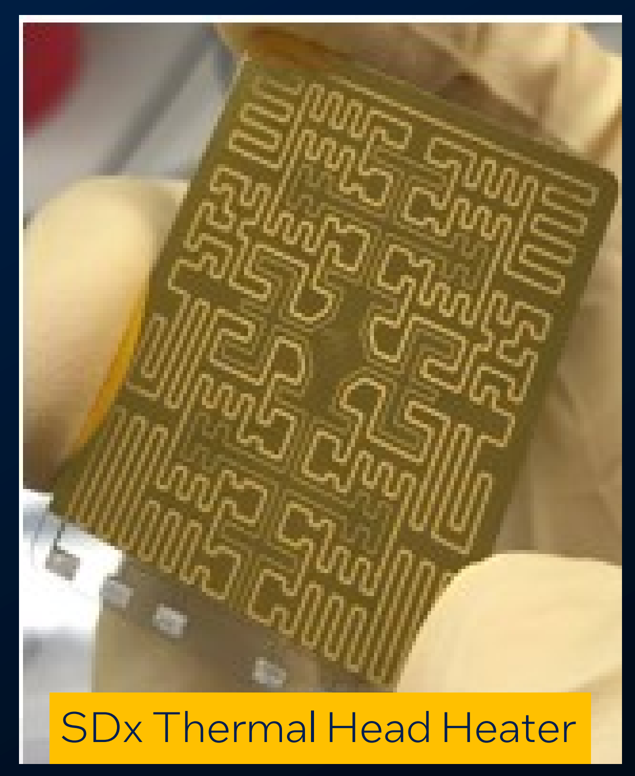


Enabling Known Good Die requires a combination of tester platform and thermal control

Intel Solution to enable KGD: Singulated Die Sort

- Singulated Die Sort/Test (SDx) <u>ensures only known-good die</u> survive to wafer level assembly processing

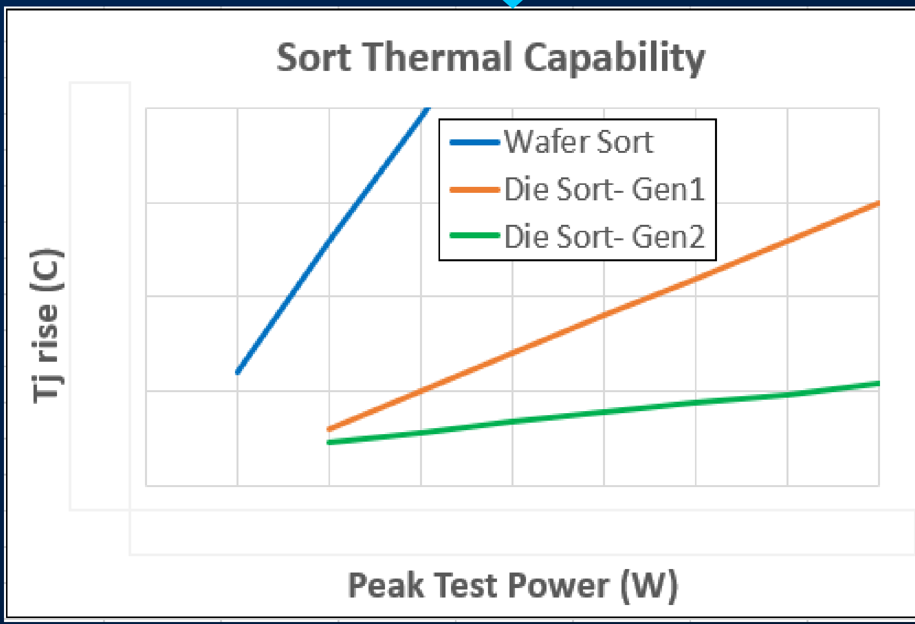
- What is SDx?
  - At its core, SDx is a novel thermal system which provides extreme thermal conductivity and response
  - Incorporates special die handling capability
  - SDx allows full final test (post-package) content and stress test at Sort (pre-package)
  - Based on Intel developed HDMT tester (High Density Modular Tester)

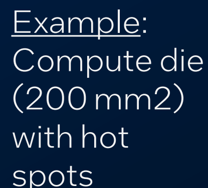

SDx Thermal Head Heater

Die Sort: Intel Thermal Solution

Best-in-class thermal capability

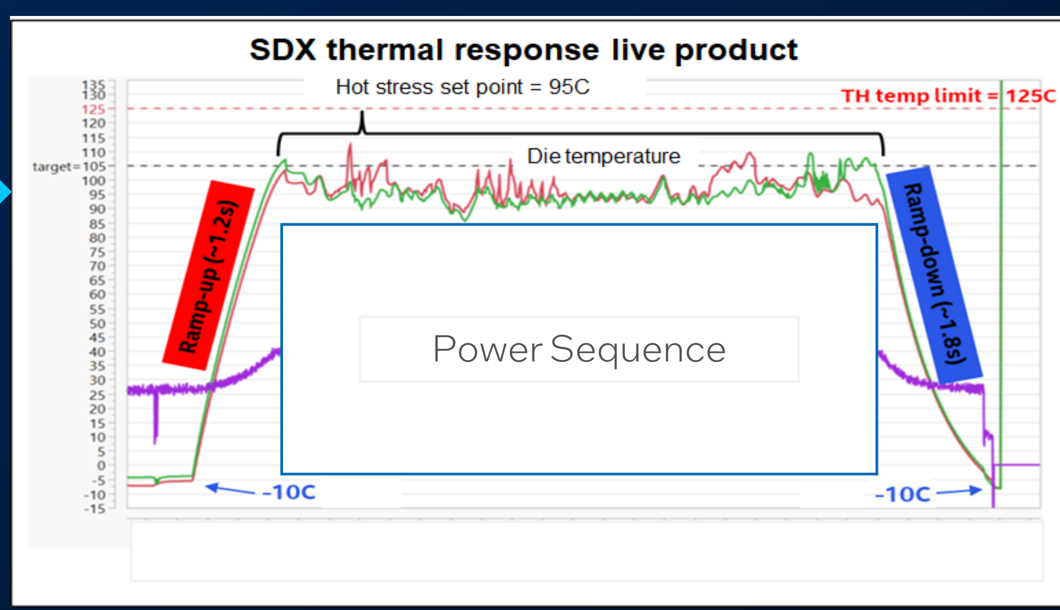
- 125C temp swing (cold to hot) in 1-2 secs
- >100x more effective thermal capability than wafer sort-based industry solutions





Tj rise = Actual Temp – Set point

Example: Compute die (200 mm2) with hot spots



SDx enables final test content & stress at Sort

- Captures up to 90% of back-end defects, thus providing higher test yield
- Tests both singulated die and singulated stacked die
- Cold & hot testing merged into a single insertion

HDMT: Intel Tester Solution

- High Density Module Tester is another key component of Intel Sort/Test
  - Intel designed and manufactured test platform

Key Advantages/Points:

- Highly re-usable, re-configurable and field upgradable
- Competitive cost-of-test for HVM and Engineering use
- Small footprint: Optimized Modular Architecture
- Integrated Infrastructure

- Modular Design allows multiple generations of capability, with multiple tester configurations tailored to product needs
- Proven tester platform with 12000+ testers running in factories & supporting products
  - 1400+ unique test programs; **2000+ users** worldwide

HDMT Capability Overview

- Key Hardware Capability

Parameter	Capability
# Digital IO Channels	896 @1.5 Gpbs up to 2240 @ 2 Gpbs
# HC/LC DPS Channels	308 total independent resources (HC: 70, LC: 238) up to 484 total independent resources (HC: 110, LC: 374)
Vector Memory (per pin pattern depth)	4GV with 8x channel linking up to 4GV with bottomless
Simultaneous power to DUT (W)	1.3 kW up to 4.3 kW

- Key Software Capability
  - Highly configurable to allow features per customer's needs
  - Highly efficient & easy to use Multi-DUT and IP level parallelism
  - Dynamic ganging of DPS rails within test flow
  - Excellent Power/Thermal control & monitoring

HDMT is a highly capable tester platform that meets all the product requirements

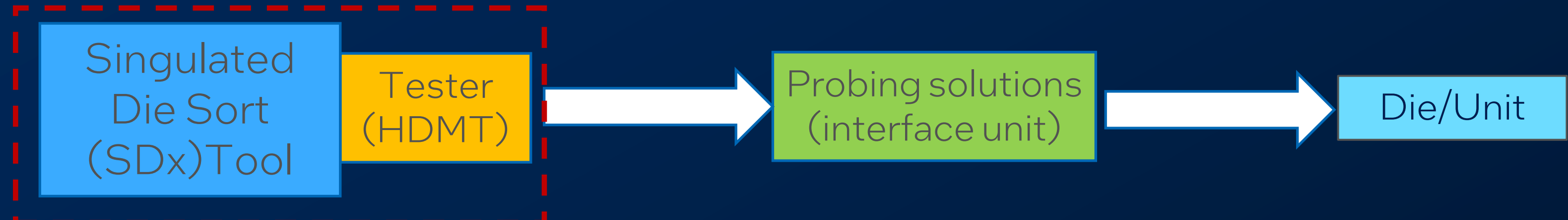
Intel's Sort Portfolio

HDMT based singulated die sort capability

Singulated Die Sort Tools on Sort Floor

Disaggregated Test– Equipment & Tester Capability

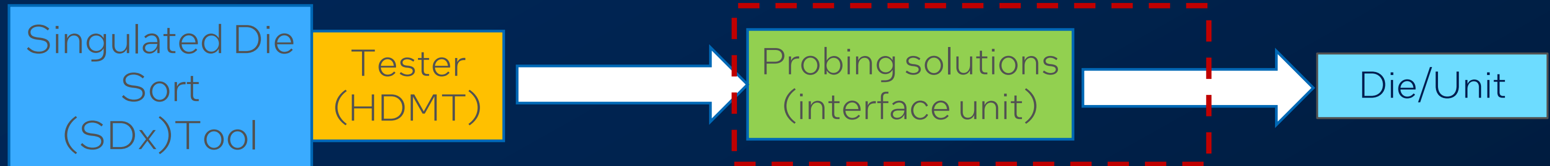
- Power requirements are trending up for new products, driving the need to deliver higher power during testing of the part



- We must send the needed power and electrical stress for testing new products
  - Dynamic Voltage Stress (DVS)
  - Voltage Margin Tests
  - Time based power sequence
- Active thermal control (beyond thermal head) for test temperature is a key requirement
  - Controlled loop for heating and cooling due to thermal control algorithm
  - Temperature streaming and multi-modal temperature monitoring using RTD, analog thermal diode and DTS

Disaggregated Test - Probing Capability

- Power delivery to unit is critical. Small chiplets will have limitations in number of bumps and PDN



- Probing solution cannot compromise assembled stack power delivery

Monolithic Era | Chiplet Era

Sort Probing	Overview	Sort Probing Solutions			
Standard (Monolithic)	Mixed bump (large + micro bump)	Industry Solution (dedicated test pads)	Intel Solution (micro-bump cluster probing)	Finer pitch micro- bump	Hybrid Bonding
100 um 70 um	Large bump u-bump		Quad probing Single probing *Patent pending (Quad probe)*	??	?? Innovation needed
>100um pitch	Smaller pitches (<100um) for chiplets	<100um (bump pitch), >150um probe pitch	36um to 25um	25um to 10um	< 10um
Best Sort Power Delivery (100% bump probing)	Innovative probing solutions needed to sort the different chiplets. Mixed pitch. Multiple probe types	Lower Sort Power Delivery (10% to 20% sort dedicated area)	Best Sort Power Delivery (100% bump probing); Max package Power Delivery (max bump packing density)	Native pitch scaling vs RDL?	Inductive Power coupling, no contact solution, others?

Beyond Wafer/Die Testing

- Intel's HDMT based overall Test Portfolio includes backend test capabilities, that go together with innovative Die Sort capabilities
  - All these test solutions meet the critical needs of disaggregated AI/HPC products

Sort

- Die level sort enables full final test content with active thermal control
- Reduces fallout at final test, significantly improving BE yield

Burn-In

- High-volume high-power burn-in capability
- Active thermal control enables lower STRESS time

Final Test

- Final Test with advanced thermal control capabilities
- Parallelism opportunities for additional cost savings

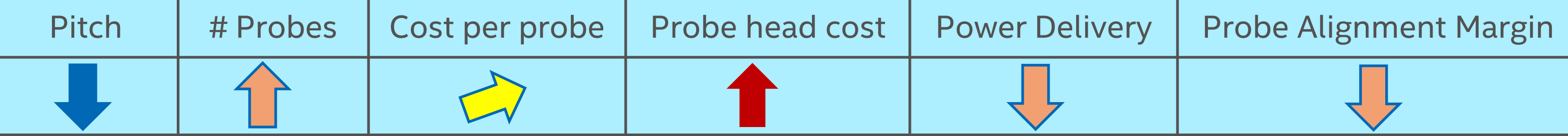
System Test

- Direct implementation of validation boards and testing for HVM screening
- True SLT in high volume for screening DPM level defects in system environment

- Intel's rigorous test methods ensure high quality and reliability of the final part
  - Testing for known good individual chiplets, stacked chiplets and final packaged units

Test Innovation and Cost

- Continuous innovation is needed to meet requirements for sorting next generation chiplets
  - Hybrid Bonding bump scaling into single digits and beyond will continue, requiring innovative probe solutions
  - Co-packed optics testing is an emerging area → will need some revolutionary ideas for concurrent functional electrical and optical testing
- Test cost will continue to be a major focus
  - Tester power density improvement will be needed to minimize additional capital purchase
  - Tester and handler parallelism enhancements for multi-unit (site) testing
  - Pitch scaling will continue to put pressure on developing cost-effective probe solutions



Pitch	# Probes	Cost per probe	Probe head cost	Power Delivery	Probe Alignment Margin
↓	↑	↗	↑	↓	↓

  - Improve test coverage and test time optimization using features such as DFT, BIST
- Right balance between cost of process complexity vs test cost is important
  - Application of redistribution layer (RDL) vs continuous pitch scaling
  - Singulated die testing with reconstitution vs wafer level testing

Summary

- Advanced Packaging Era and the Disaggregated Flow is here to stay in the semiconductor industry
- It is critical to identify Known Good Die (KGD) and catch all defects prior to assembly in advanced packaging
- Intel's unique Test solutions based on HDMT platform and die-level test capability with SDx equipment, ensure KGD
- Intel's HDMT (tester) is available for use by IFS (Intel Foundry) Test Services customers with support from emerging ecosystem
- Cost-effective test innovations are essential to meet emerging product needs

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