

2020 SW Test Untethered Conference

Moore's Law and the Future of Test

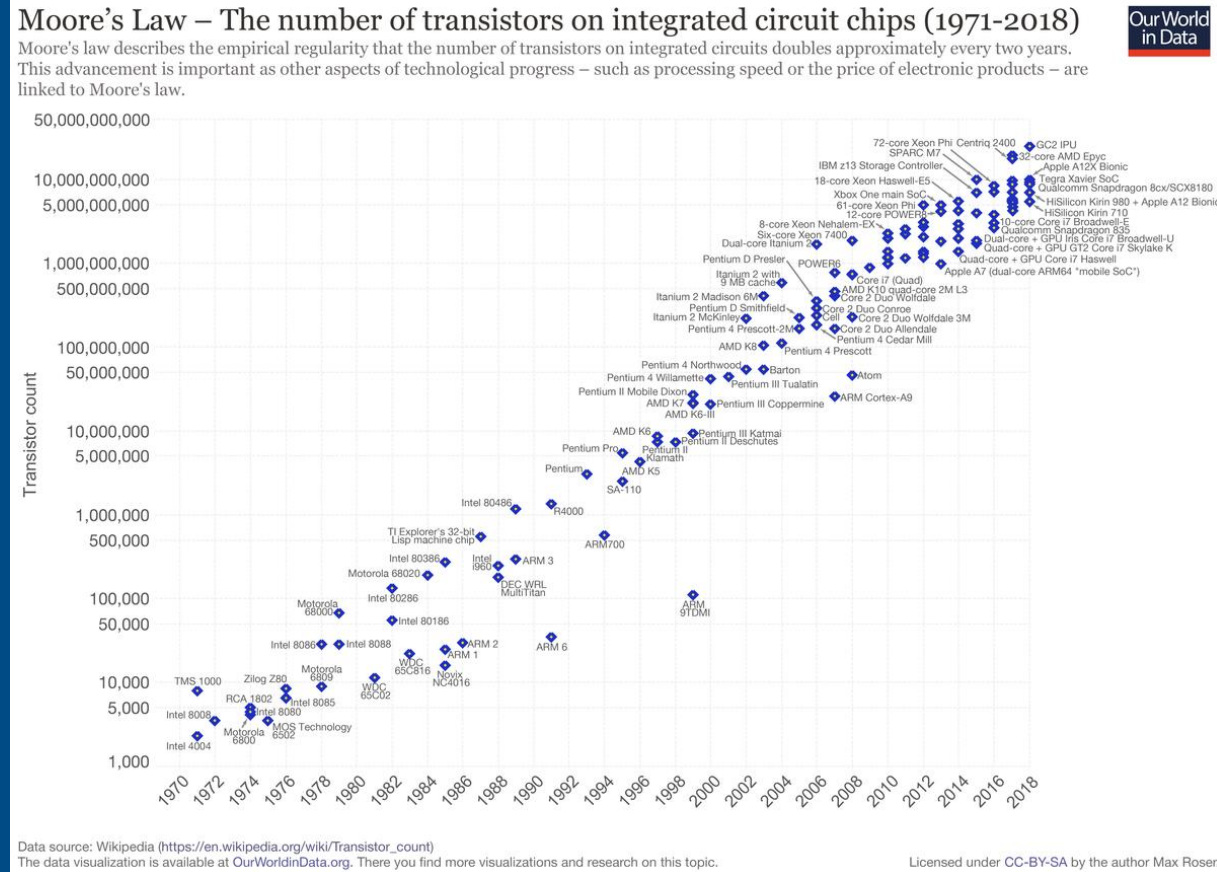
Pooya Tadayon, Intel Fellow

Assembly Test Technology Development

Director, Test Probe Technology

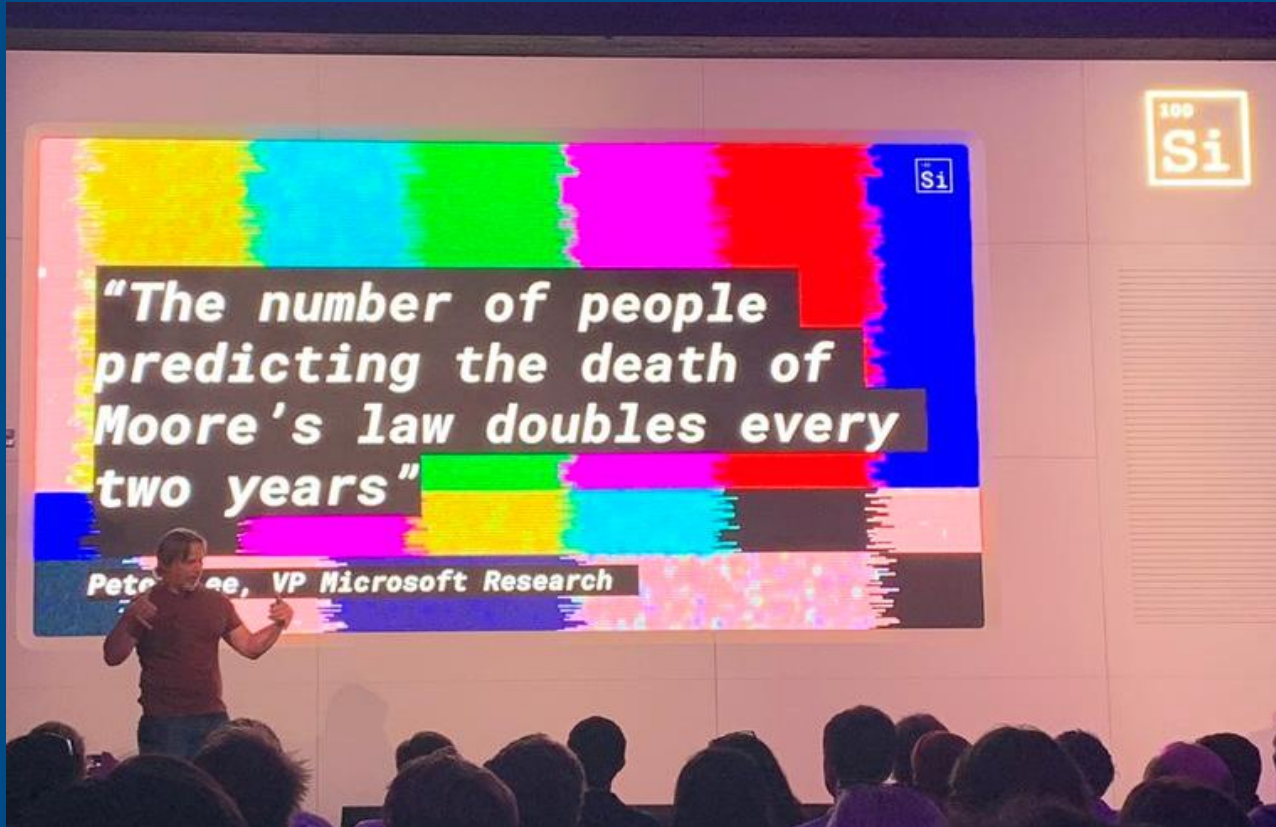


Moore's Law



Moore's Law has been the growth engine for the semiconductor industry

Moore's Law



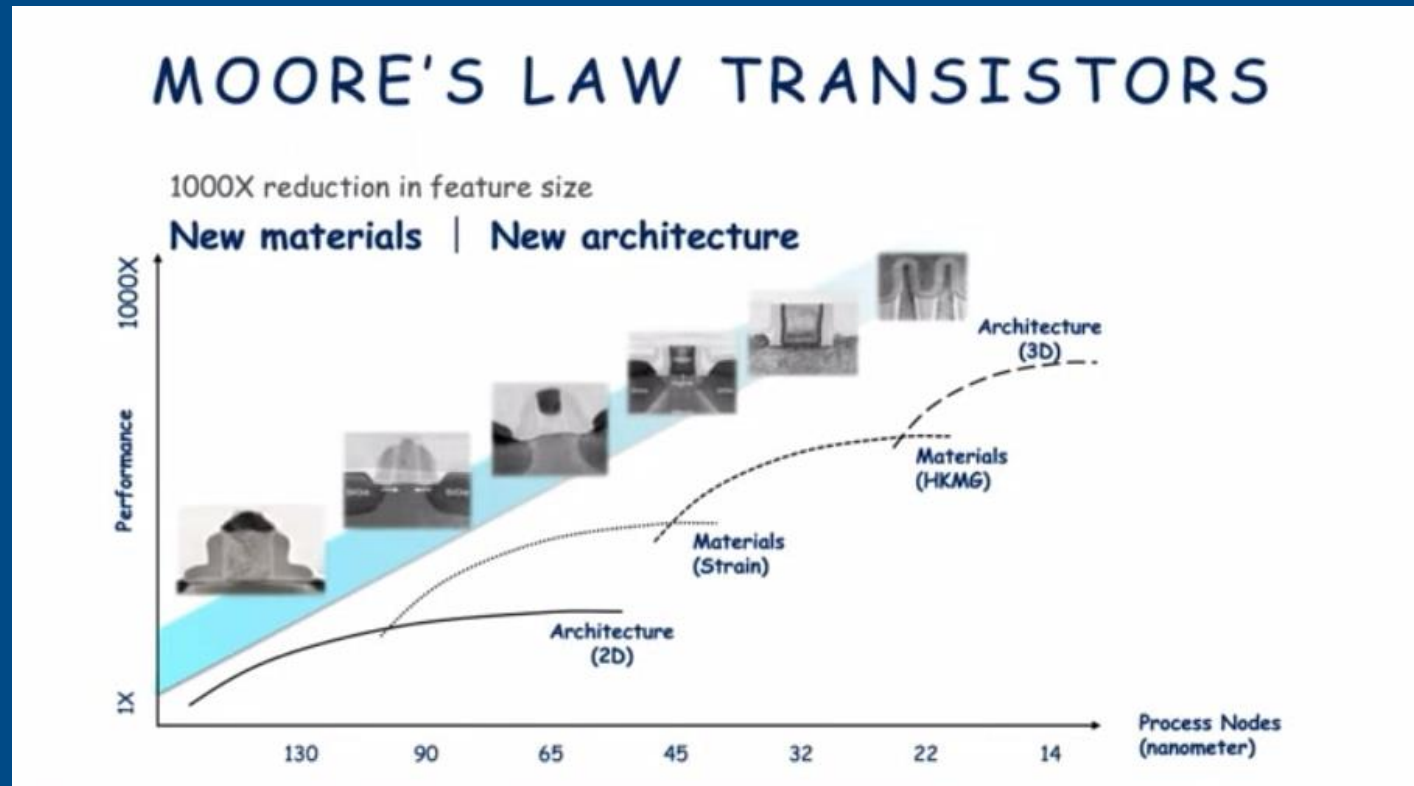
*"Moore's Law is not dead..." –Jim Keller, Sr. VP Si Engineering Group
2019 Silicon 100 Summit*

"The reports of my death are greatly exaggerated."

-Mark Twain

Moore's Law will continue to fuel the industry

Moore's Law



<https://www.nextbigfuture.com/2020/04/jim-keller-reviews-moores-law-computing-and-considers-ai-chips.html>

Innovation in materials and architecture has kept – and will continue to keep – Moore's Law alive

Future of Moore's Law: *die disaggregation and heterogeneous integration*

Moore's Law, 40 years and Counting Future Directions of Silicon and Packaging

Bill Holt
General Manager
Technology and Manufacturing Group
Intel Corporation

InterPACK '05
2005 Heat Transfer Conference

Key Messages

- **Systems/platform** focus drives increased **requirements** for silicon and packaging
- Making the right **choice between on-chip and in/on package** integration is critical to cost effective solutions
- Moore's Law is the engine for continued growth
- Silicon is ideal for **homogenous** integration
- Packaging is ideal for **heterogeneous** integration

Momentum Builds for Advanced Packaging

"Increasing density in more dimensions with faster time to market."

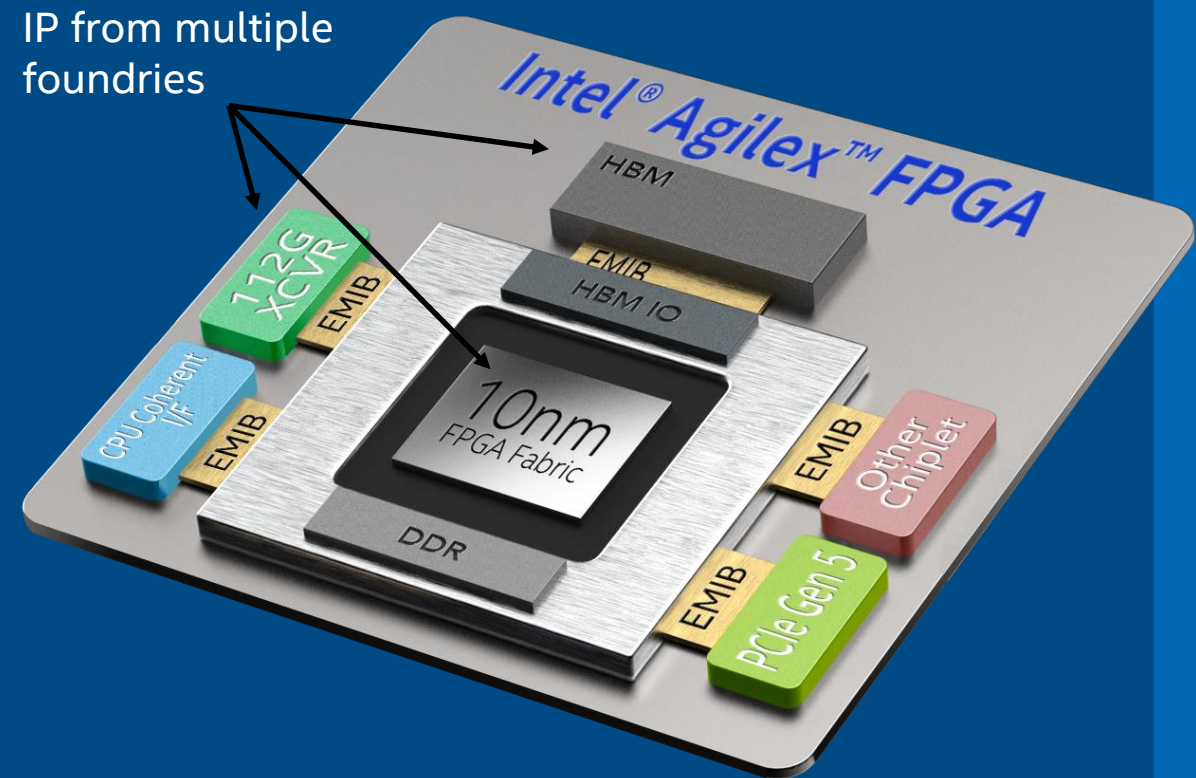
Sept. 2020

<https://semiengineering.com/momentum-builds-for-advanced-packaging/>

The need for, and availability of, advanced packaging is finally here

Future of Moore's Law: *die disaggregation and heterogeneous integration*

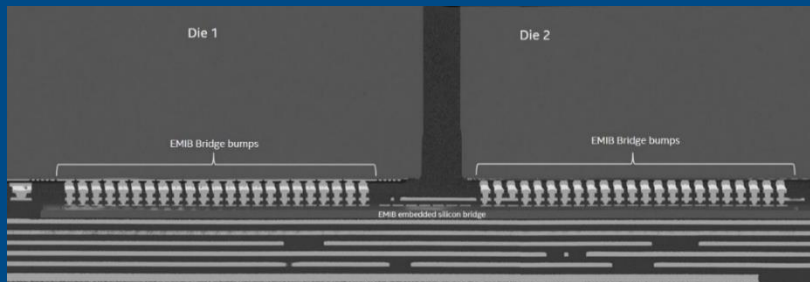
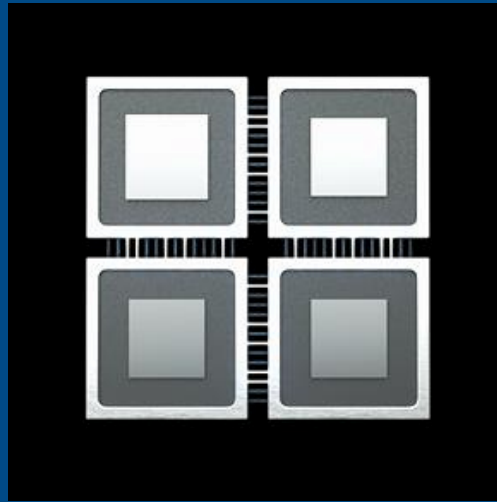
- Stitch IP from multiple nodes & foundries
- Build yield resiliency
- Enable silicon area >> reticle size



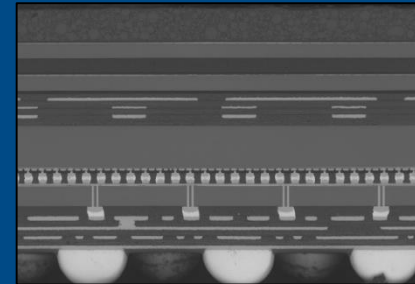
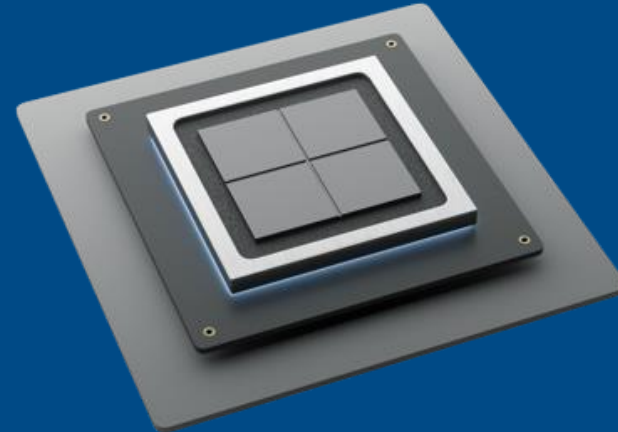
Industry will rely more on advanced packaging to extend Moore's Law

Advanced Packaging Options

EMIB

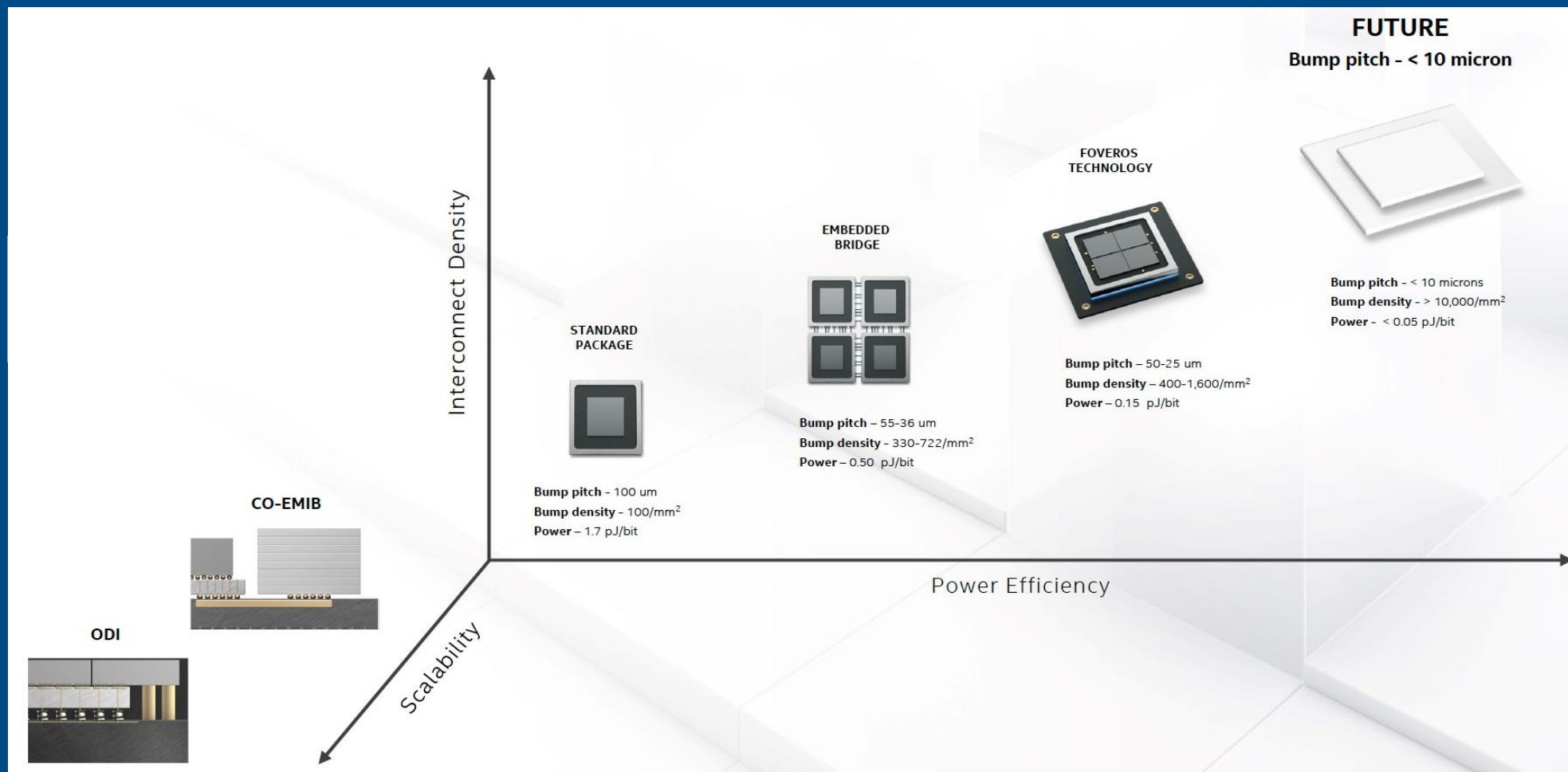


FOVEROS



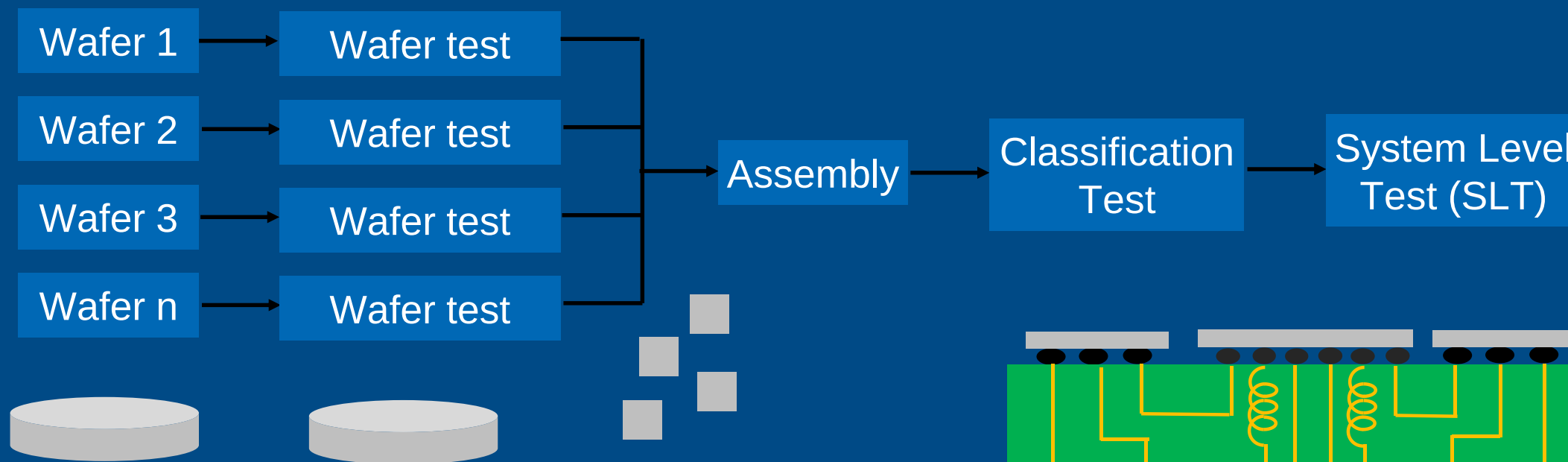
Multiple advanced packaging solutions exist for different applications...

Advanced Packaging Options



...with many additional concepts at various stages of maturity

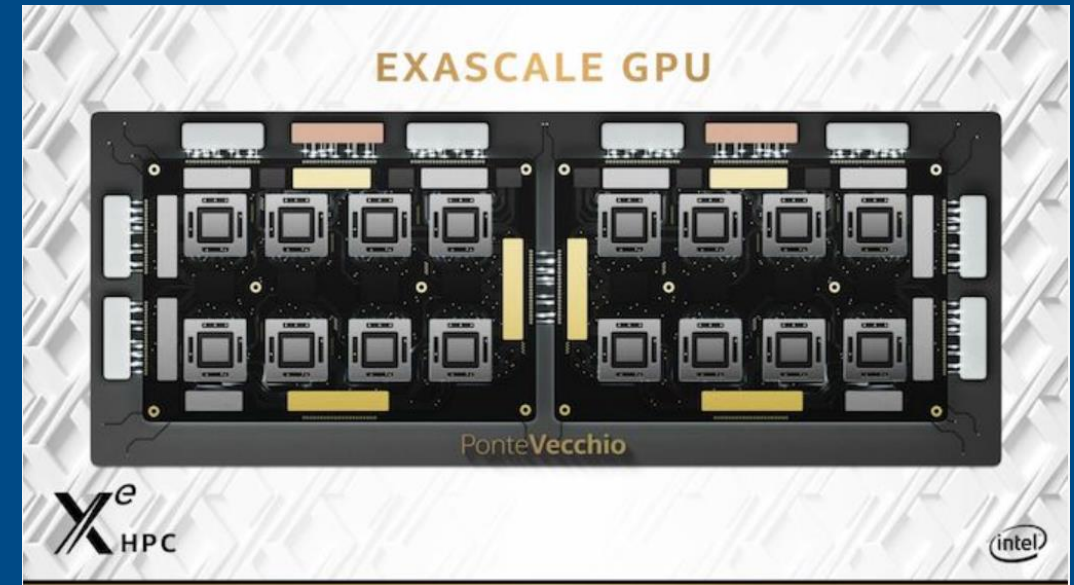
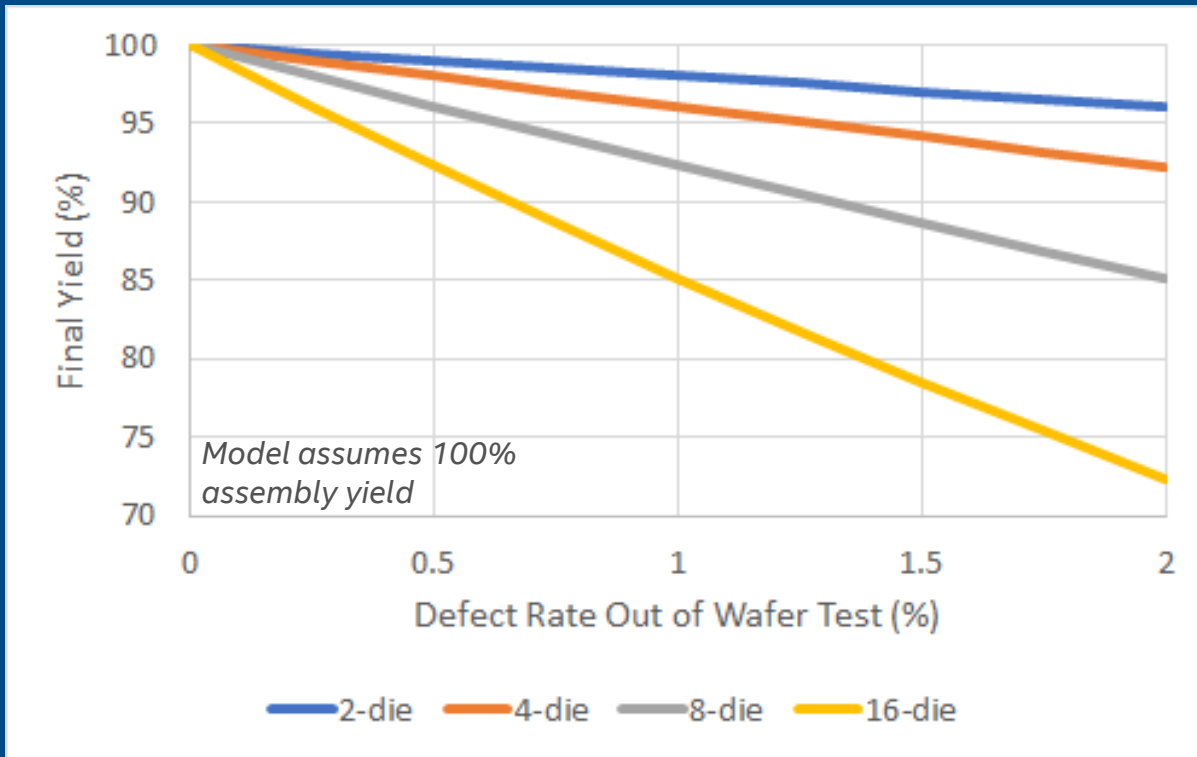
Impact to Test



Typical 2D/2.5D manufacturing flow

Characterized Know-Good-Die (cKGD) out of wafer test is critical to making disaggregation and heterogeneous integration successful

Impact to Test



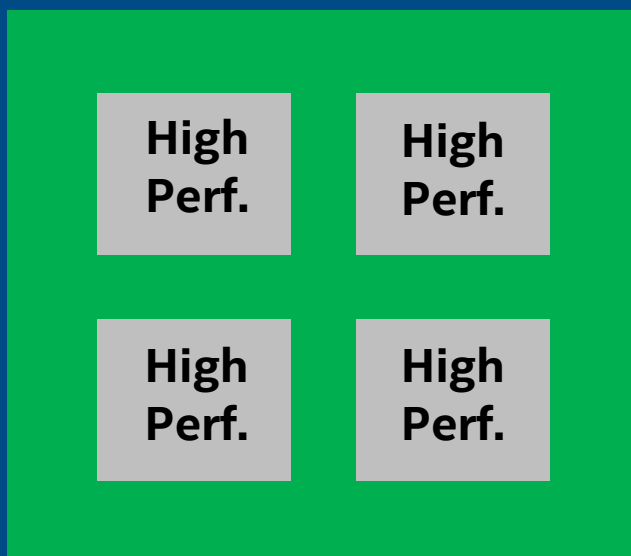
<https://www.anandtech.com/show/15188/analyzing-intels-discrete-xe-hpc-graphics-disclosure-ponte-vecchio/3>

"On the high-end in the data center, Ponte Vecchio consists of a unique chiplet architecture with sixteen compute chiplets in total.

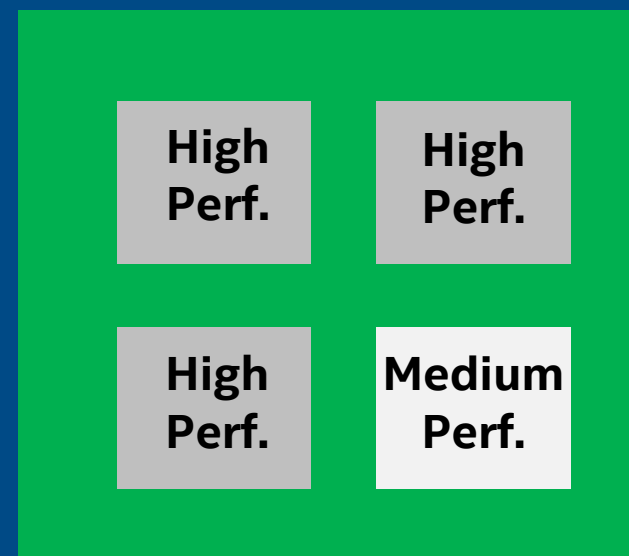
<https://seekingalpha.com/article/4321159-nvidia-faces-huge-threat-from-intels-chiplet-gpu-approach>

KGD has historically been associated with yield, and the goal of minimizing number of defects escaping wafer test

Impact to Test



Shipped as
High Performance



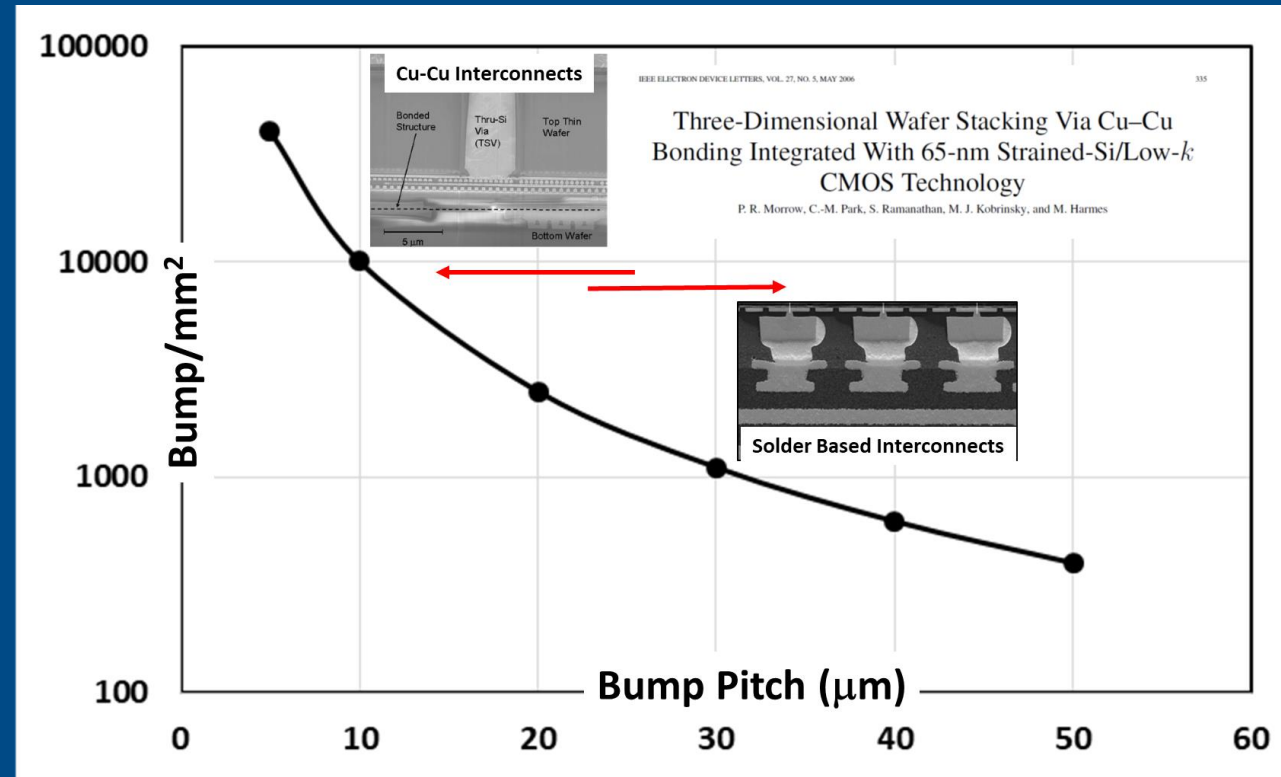
Shipped as
Medium Performance

In addition to yield, die disaggregation demands an accurate prediction of device performance in the final package & system environment (i.e. cKGD)

Impact to Test:

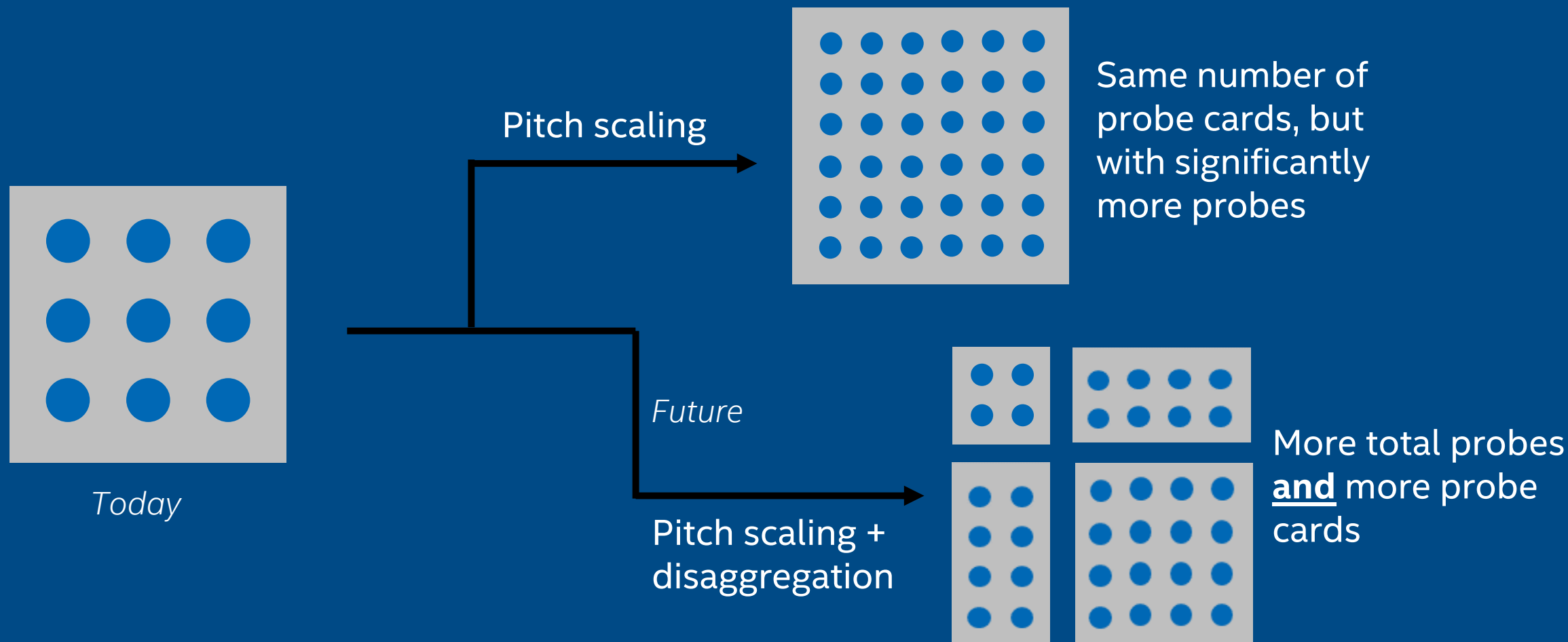
economic & technical challenges to producing cKGD

Advanced Packaging Drives Pitch Scaling



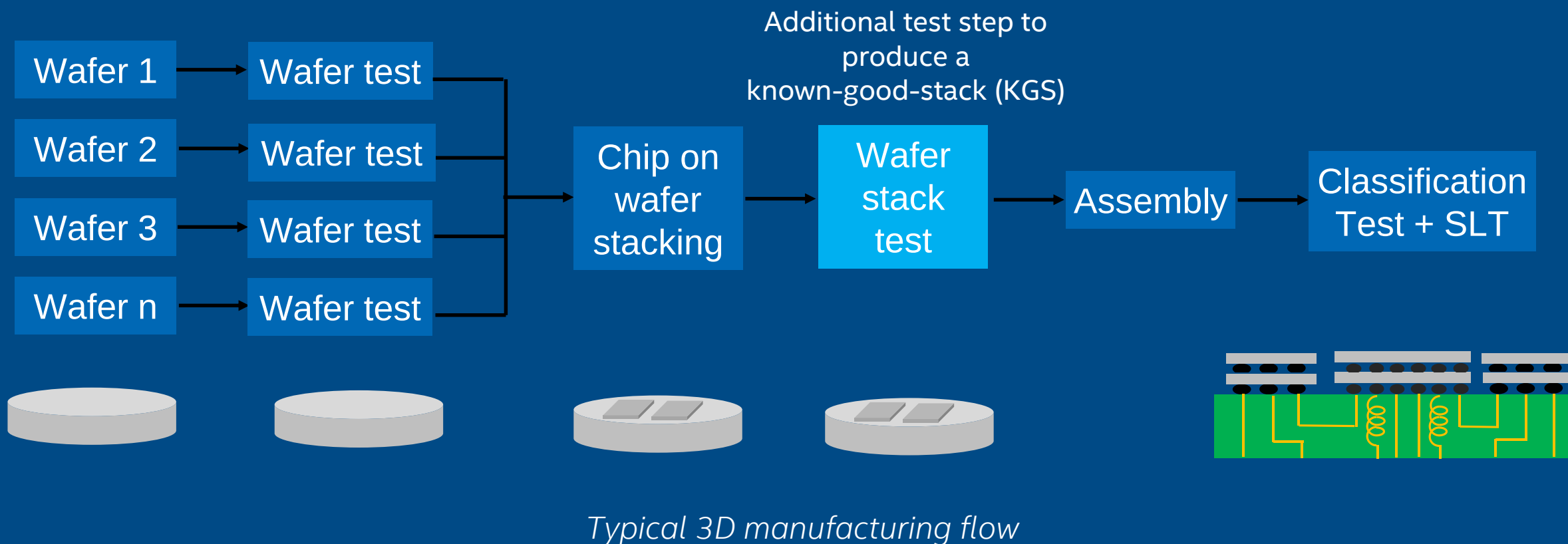
Insatiable appetite for die-to-die interconnect density is driving very aggressive pitch scaling roadmap towards 3D architectures

Impact to Test Industry: *Probe Cards*



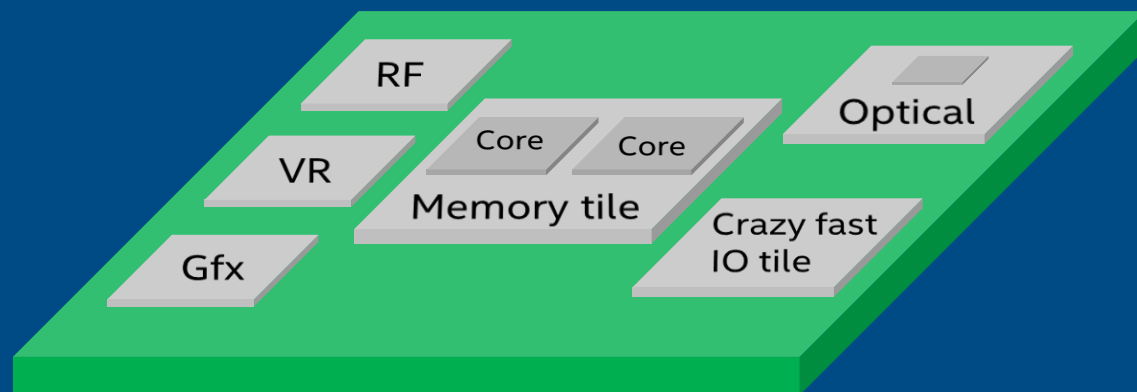
Test cost cannot scale with number of chiplets; probe industry will need to scale to support more probes and probe cards at a lower cost

Impact to Test Industry: ATE



3D architectures drive additional test steps; ATE industry will need to enable faster, lower cost systems to keep cost at parity

Impact to Test Industry: ATE



Test strategy?

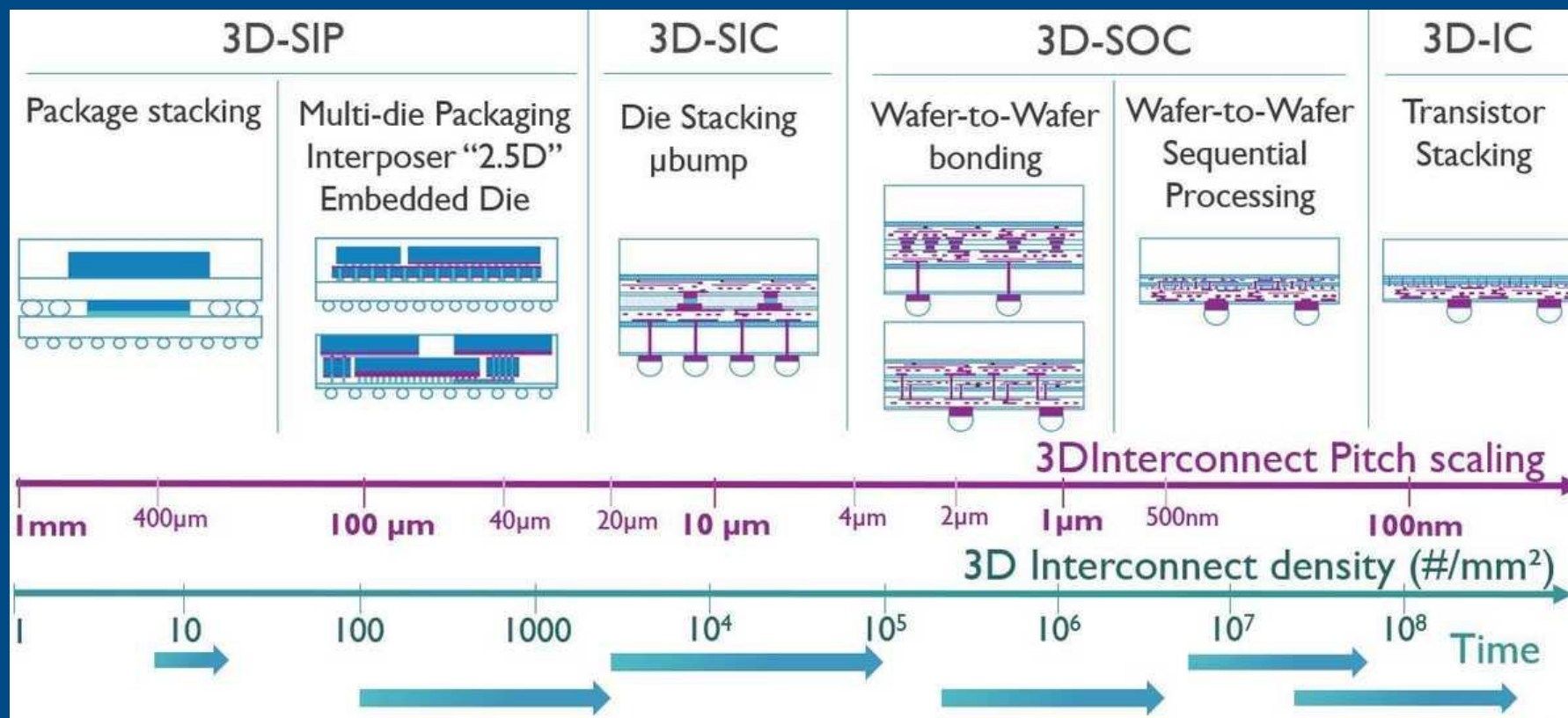
Multiple sockets on specialized ATE to test each IP separately

Single socket on a big iron ATE that can test everything

Higher reliance on system level test; SLT capable ATE?

As devices begin to resemble a system, new strategies and solutions are needed to test these products in a cost-effective manner

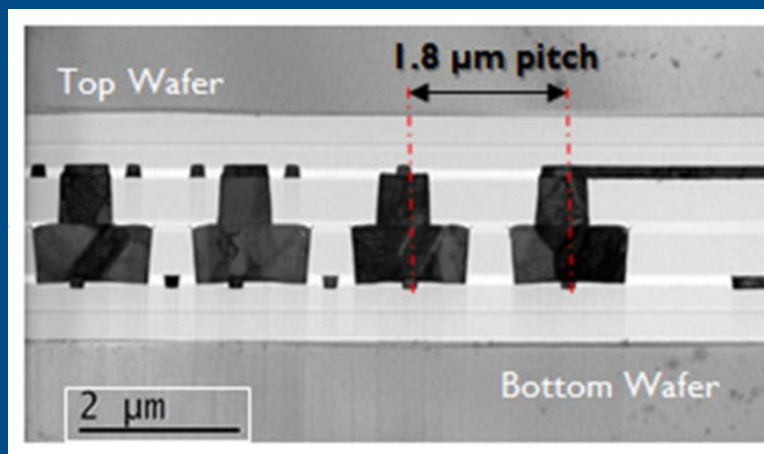
Pitch Scaling Roadmap



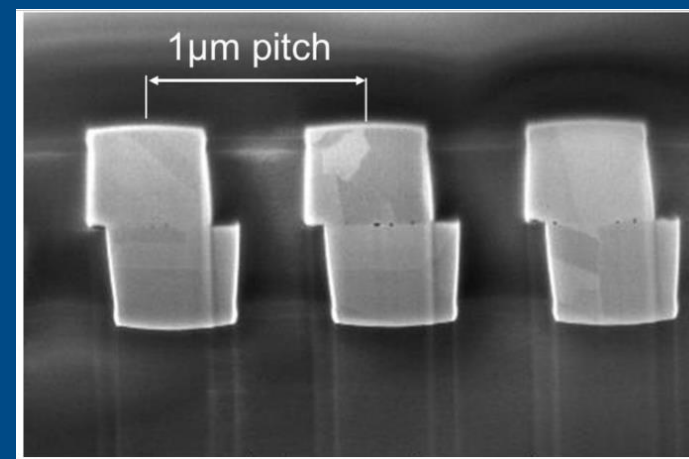
<https://www.imec-int.com/en/imec-magazine/imec-magazine-july-2019/a-3d-technology-toolbox-in-support-of-system-technology-co-optimization>

Die-to-die interconnect pitches are forecasted to go below 1 µm

Pitch Scaling Roadmap



Source: IMEC



Source: LETI

TSMC Teases 12-High 3D Stacked Silicon: SoIC Goes Extreme

"In the case of SoIC, the hybrid-bonding pitch is on the scale of 9 μm for N7/N6 chips and 6 μm for N5 chips."

<https://www.anandtech.com/show/16026/tsmc-teases-12-high-3d-stacked-silicon>

Industry is moving aggressively at enabling this roadmap;
is native pitch probing at these dimensions realistic?

Pitch Scaling, Hybrid Bonding, and Test

Towards a complete direct Hybrid Bonding D2W integration flow: Known-good-dies and die planarization modules development

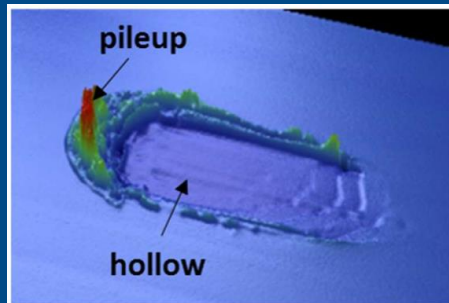
E. Bourjot, P. Stewart, C. Dubarry, E. Lagoutte, E. Rolland, N. Bresson, G. Romano, D. Scevola, V. Balan, J. Dechamp, M. Zussy, G. Mauguen, C. Castan, L. Sanchez, A. Jouve, F. Fournel, S. Cheramy

Univ. Grenoble Alpes

CEA, LETI

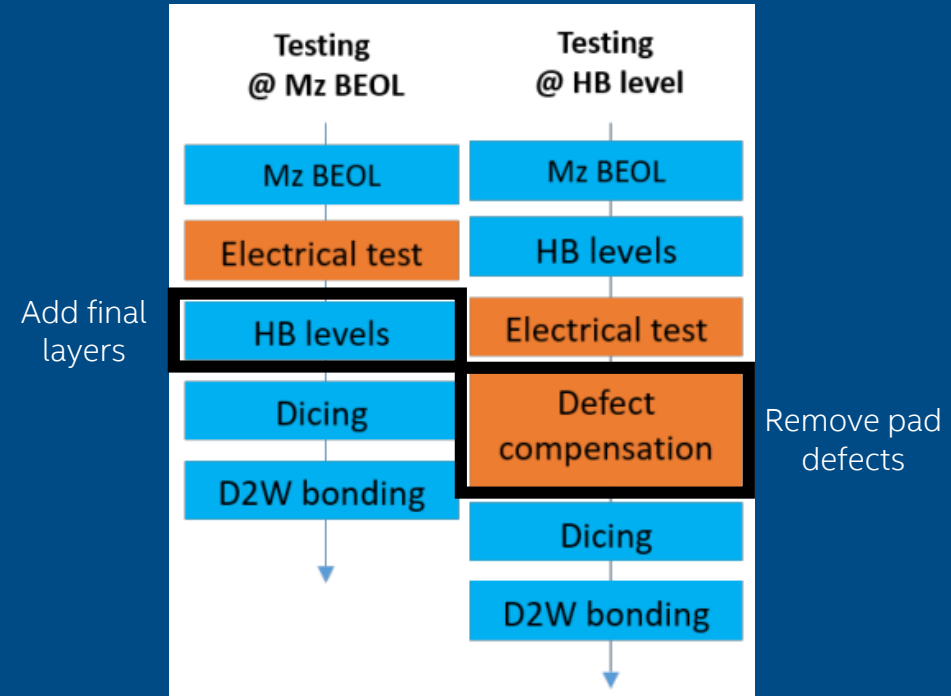
38000, Grenoble

emilie.bourjot@cea.fr



Probe marks are killer defects:

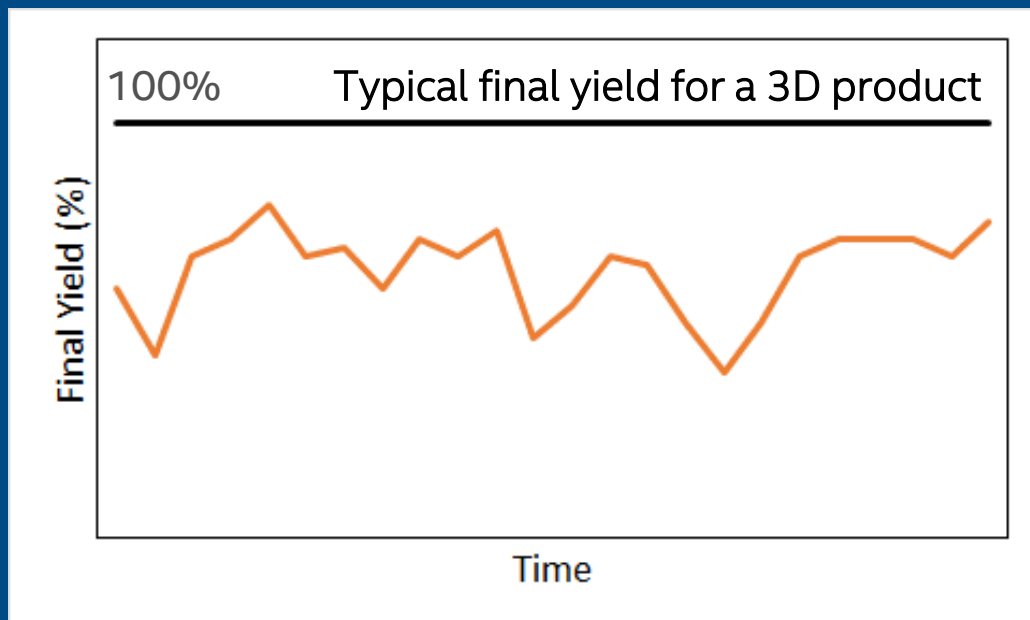
the fidelity of hybrid bonding is highly sensitive to the quality of the copper pad which must be controlled at the nanometer level



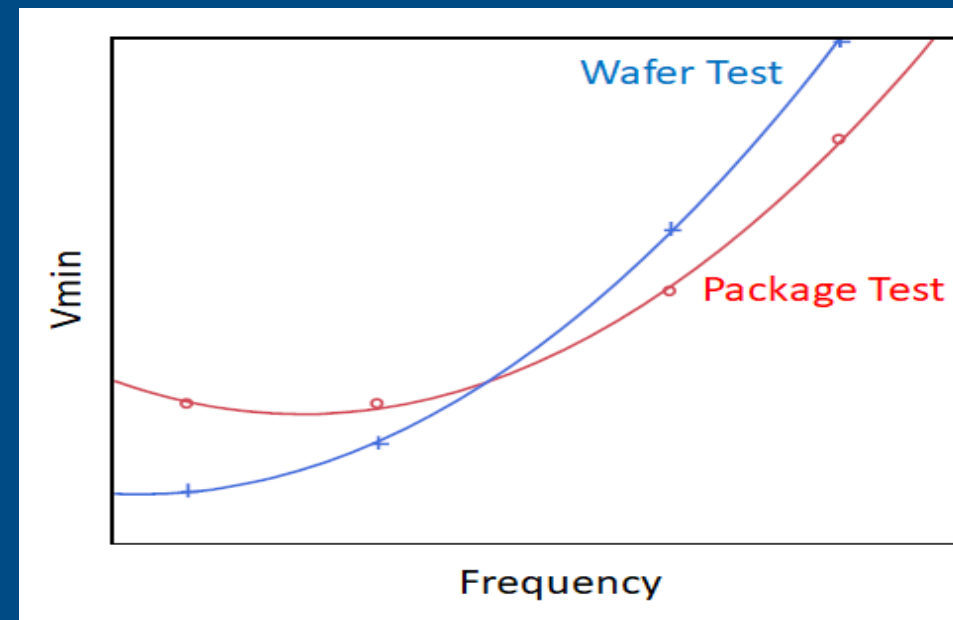
This drives a flow in which wafers are further processed after test to add the final layers or remove pad defects

Some of the proposed hybrid bonding flows lead to an open-loop process and make it very difficult to generate a cKGD

cKGD Production Challenges



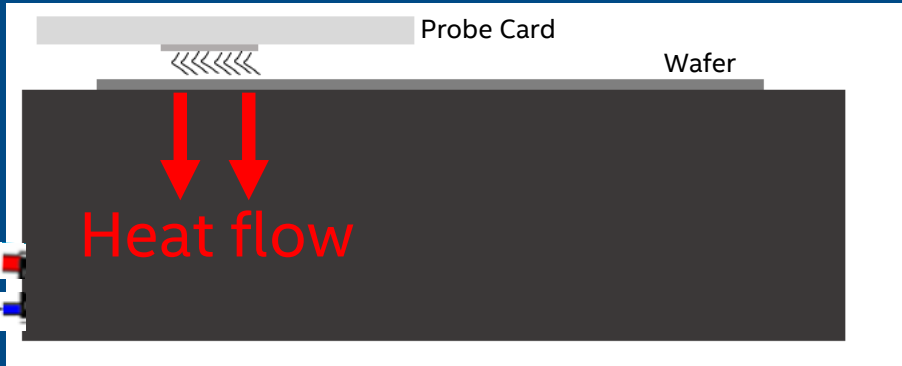
Despite best efforts to produce KGD out of wafer test, there are still a significant number of defects that are being caught at package test



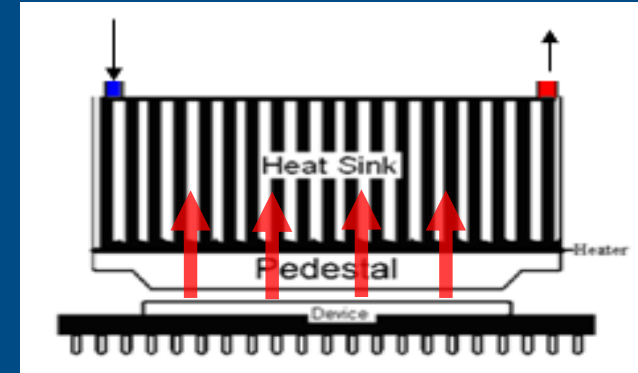
Device performance shifts due to differences in the wafer test vs backend test environment

Differences in wafer test vs backend test environment further complicate producing a cKGD

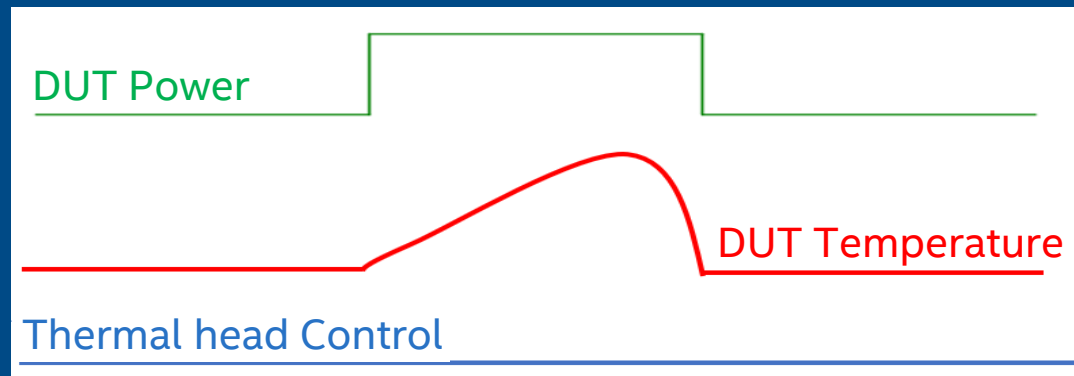
cKGD Challenges: *thermal environment*



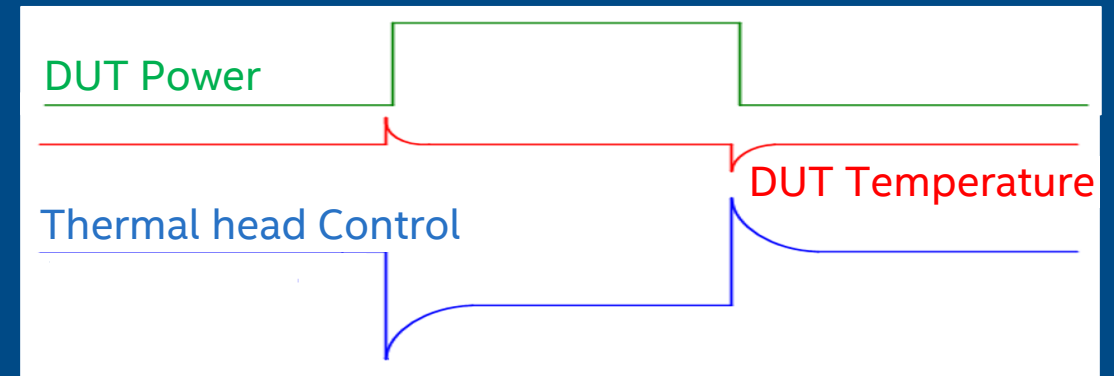
Attributes:
High mass
Passively cooled



Attributes:
Low Mass
Actively cooled



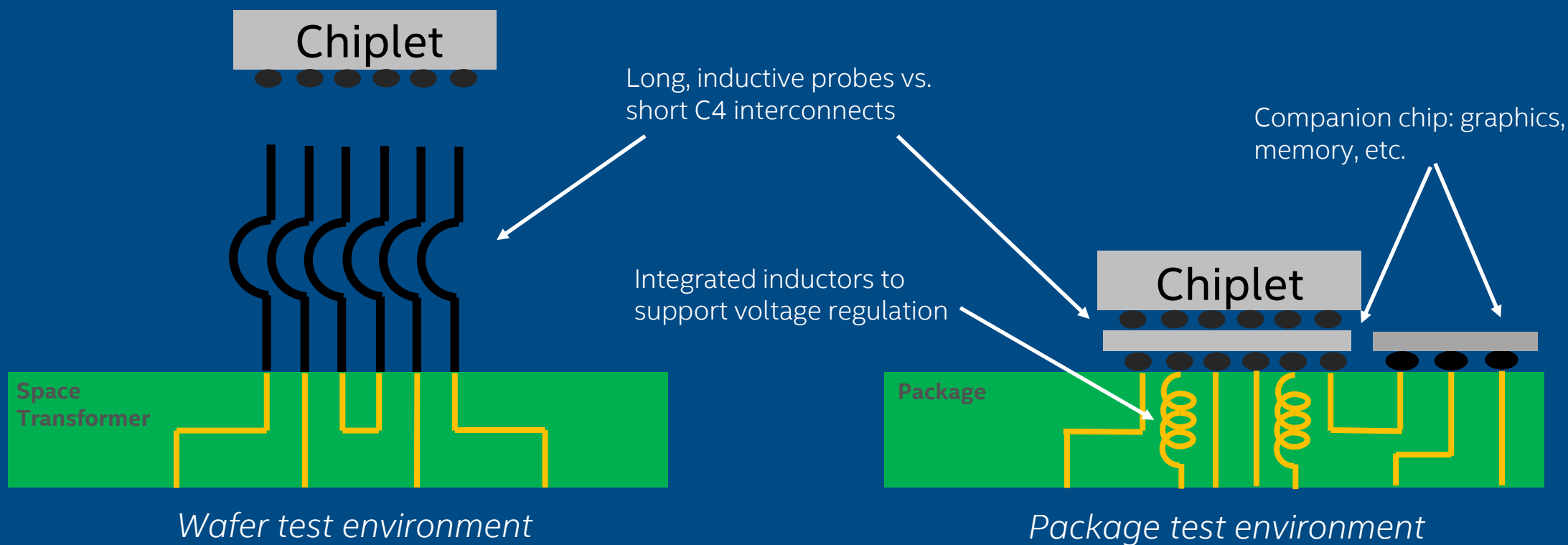
*Wafer test environment:
Junction temperature not maintained during test*



*Package test environment:
Junction temperature maintained during test*

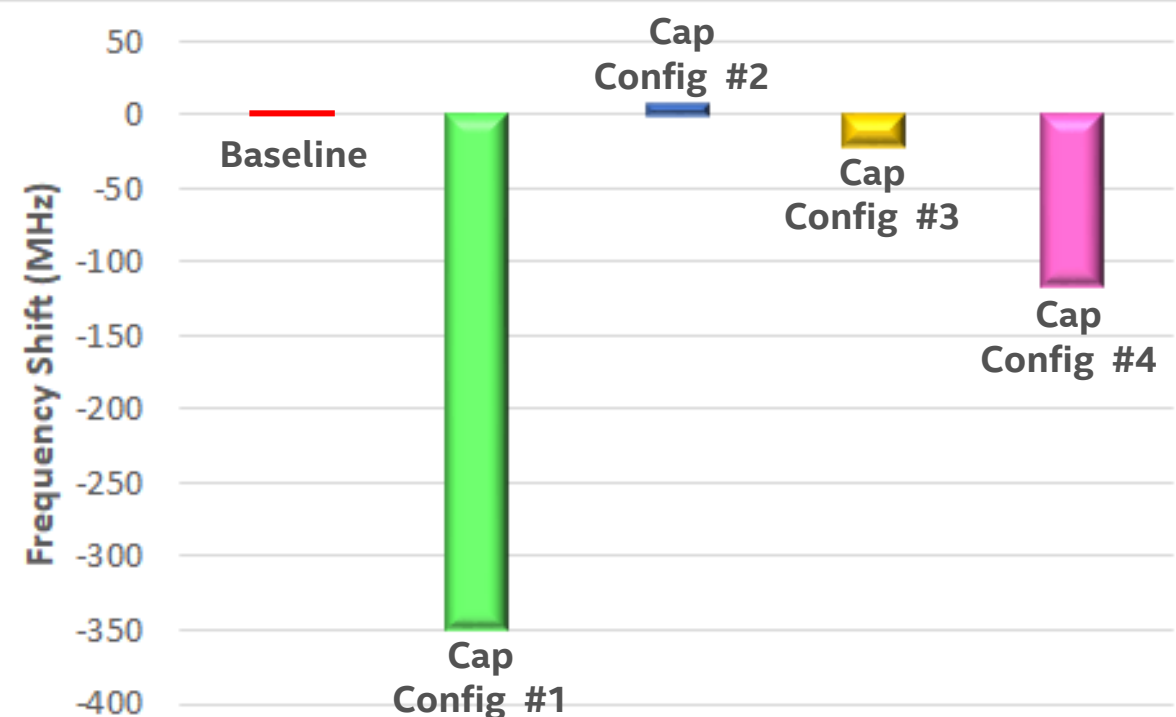
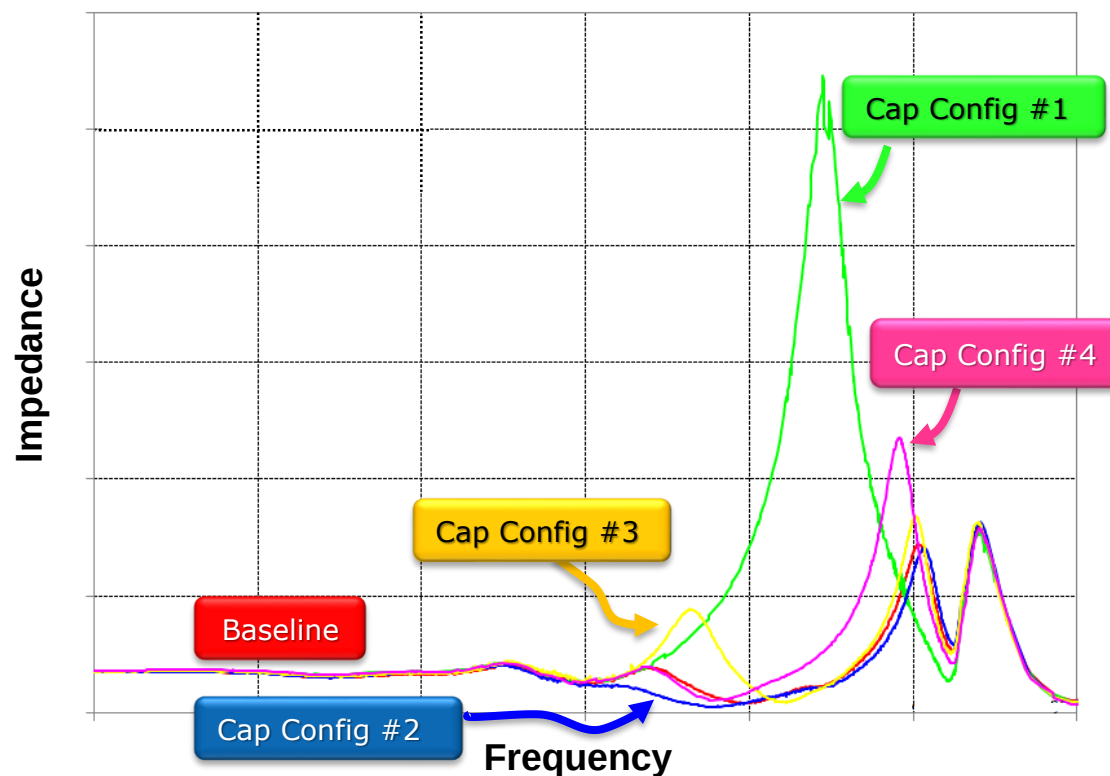
Differences in the thermal environment will affect device performance, characterization, and defect capture rate

cKGD Challenges: *electrical environment*



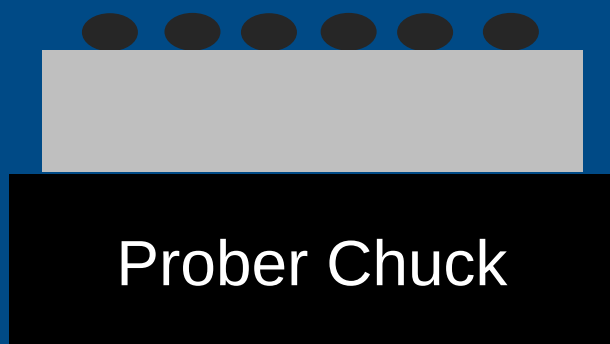
The package is taking on new levels of complexity to enable heterogeneous integration, better power delivery & reduced noise; will the space transformer need to follow?

cKGD Challenges: *electrical environment*



Without innovation, differences in the wafer test and package test electrical environment can affect power delivery fidelity which in turn affects the performance/characteristics of the device

cKGD Challenges: *mechanical environment*



*Wafer test environment:
thick Si held flat by a
vacuum chuck*



*Package test environment:
thin Si susceptible to significant
stresses due to warpage*

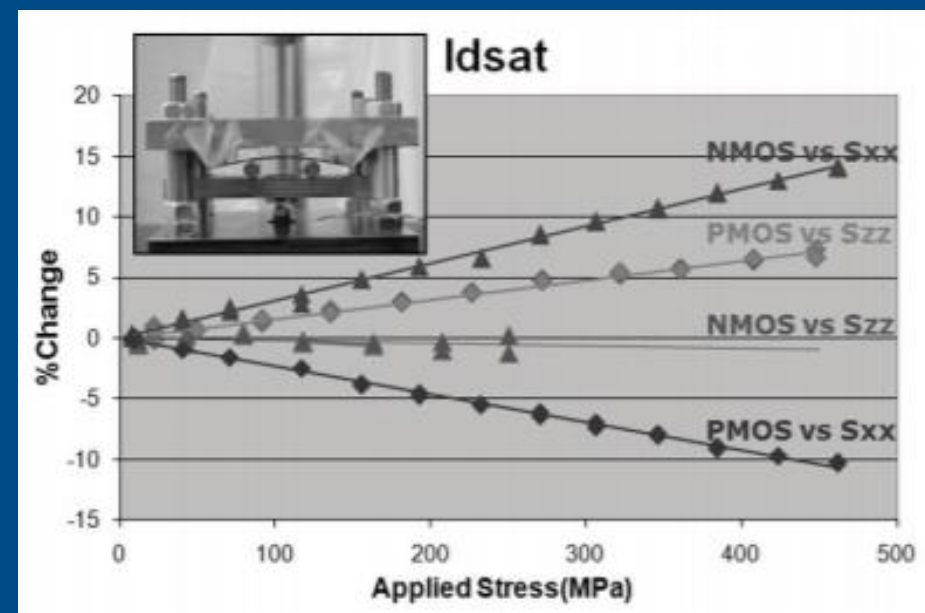
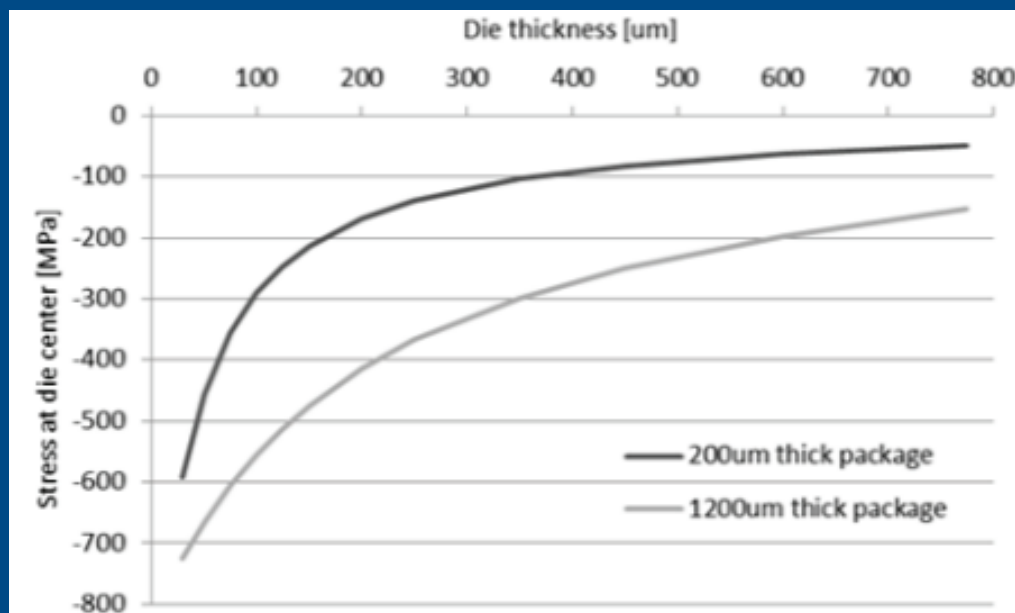
Si experiences different stresses at wafer test vs package test

cKGD Challenges: *mechanical environment*

Die-Package Stress Interaction Impact on Transistor Performance

Gerald S. Leatherman, Jessica Xu, Jeffrey Hicks
Logic Technology Quality and Reliability, Intel Corporation, Hillsboro, OR
503-613-8462, gerald.s.leatherman@intel.com

Bahattin Kilic, Daniel Pantuso
Design and Technology Solutions, Intel Corporation, Hillsboro, OR



Device performance is affected by the mechanical stresses induced on the Si

Is SLT @ Wafer on the Horizon?

SiP Global Summit 2012
系統級封裝與測試論壇

semi

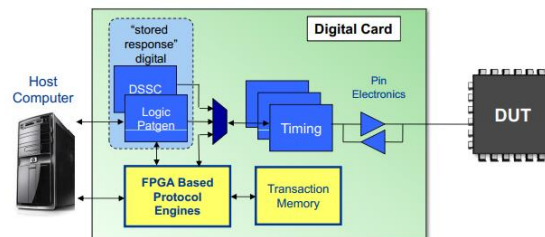


Is System Level Test Practical At The Wafer Level ON ATE For 3D-IC Processors?

Gregory Smith
Teradyne

SLT on ATE is Enabled by
Protocol Aware ATE

SiP Global Summit 2012
系統級封裝與測試論壇



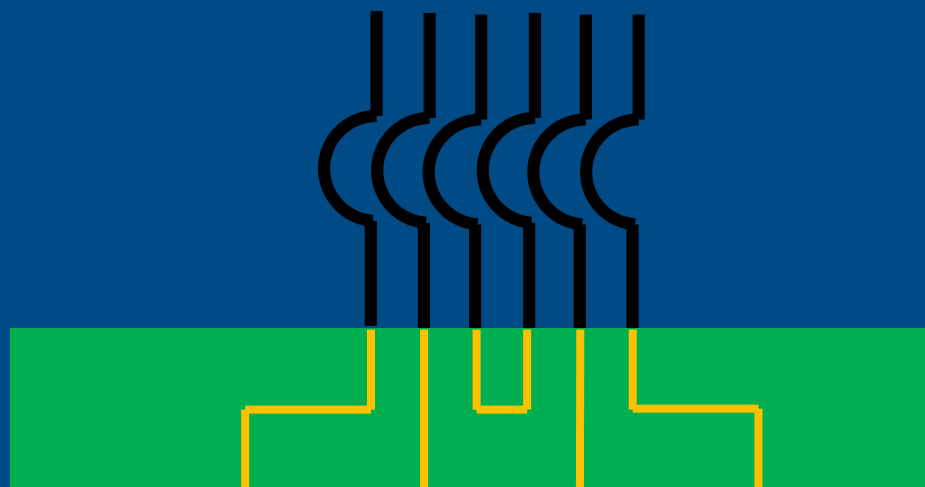
- PA Architecture integrated into **Digital** Instrument
 - Select Protocol Aware or Standard Digital on any pin
 - Used Together with Scan, BIST, etc.
- “Real Time Intelligence” To communicate with DUT
- FPGA architecture allows flexibility and **low latency**

Booted
Windows at
wafer level!



Enabling SLT at wafer level is doable, but with a high degree of complexity

Future Wafer Test?

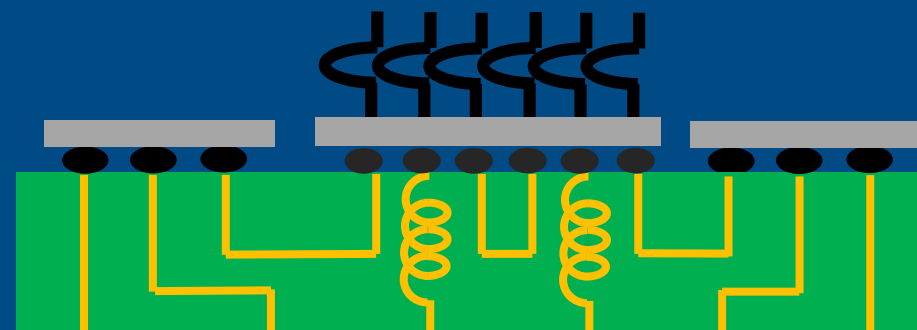


ATE

Today

Attributes:

Short probes, capable of high temperature test
Organic ST w/all the internal features of a package
Companion die
SLT capable ATE
Active thermal control wafer chucks

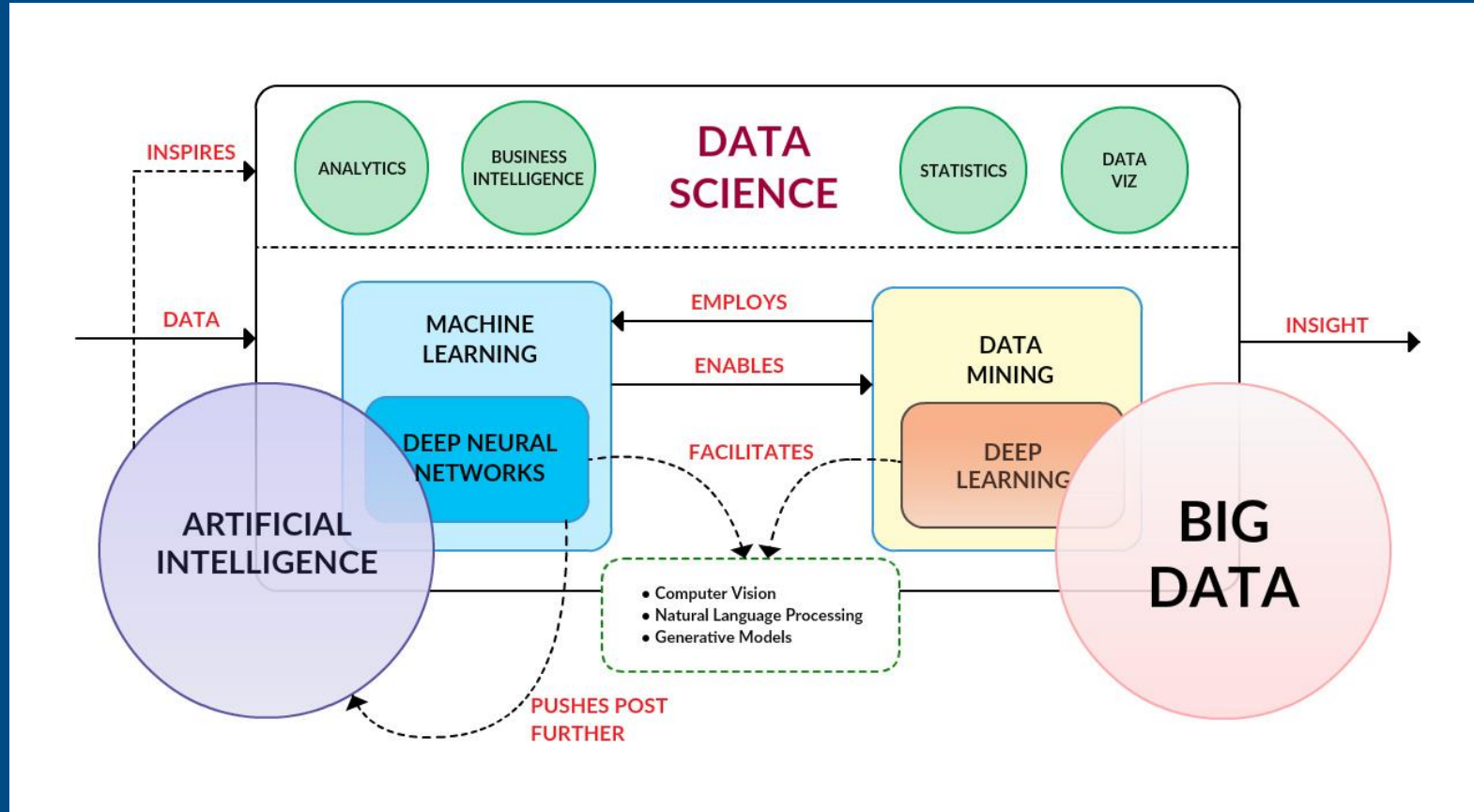


SLT Capable ATE

Future?

Everything is possible, but is this affordable?

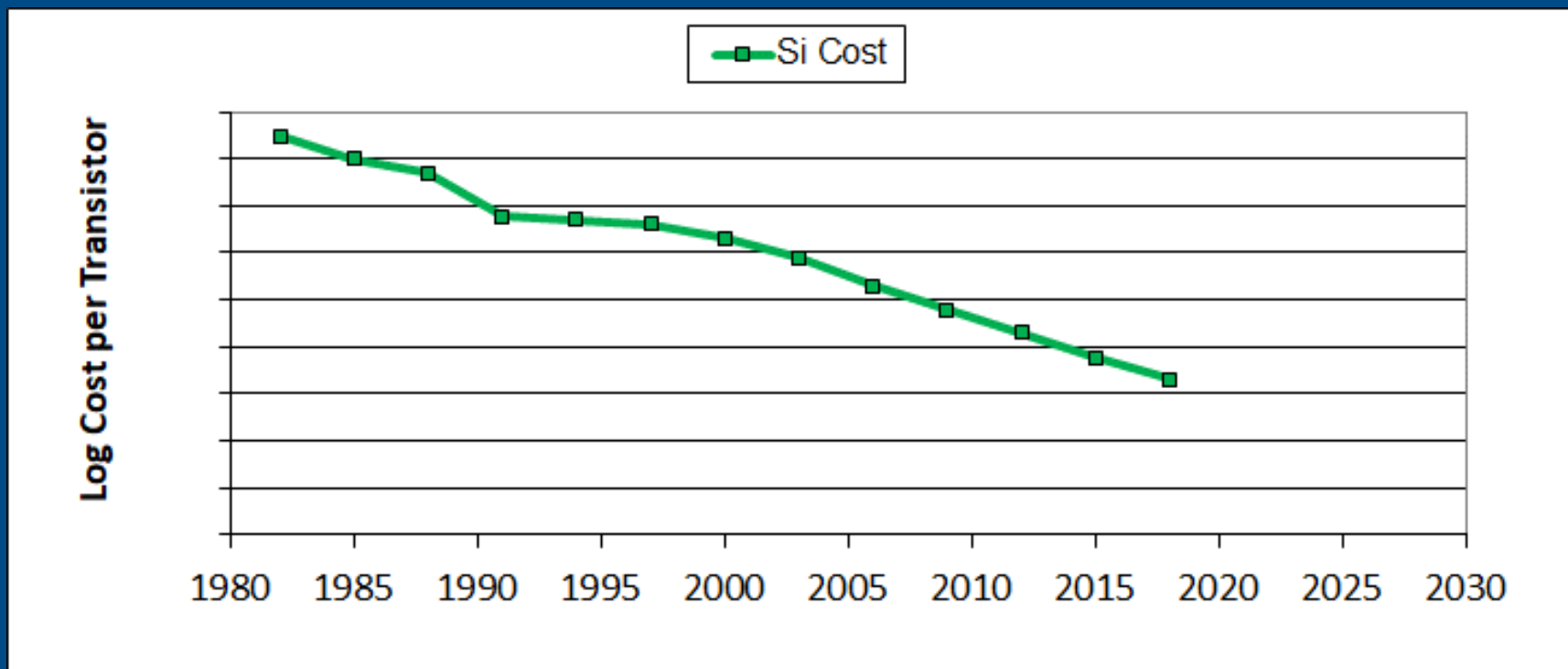
Big Data and AI: *adaptive test on steroids*



Source: Whatsthebigdata

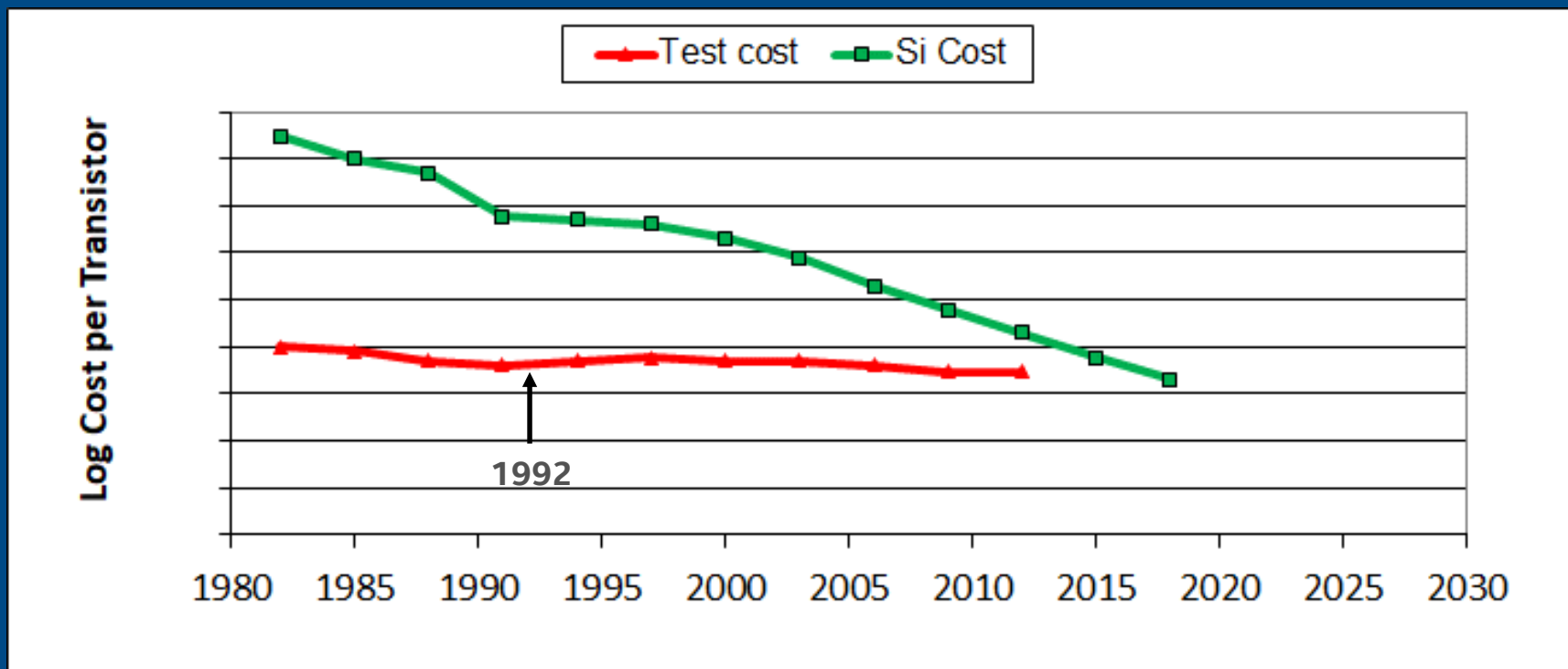
Test will need to rely on AI and enhanced Big Data analytics to better predict chiplet performance in end-use environment

Moore's Law: *it's really an economics law*



The economic component of Moore's Law has enabled >7 orders of magnitude growth in transistors over the last 50 years, despite increasing complexity in manufacturing process

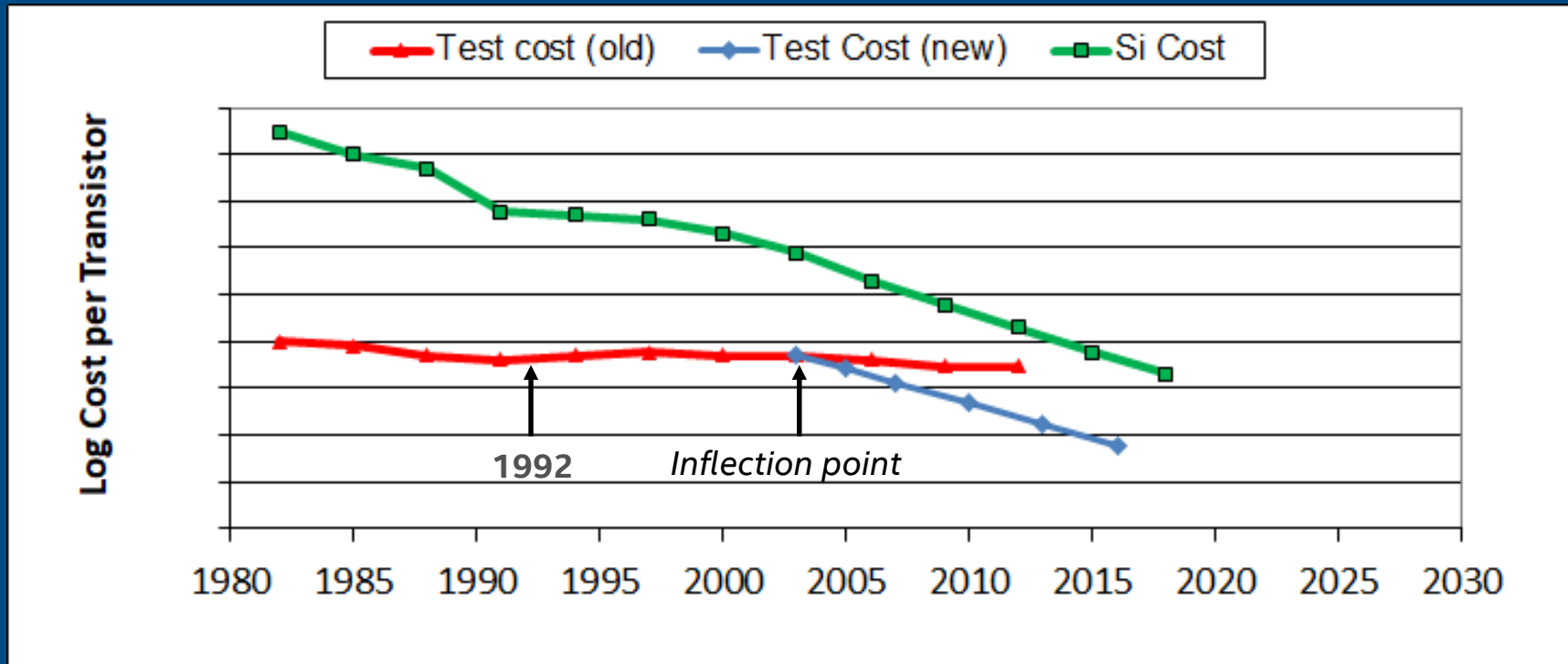
Moore's Law: *it's really an economics law*



Source: SIA Roadmap, circa 1992

In 1992, it was forecasted that the cost to test a transistor would exceed the cost of manufacturing a transistor within ~two decades

Moore's Law: *it's really an economics law*

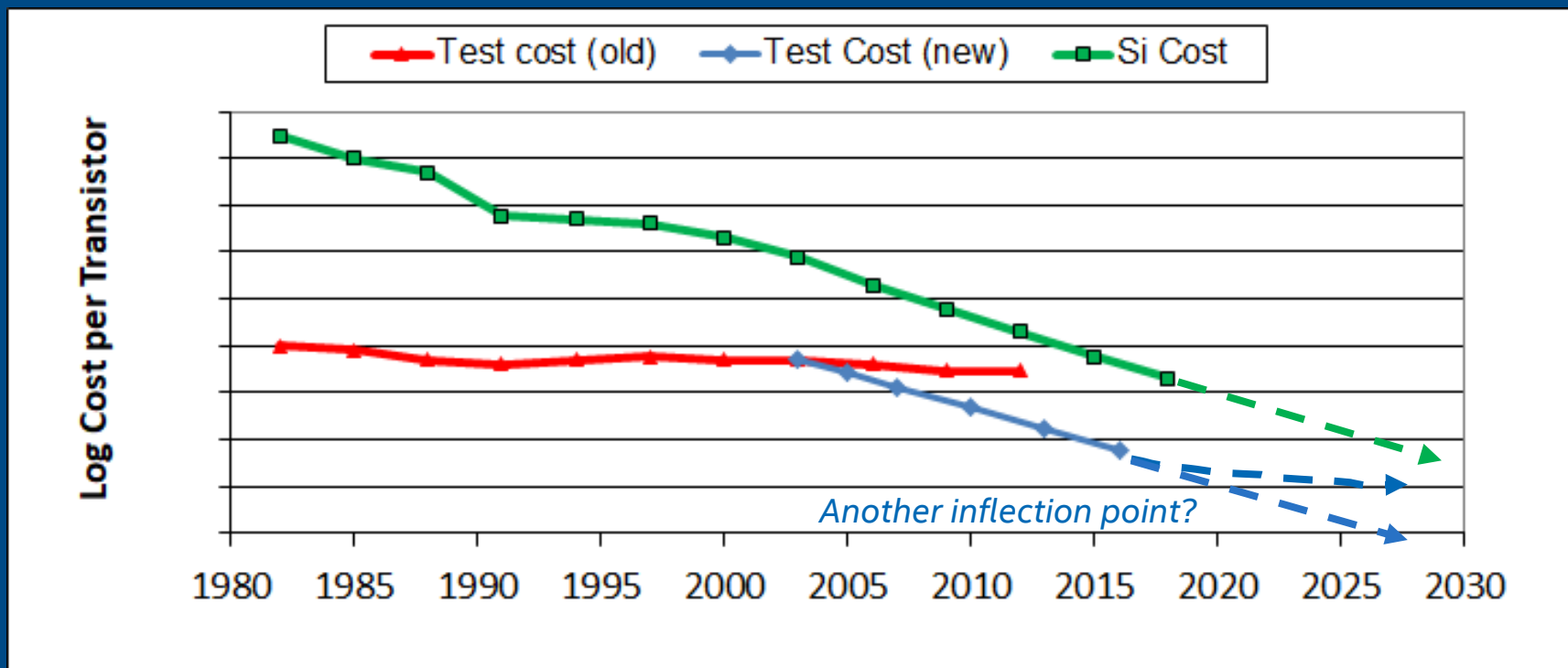


Source: SIA Roadmap, circa 1992

Source: ITRS Roadmap, circa 2001

Within a decade, through a lot of ingenuity and hard work, test cost was forecasted for the first time to track Si cost

Moore's Law: *are we at an inflection point?*



Source: SIA Roadmap, circa 1992

Source: ITRS Roadmap, circa 2001

Heterogeneous integration is going to challenge test cost, and innovation is needed to keep the cost curve on the same trajectory

Summary

- Moore's Law will continue, as long as people have new ideas
- Die disaggregation and heterogeneous integration is the next frontier along the continuum of Moore's Law
- These trends drive the need for cKGD and will have a significant impact on future test strategy and the test industry
- Test must not become a limiter: innovation is required from interconnect technology to tester instruments to enable a cost-effective test strategy