

Opto-electronical probe card for high-volume wafer level test of photonic integrated circuits

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MORE LIGHT

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sicoya

PROBE TODAY, FOR TOMORROW

Content

- Application and background
- General test solution and setup
- Working principle
- Demonstrator
- Lab measurements and feasibility results
- Wafer prober compatibility
- Wafer-level test of EPIC DUT
- Conclusion and Outlook

Application and Market requirements

UFO Probe™ - ultra-fast opto-electronic probe card.

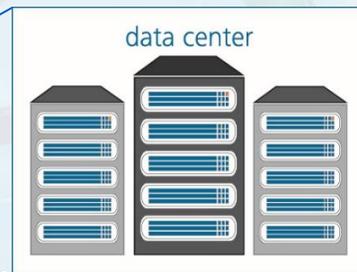
JENOPTIK developed a solution for high-volume wafer level test of photonic integrated circuits (PIC) for optical transceivers.



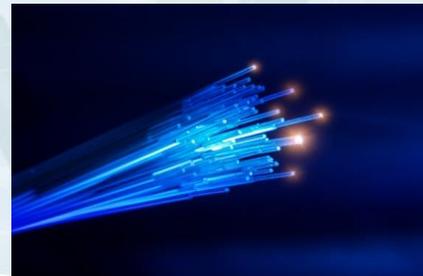
What's the driver?



Connected World



Higher data rates

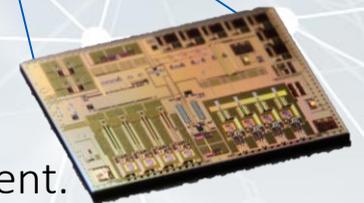


Optical communication.



Signal conversion

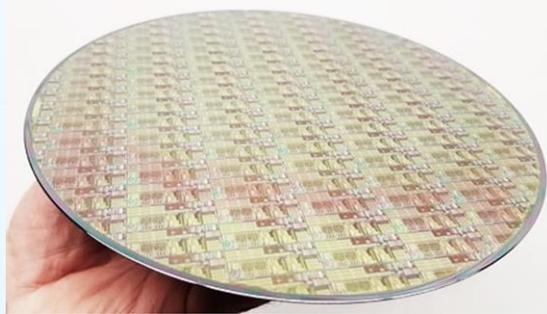
PIC as core component.



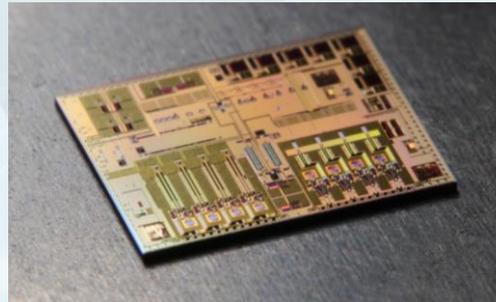
PROBE TODAY, FOR TOMORROW

Application and Market requirements

Fabrication of photonic integrated circuits in CMOS technology



CMOS Wafer



Electronic Photonic Integrated Circuit



Optical ASIC or Module

The PIC ecosystem is still under development.

It needs to

- align with CMOS fabrication chain,
- meet current industry standards,
- reduce costs!

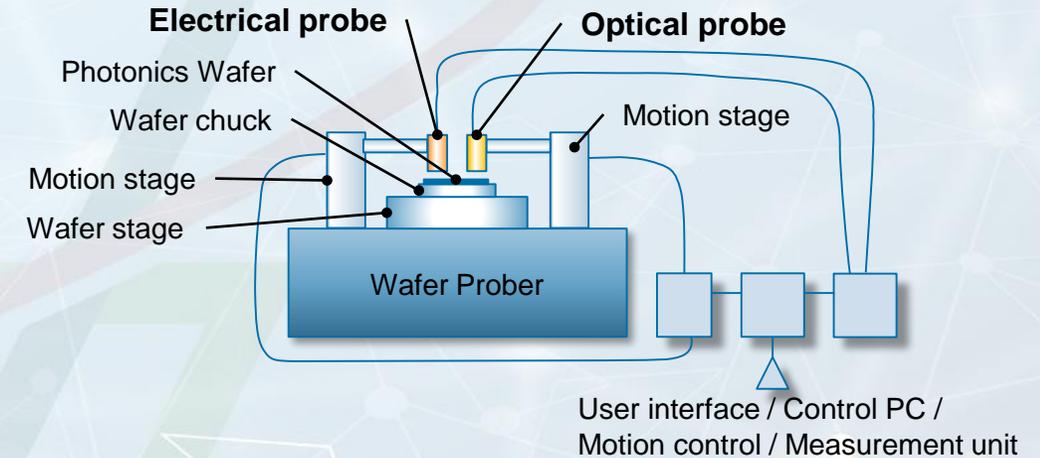
→ **Opto-electronical testing plays a vital role!**



Current and Ideal Wafer Level Test Solutions

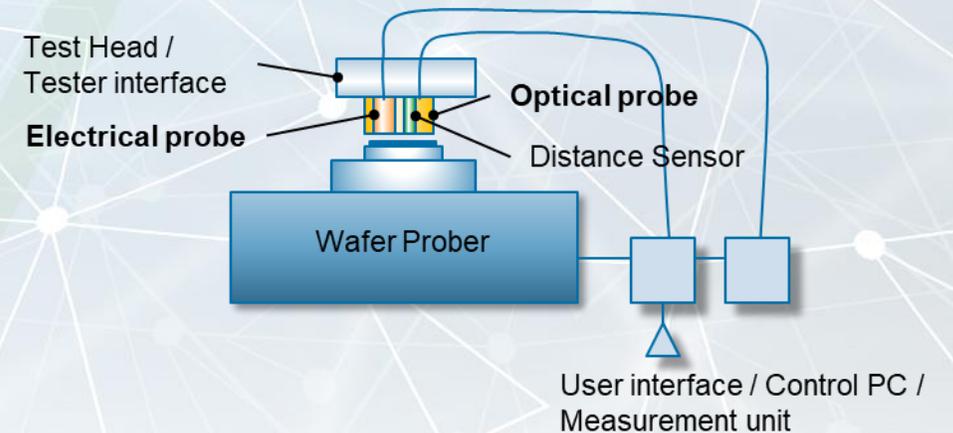
Current solutions

- Fiber based
- Active alignment in sub-micrometer range
- Separated probes - electrical and optical
- Dedicated or customized probing equipment
- Little to no possibility of parallelization



Ideal solution

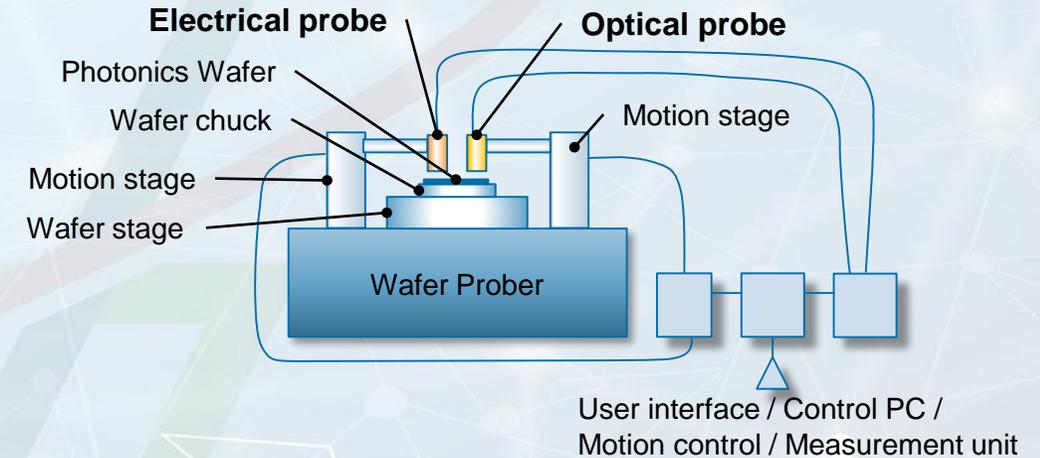
- **Plug & Play** ready for existing standard IC wafer probers and automated test equipment
- **No active alignment** time per chip
- **Parallel qualification** → multi-DUT regime
- Operated by same personnel as standard IC equipment



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Ideal solution

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Consequences

- optical and electrical probe in **one probe card**
- Compatible to existing interfaces
- Deal with **,coarse'** prober alignment tolerances
- **Optics** that works **alignment insensitive**
- **Scalable** solution with simple handling

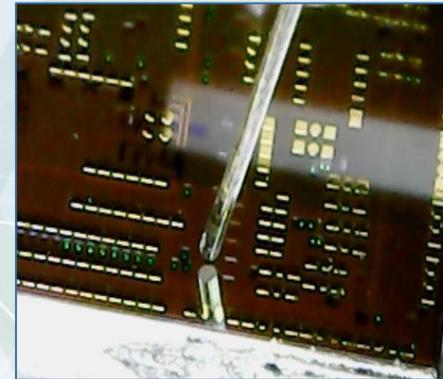
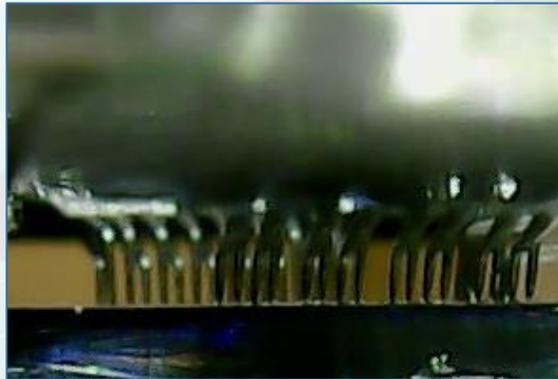
Working Principle

Big Question:

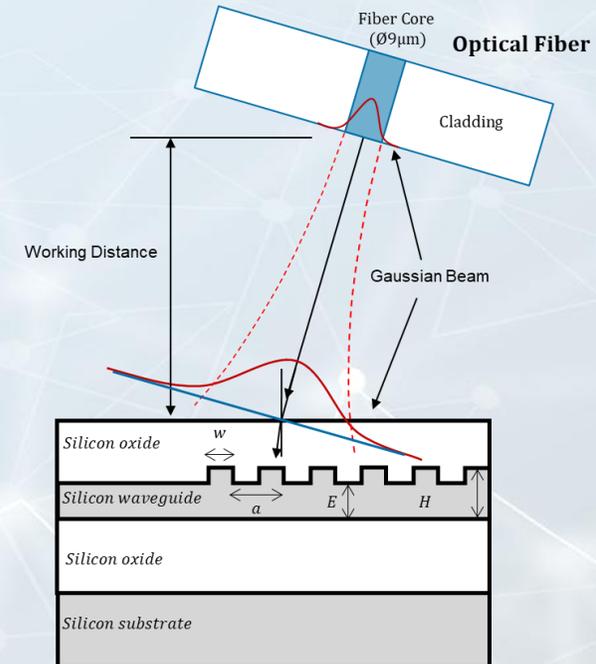
- How to get ELECTRICAL and OPTICAL probes together?



Micrometer position tolerance at bond pad



Sub-Micrometer position tolerance at grating coupler

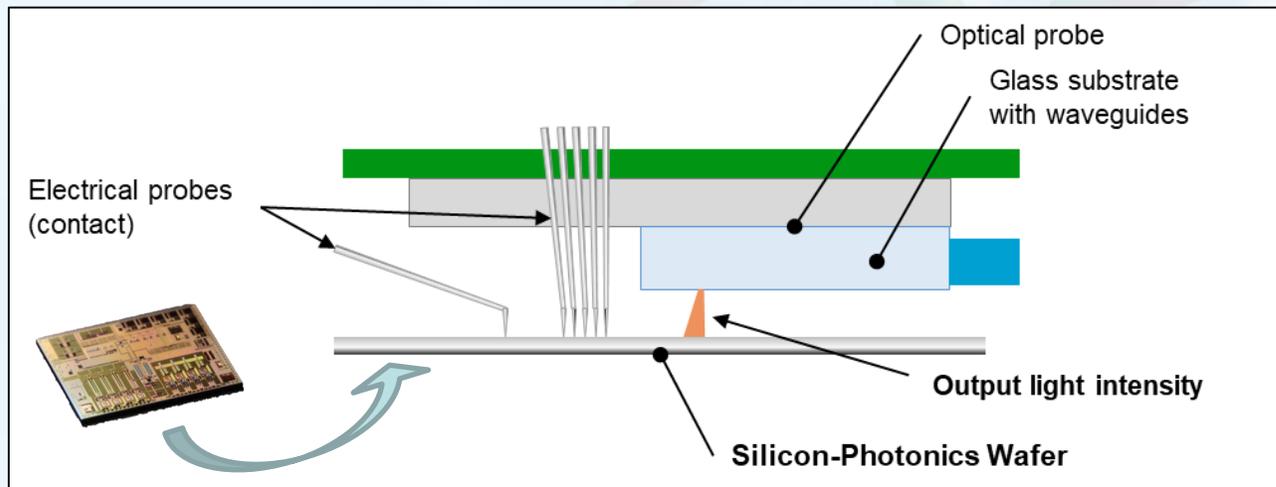


Working Principle

Challenge of an opto-electronical probe card:

- Realize an alignment insensitive optical probe.

Schematic of the UFO Probe principle



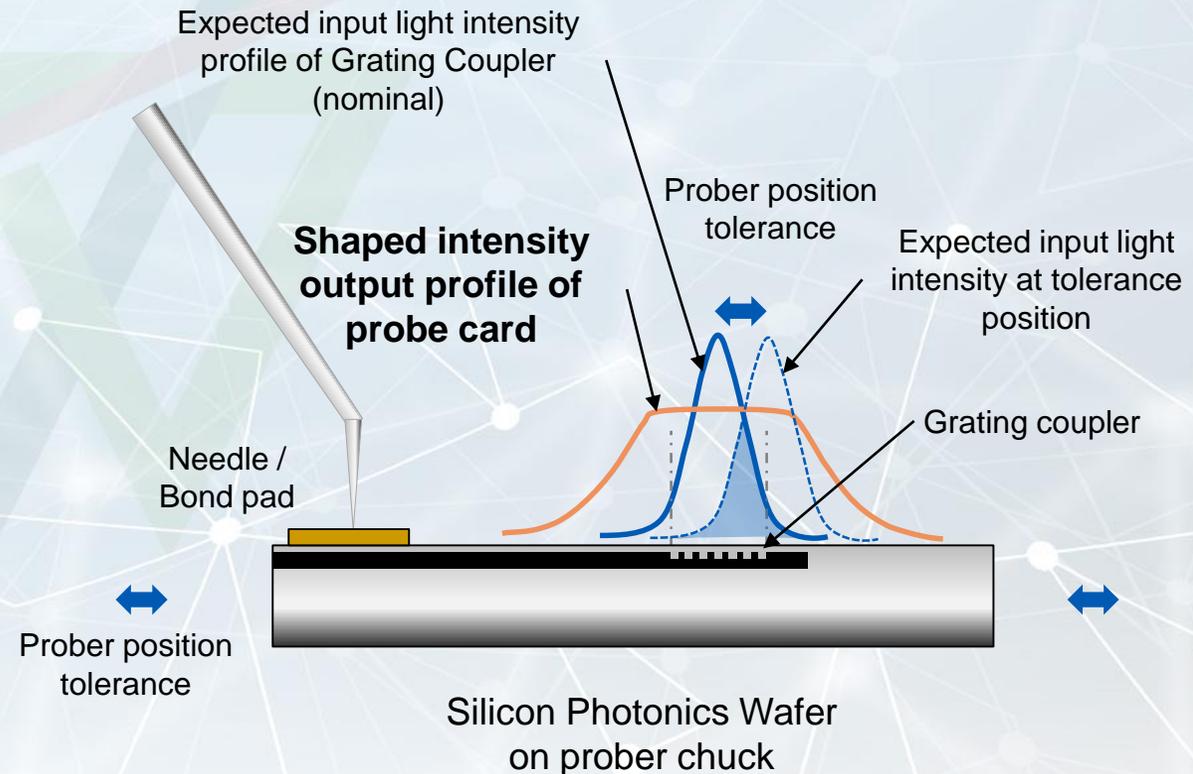
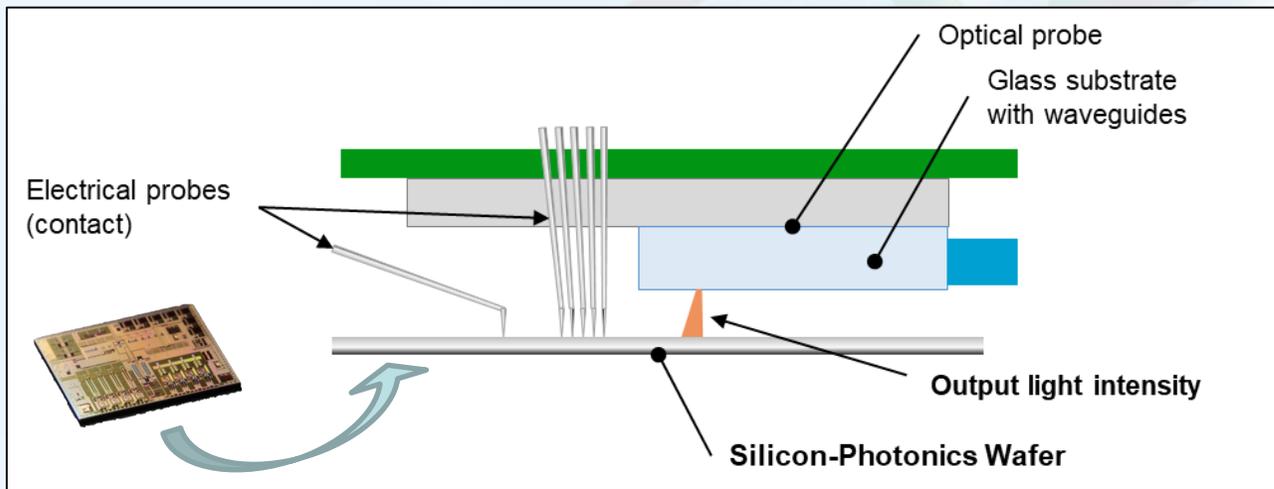
Working Principle

Challenge of an opto-electronical probe card:

- Realize an alignment insensitive optical probe.

Optical concept compensates prober alignment tolerances.

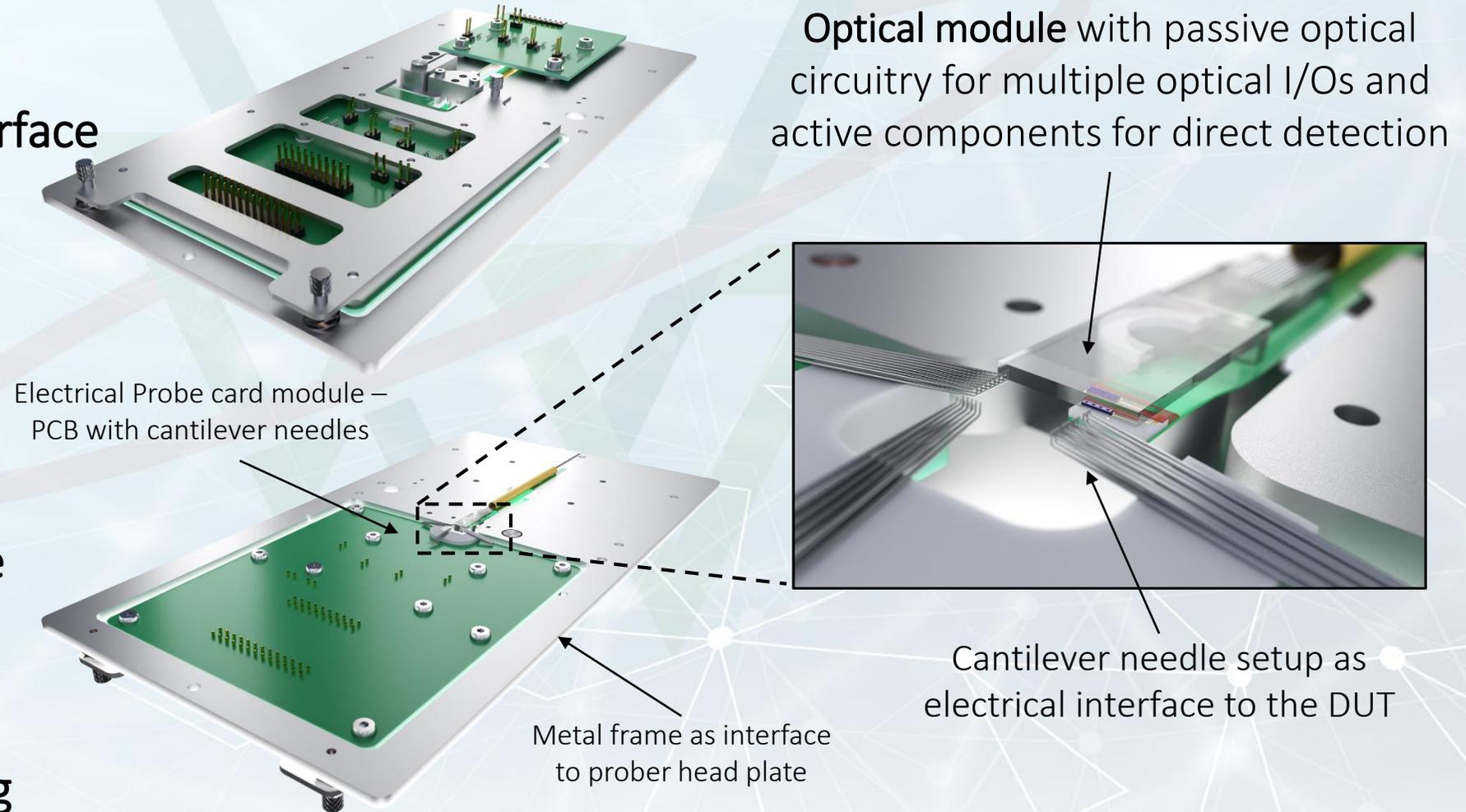
Schematic of the UFO Probe principle



Technical Realization of Demonstrator

Demonstrator

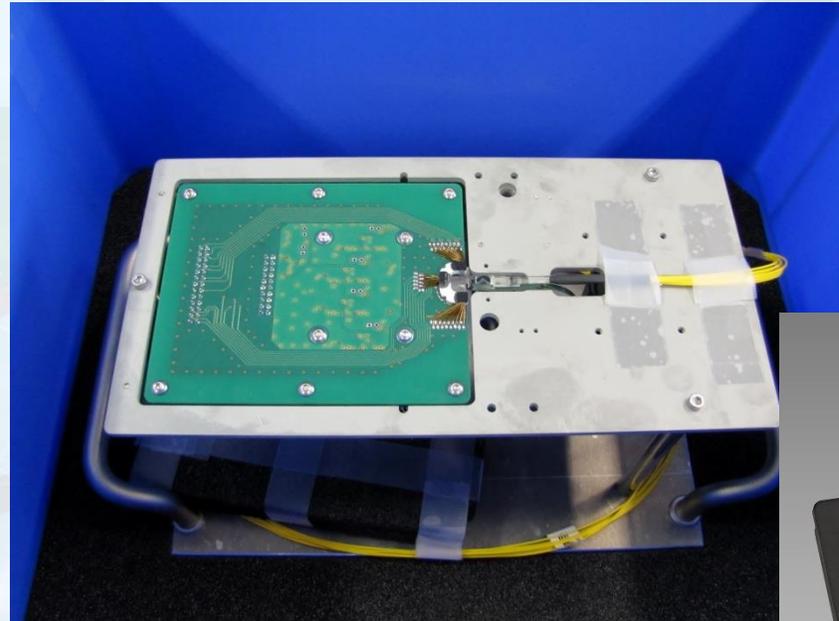
- Standard prober interface (Eurocard format)
- Monolithic optical module
- 16 optical I/Os
- Alignment insensitive optical coupling
- Simultaneous optical and electrical probing



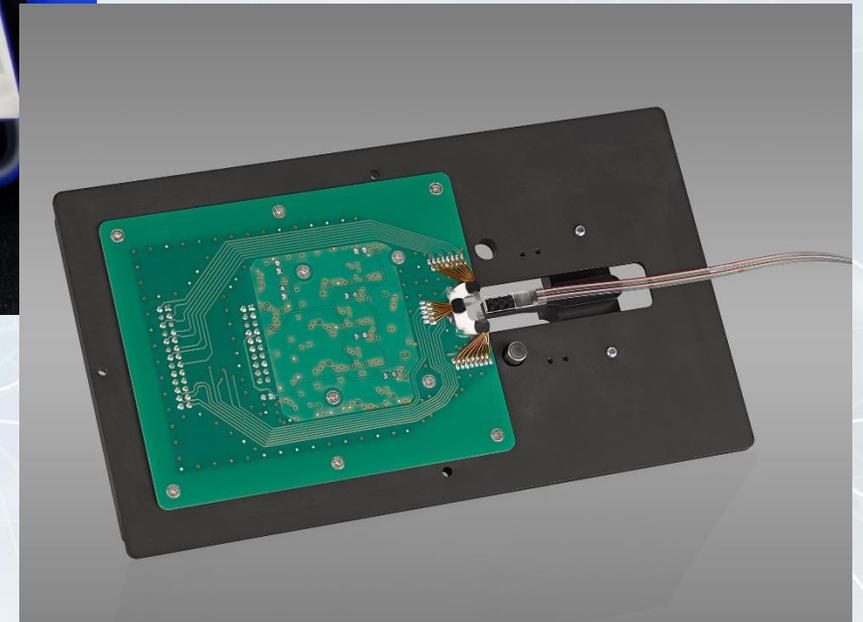
Technical Realization of Demonstrator

Demonstrator

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Functional Model for lab verification and integration purposes

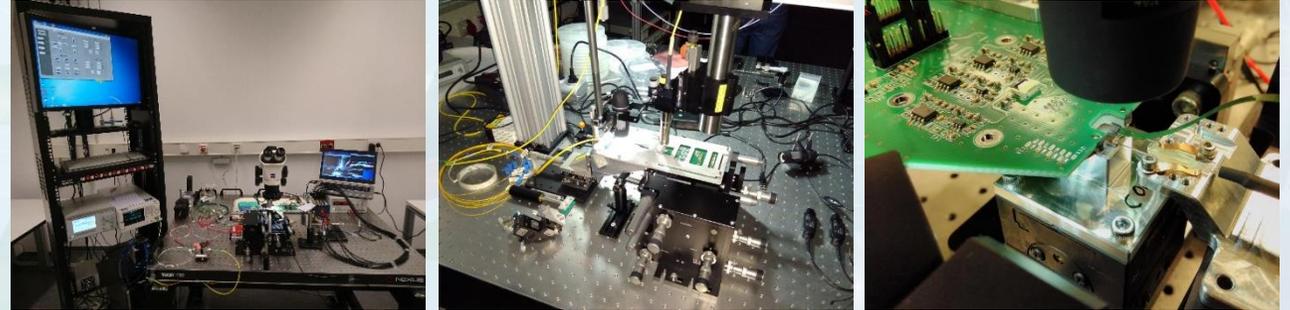


Functional Model for prober compatibility check

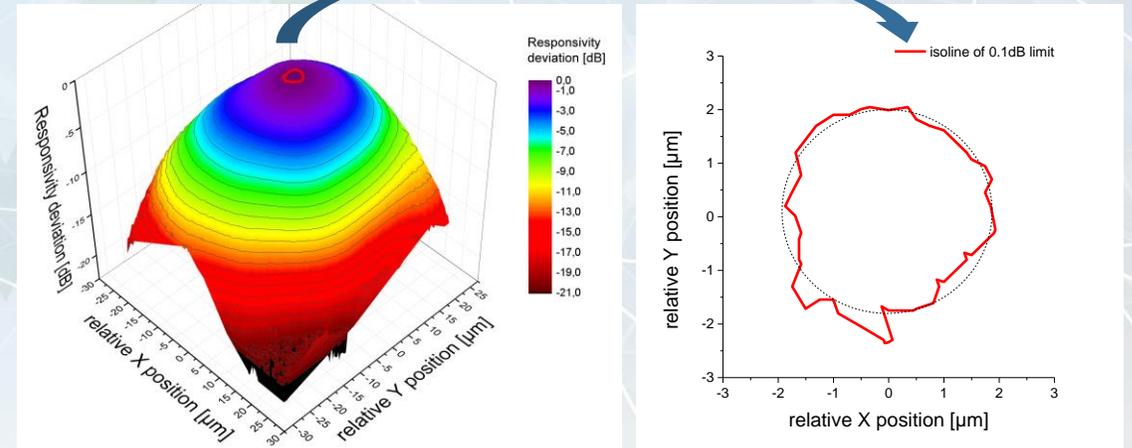
Demonstration of Working Principle

Conformation of optical working principle under lab conditions

- Build lab setups for raster scan, free space imaging, integration feasibility
- Manufacturing setups
- PIC samples provided by Sicoya
- Measured displacement for -0.1 dB sensitivity range
 - RX channel: $\pm 1.9\mu\text{m}$
 - Alignment loop: $\pm 1.0\mu\text{m}$



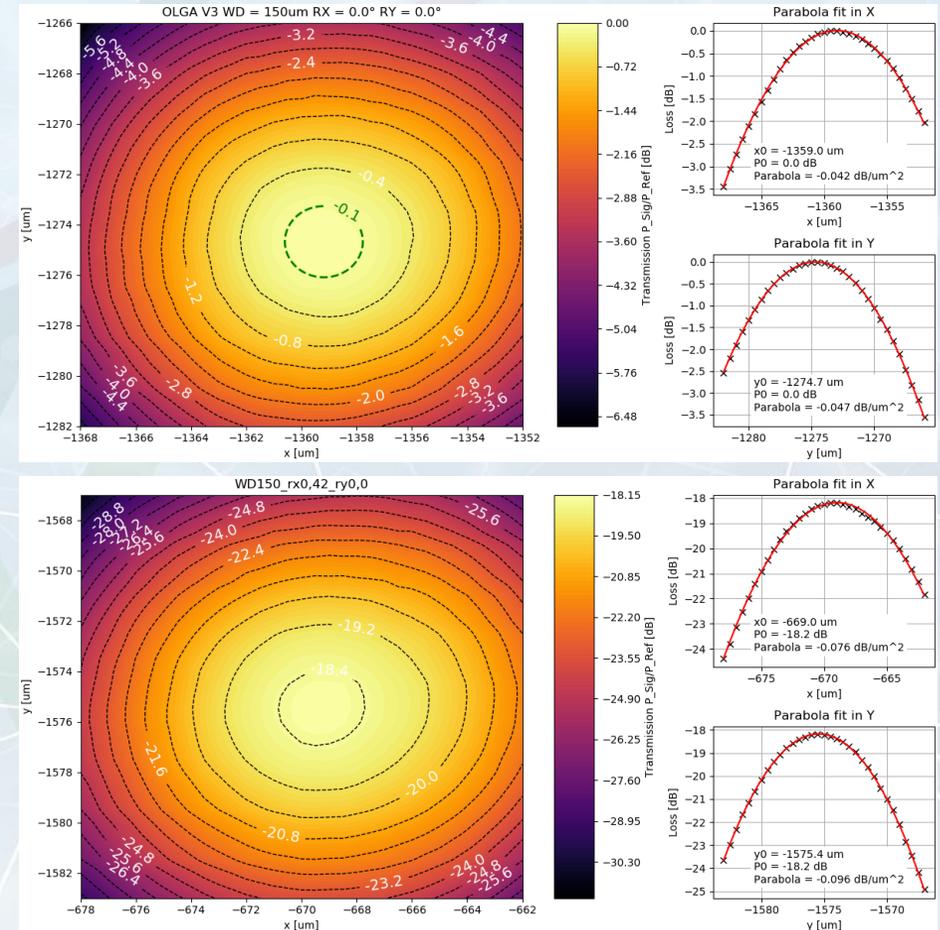
→ Working principle of probe card confirmed



Demonstration of Working Principle

Conformation of optical working principle under lab conditions

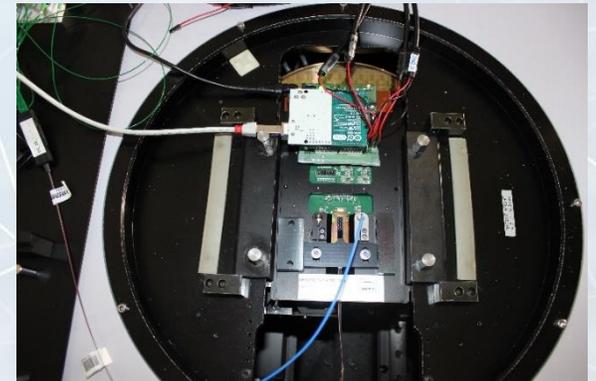
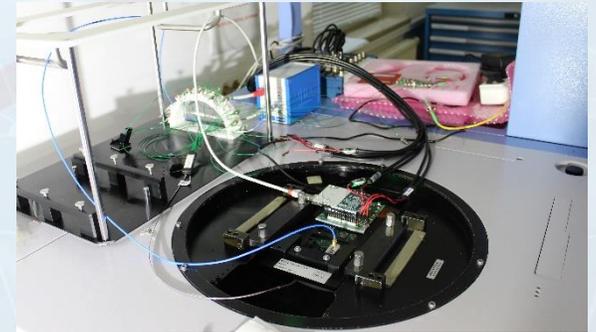
- Raster scans for different optical modules together with PIC
- Optical working distances (WD): typical 50 - 200 μm
- Alignment sensitivity: $\pm 1.25 \mu\text{m}$ @ -0.1dB and 150 μm WD
- Setup insertion loss : $\sim -18\text{dB}$ to -24dB (incl. loss of optical module, over-illumination, DUT with GC and waveguide)
- Challenge:
Alignment insensitivity, insertion loss and optical working distance are not independent parameters to optimize.
→ Find optimum for test case.



Prober compatibility

Conformation of optical working principle - fab conditions

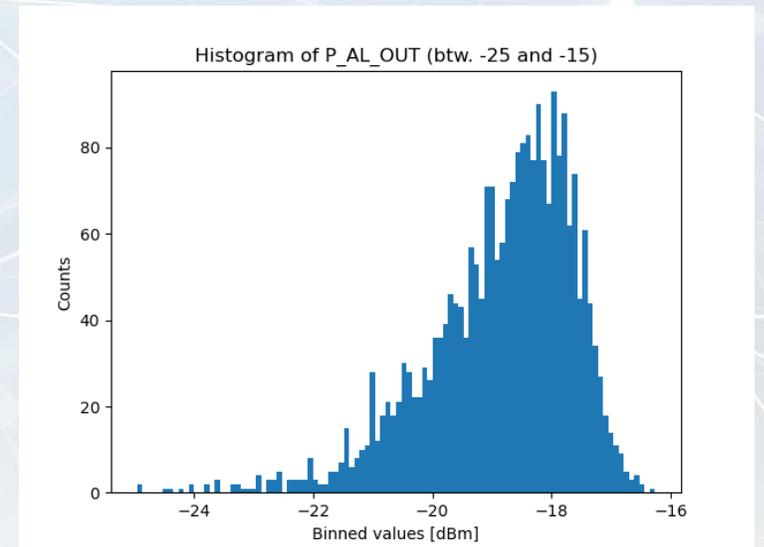
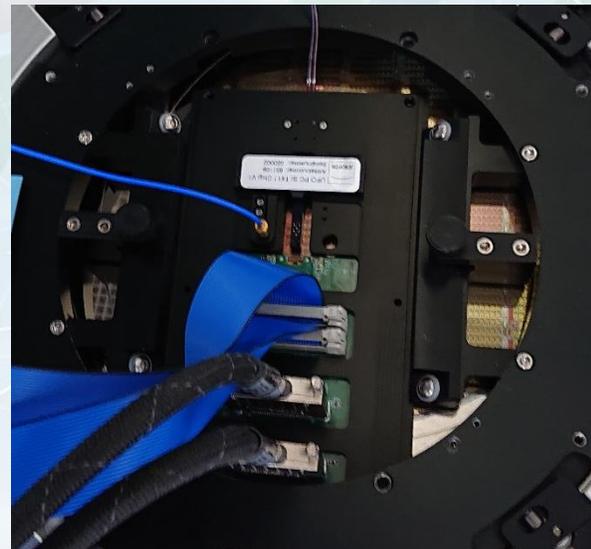
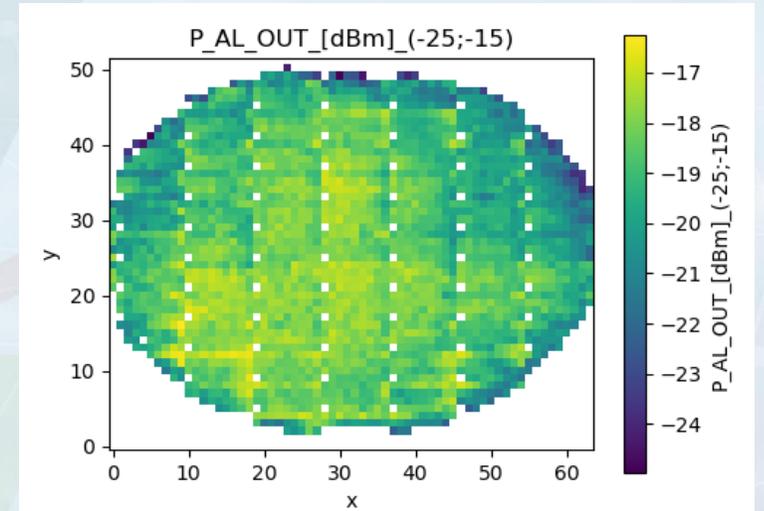
- Initial wafer-level tests on an Accretech UF200R prober
 - Mechanical probe card interface
 - Communication with prober
 - Needle and probe card alignment
 - Optical test of PIC alignment channel
- Further tests on Accretech UF3000EX under test floor conditions
 - Online Cleaning successfully demonstrated
 - Probing stability and working distance
 - Alignment procedure and full test program



Device Wafer-level Test – Optical Alignment Channel

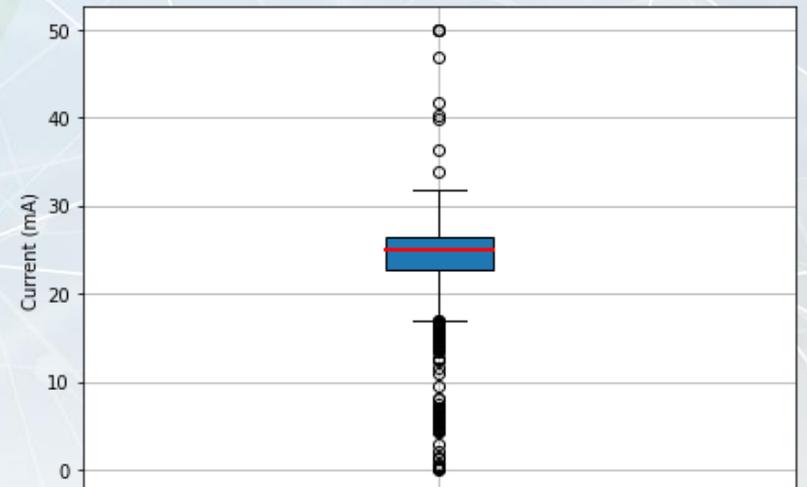
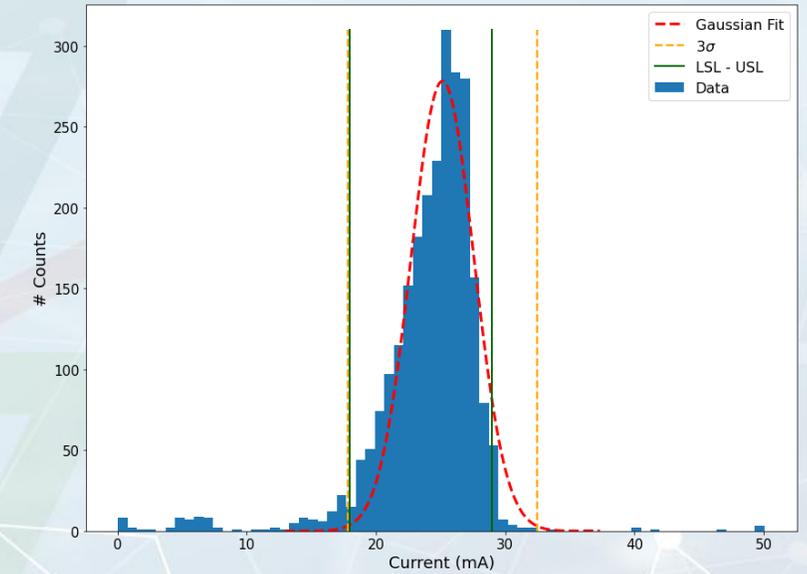
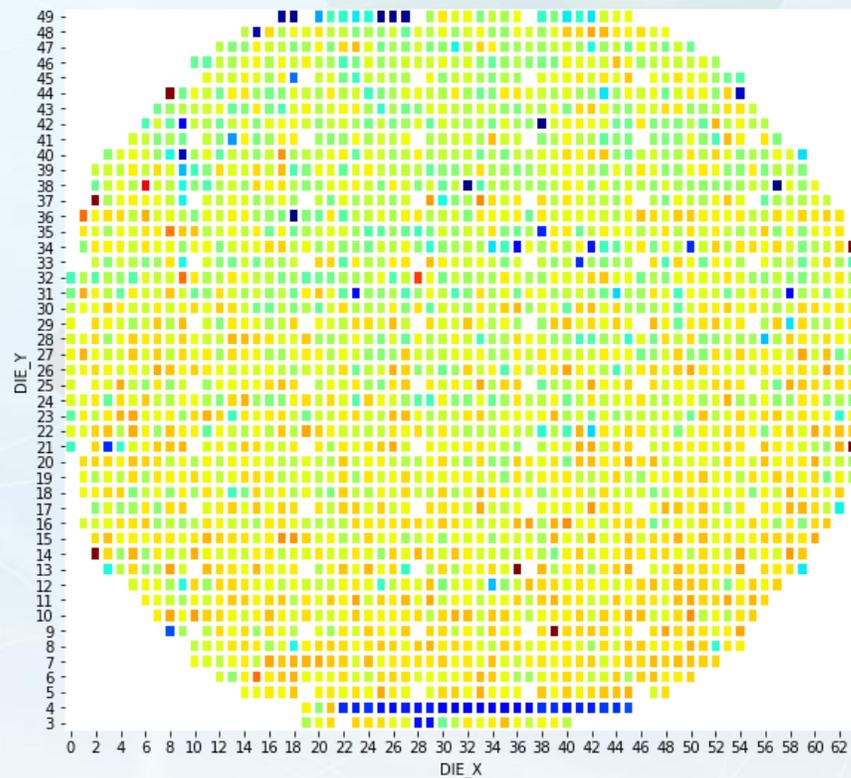
Wafer-level test of transceiver device

- Final production test
- RX, TX, alignment channel and comprehensive electrical tests in a single touch-down
- 1x alignment per wafer, no additional alignment per chip
- Example of wafer map for optical alignment channel



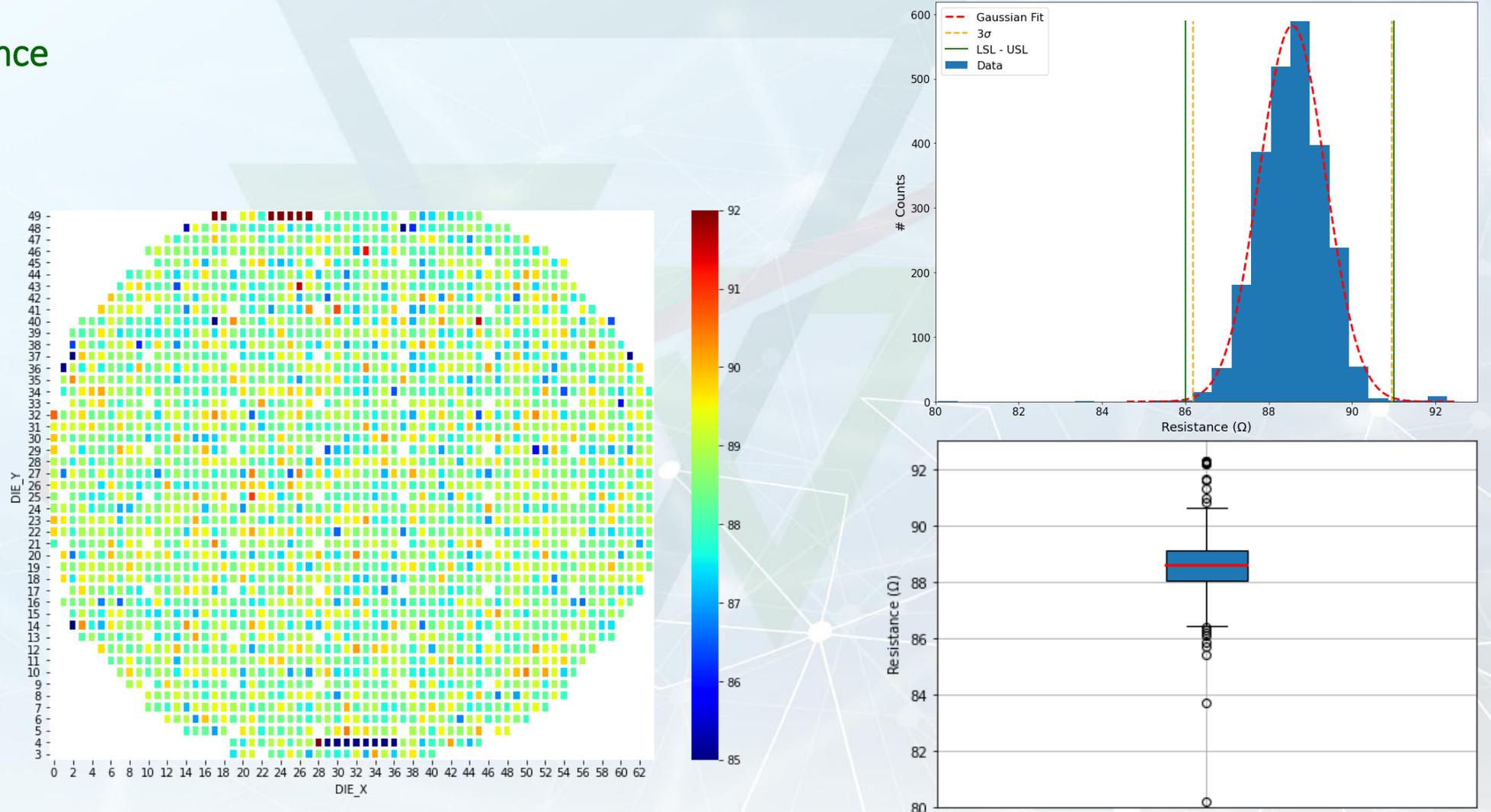
Device Wafer-level Test – Receiver input current

- Receiver supply current I_{VCCA} , $VCCA = 2.5\text{ V}$
- Current supply for RX input buffer, bandgap reference, RX CDR, RSSI detector, FSM Vtune



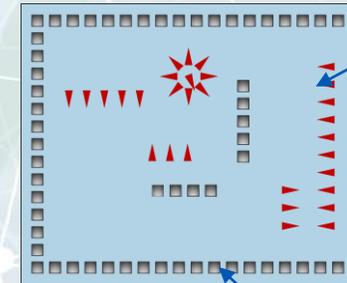
Device Wafer-level Test – Contact Resistance

- Contact Resistance



Conclusion & Outlook

- Realized a monolithic opto-electronical probe card for PIC measurement
- Proved working principle under lab and test floor conditions
- Showed compatibility with standard prober equipment
- Established final test for production runs
- Evaluation of insensitivity range vs. absolute loss ongoing
- **Next steps:**
 - Improvement of insensitivity range
 - Platform development for other needle types
 - RF capable probe card
- **Outlook:** probe cards for multi-DUT and high count optical I/O testing (switches)



Grating couplers,
'arbitrary' position and
orientation for:

- Fiber arrays
- Fiber bundles
- Single fibers
- Laser diodes

Bond pads with
'arbitrary' position

The background features a light blue and green color scheme. A network diagram with white nodes and lines is overlaid on a semi-transparent, stylized 'W' logo in shades of green and blue. A thick, reddish-brown curved line also arcs across the background.

Thank you
for your attention!

Time for questions...