SWTEST 2021 CONFERENCE

PROBE TODAY, FOR TOMORROW

30TH ANNIVERSARY

The Digital Revolution: NRZ to PAM4

FormFactor™

Daniel Bock, Ph.D.
David Raschko

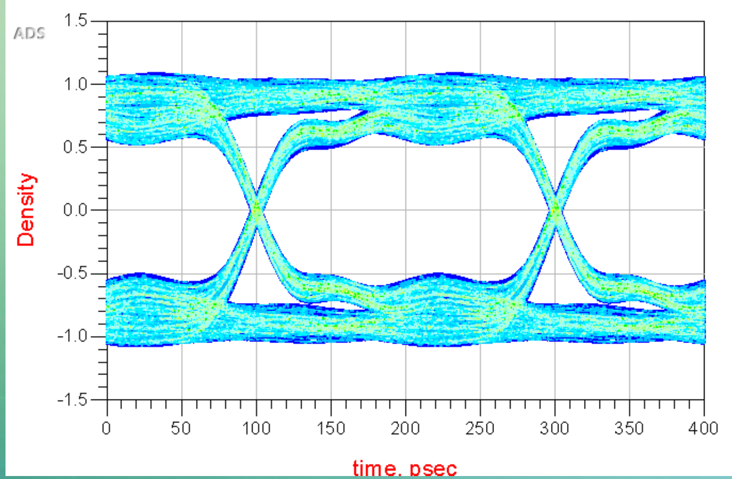
Aug. 30 – Sep. 1, 2021

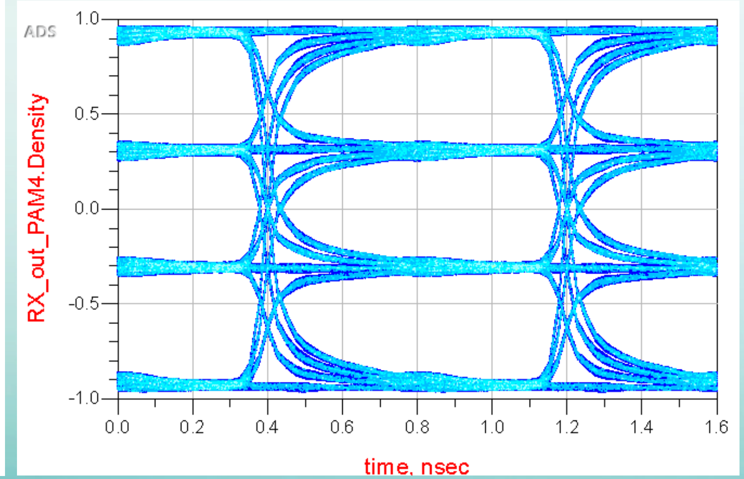
Agenda

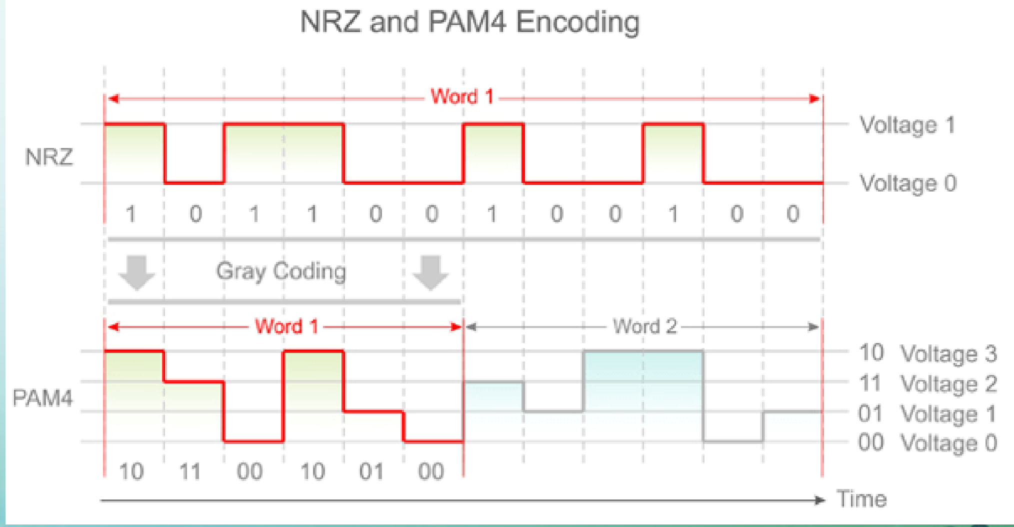
- **Introduction**
  - What is new with PAM4?
  - Why do we need PAM4?
  - What is the timeline for PAM4?
- **What is the Status Quo for Digital Test? (NRZ)**
  - What specs are important?
  - How are specs determined?
  - Sensitivity of NRZ to loss
- **What changes with PAM4 for Test?**
  - Sensitivity of PAM4 to loss
  - What specs are needed for PAM4?
- **How is Digital Test Managed?**
  - Testerization
  - Loopbacks
  - Loopback Taps
- **New FFI MEMS Probe and Summary**

What is PAM4?

- **Pulse Amplitude Modulation**
- **Digital encoding to create bitstreams**
  - Uses 4 Amplitude Levels to send 2 bits per Unit Interval
    - Effectively doubles the data rate without a change in clock speed

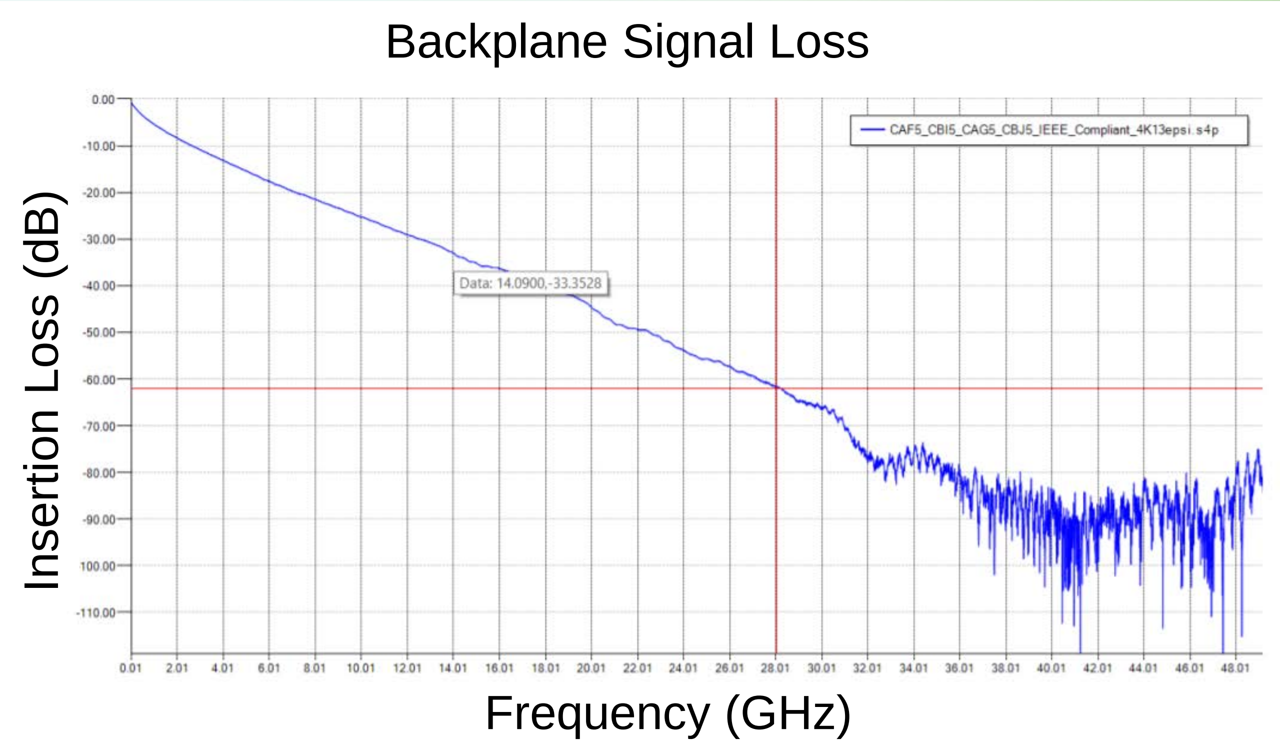






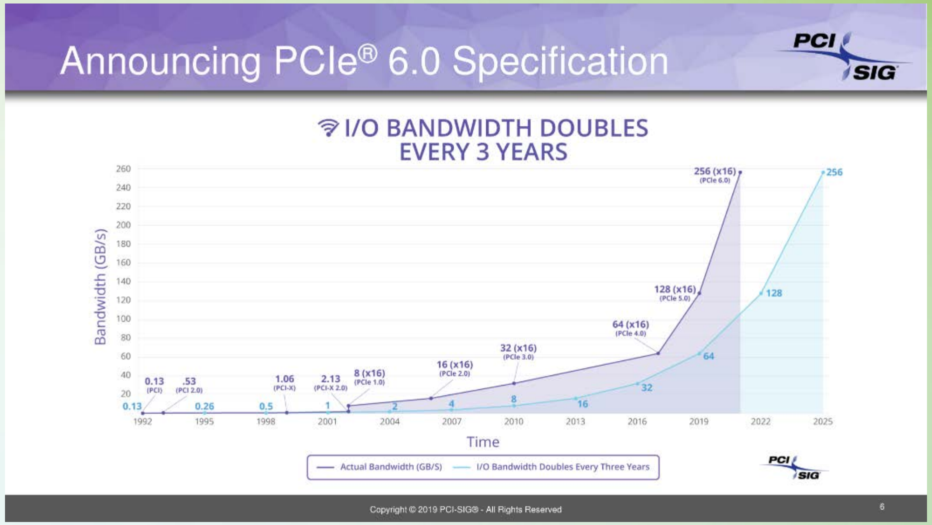
Why PAM4?

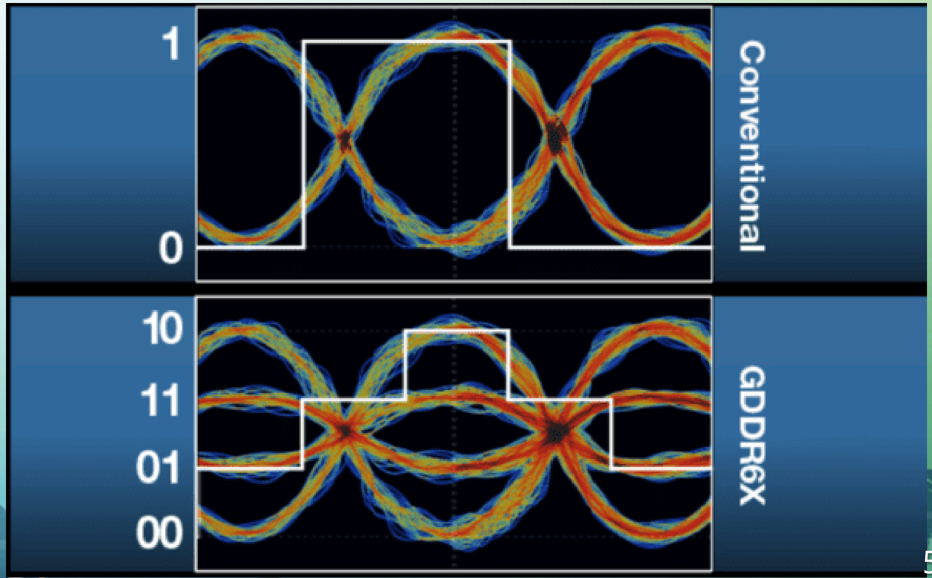
- **As speeds increase loss also increases**
- **PAM4 2x the data rate without increasing frequency**
- **PCIe as an example:**
  - Data rates double with each new standard
  - PCIe 5.0 = 32Gbps
  - PCIe 6.0 = 64Gbps
    - NRZ = 32GHz
    - PAM4 = 16GHz



When?

- **PCIe 6.0**
  - Next generation PCIe communication protocol
  - Standard released in Q4 2020
- **GDDR6X DRAM**
  - Memory interface that uses PAM4 in conjunction with high-end graphics cards
  - Q4 2020
  - https://www.edn.com/pam4-makes-it-to-memory-interfaces/



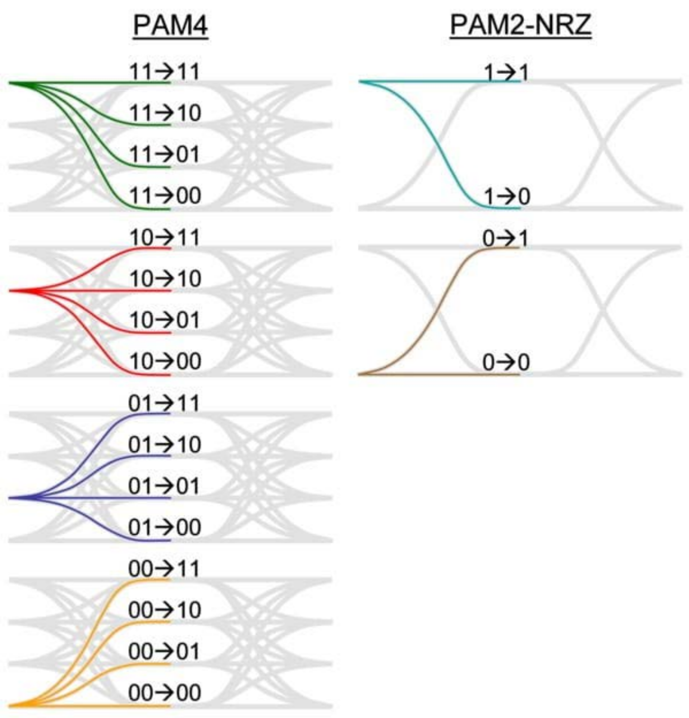


How Does PAM4 Affect Wafer Test?

- **Probe Card specs traditionally derived through the Nyquist frequency**
  - The Nyquist frequency is the maximum frequency f_{max} that can be measured with a system sampling at frequency f_{sample}
    - **$f_{sample} = 2 f_{max}$**
    - 15dB Return Loss
    - 3dB Insertion Loss
    - 20dB Crosstalk
  - For a 16 Gbps NRZ signal, the 3 dB point is 8 GHz using this short-hand
- **Do these specs work for PAM4?**

PAM4 Specifications?

- **The specifications for PAM4 require better performance than a NRZ signal operating at the same symbol rate**
- **That is due to:**
  - **The number of transitions is much higher**
  - **The dV between levels is much lower**



General Overview of Spec Differences

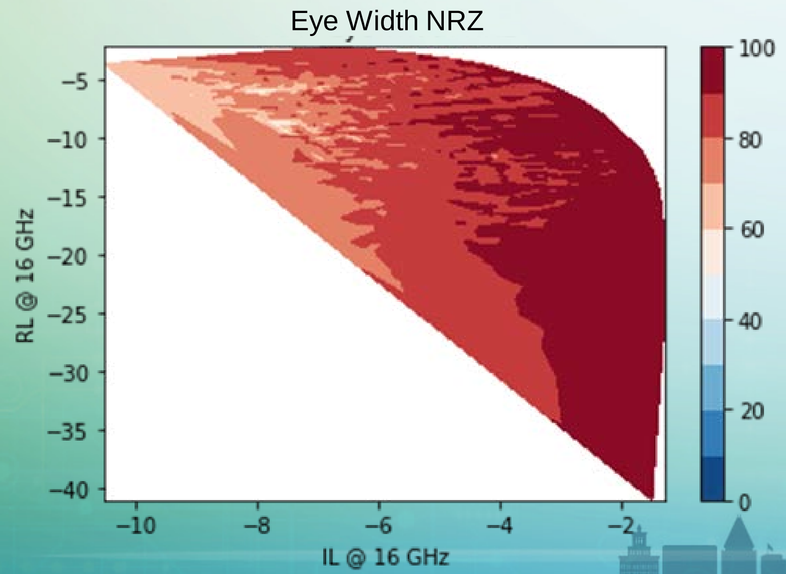
- **The differences lead to 'generic' differences in performance**
- **What do these generic differences require from the probe card?**

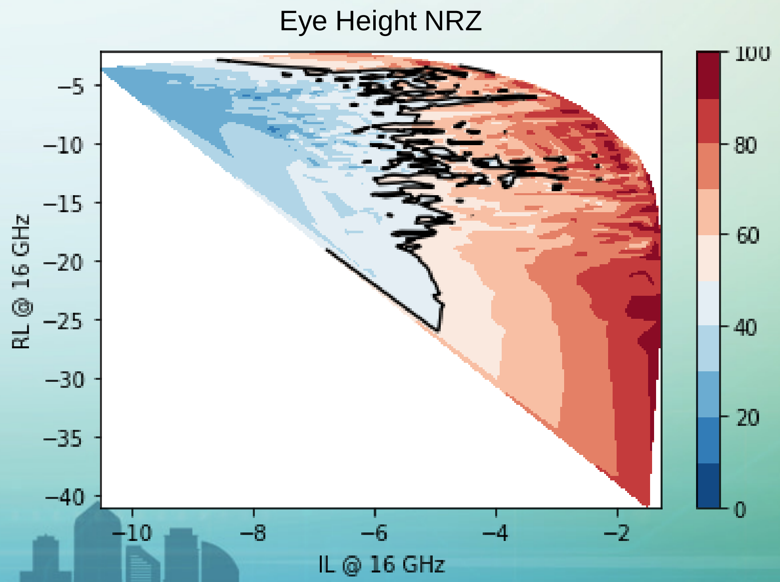
TABLE 1		
	NRZ	PAM4
Bits Per Symbol	1	2
Symbols	2	4
Eye Diagrams Per UI	1	3
Relative SNR Electrical	0 dB	9.5+ dB
Relative SNR Optical	0 dB	4.7+ dB
Distinct Transitions	2	12
Rising/Falling Edges	2	6
Average Transition Density	50%	75%
Skew and Compression	Absent	Present

https://www.signalintegrityjournal.com/articles/1151-pam4-for-better-and-worse

NRZ Loss Sensitivity

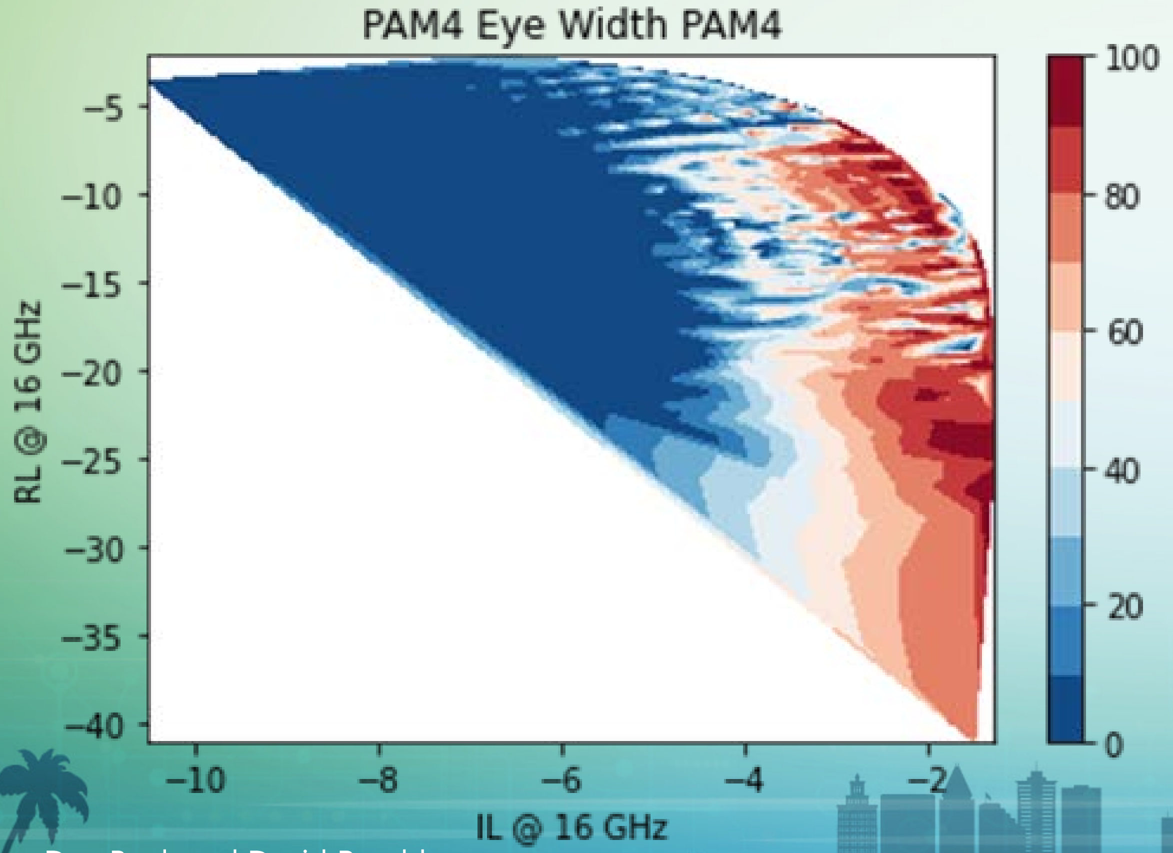
- **Sensitivity analysis exploring eye opening vs. Insertion Loss and Return Loss**
  - **NRZ overall performance appears to be dominated by the height, NOT WIDTH**
  - **At 16 GHz, if IL is < 5 dB, then the eye is larger than 50%**





PAM4 Loss Sensitivity (Width)

- **Sensitivity analysis exploring eye Width vs. Insertion Loss and Return Loss**

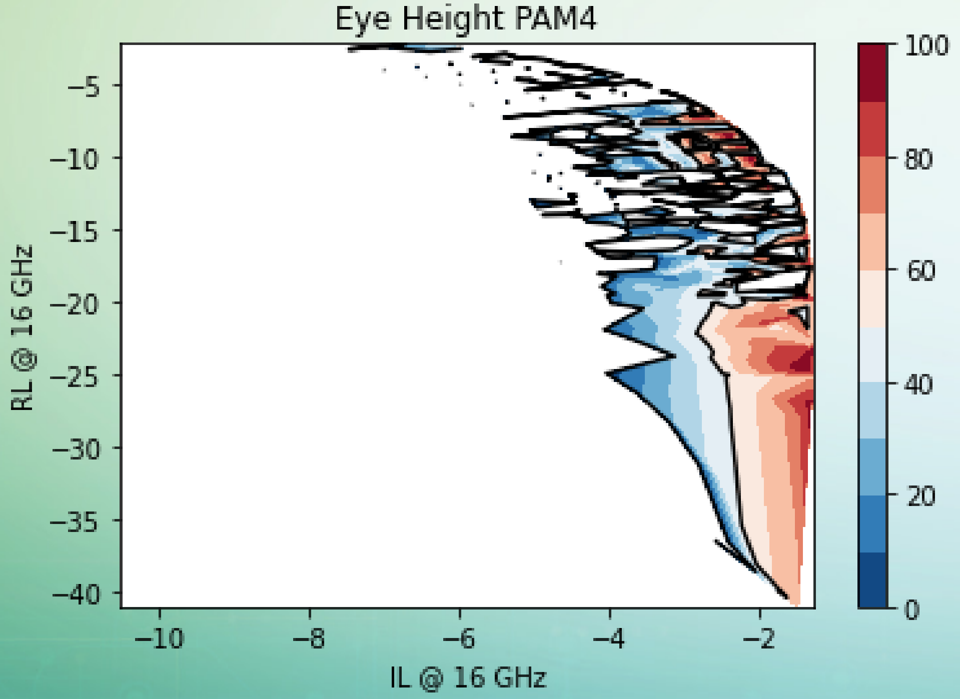


For a 50% eye width Insertion Loss must be better than -3 dB and Return Loss must be better than -10 dB at the Nyquist frequency

This represents a ~2x increase in probe card performance compared to NRZ

PAM4 Loss Sensitivity (Height)

- **Sensitivity analysis exploring eye Height vs. Insertion Loss and Return Loss**



For a 50% eye height Insertion Loss must be better than -3 dB and Return Loss must be better than -10 dB at the Nyquist frequency

The eye height appears to fall off a cliff much faster than the width

Comments on Eye Height and Width

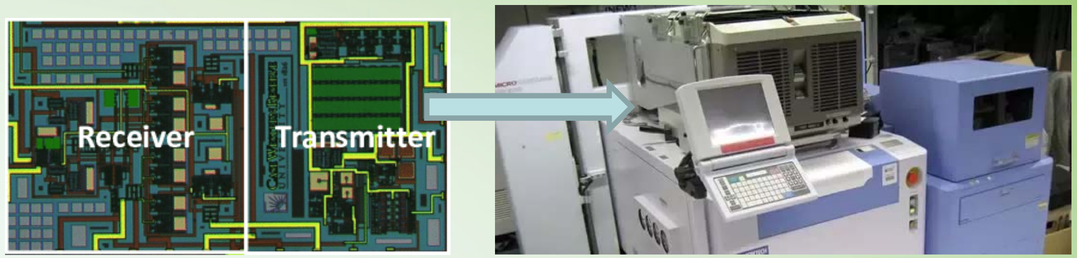
- **PAM4 and NRZ Probe Card Spec:**

Digital Protocol Type	Insertion Loss Spec	Return Loss Spec
NRZ	-5 dB	-10 dB
PAM4	-3 dB	-10 dB

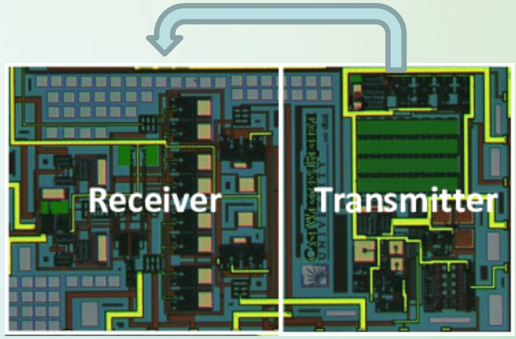
- **It appears that the eye height is more sensitive to performance than the width**
  - **Most likely since IL is known to be more important to the performance than RL**
  - **IL affects the height more than the width, and RL affects the width more than the height**

How is Digital Test Managed?

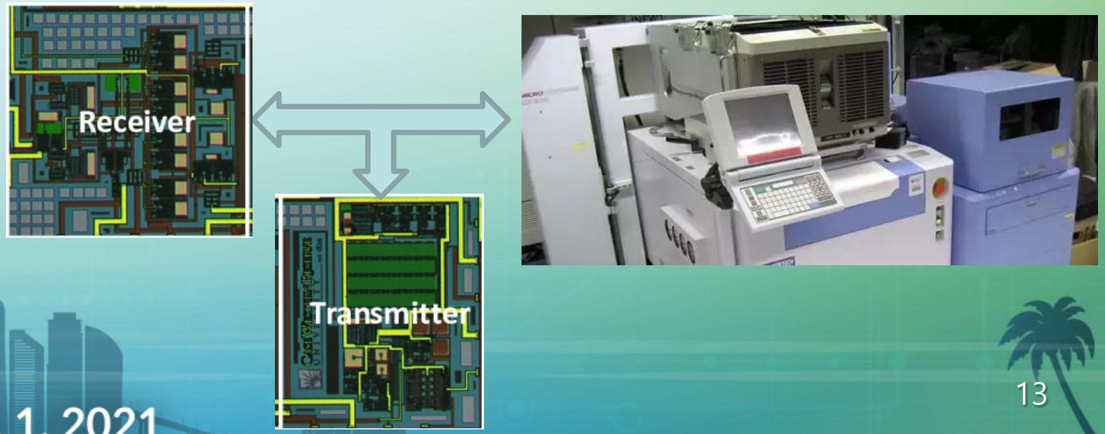
- **Testerization – Direct Connection to Tester Channel**
  - Probe -> MLO -> PCBA -> Tester Resource
    - MLO/PCBA Loss >> Probe Loss



- **Loopback Test – Signal goes from DUT TX to RX**
  - Probe -> MLO -> Probe
    - MLO/PCBA Loss = Probe Loss
    - Probe Loss is significant as it contributes to loss 2x in the signal path



- **Loopback Tap – Combination of high speed on loopback, and low speed on tester path**

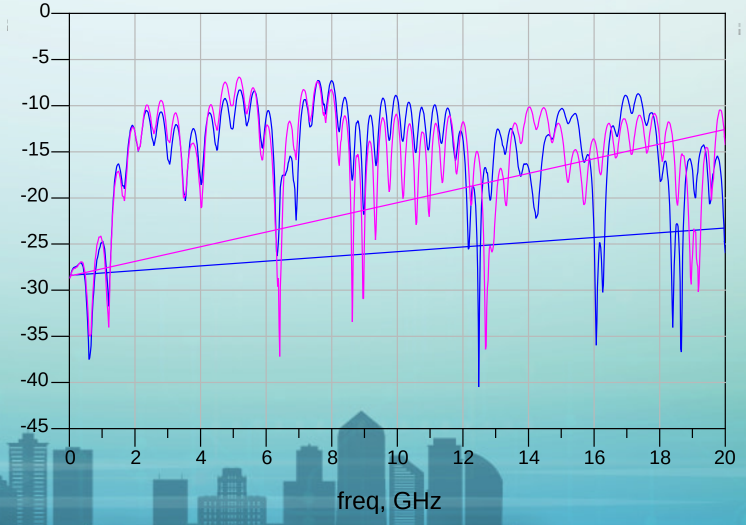


Testerization Performance

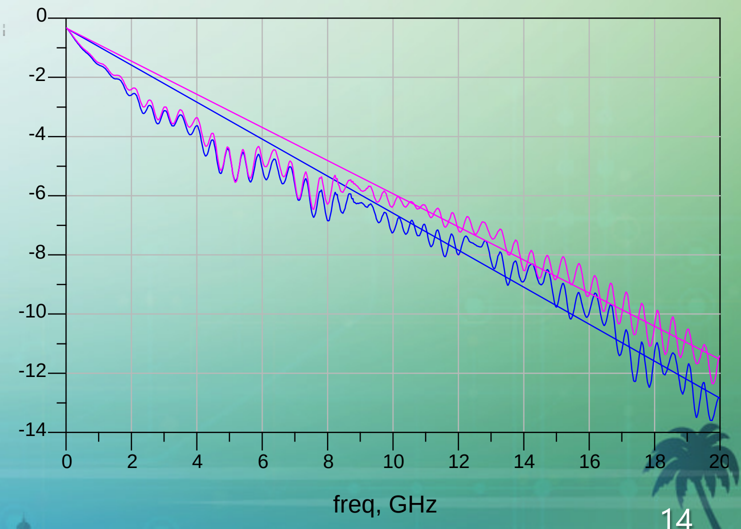
- **Testerization = Probe + MLO + PCBA to tester Resource**
  - MLO and PCBA Loss dominate the performance due to long path lengths
- **PAM4 ~10Gbps**
- **NRZ ~10 Gbps**

Pink = PCBA + MLO
Blue = PCBA + MLO + MEMS Probe

Insertion Loss

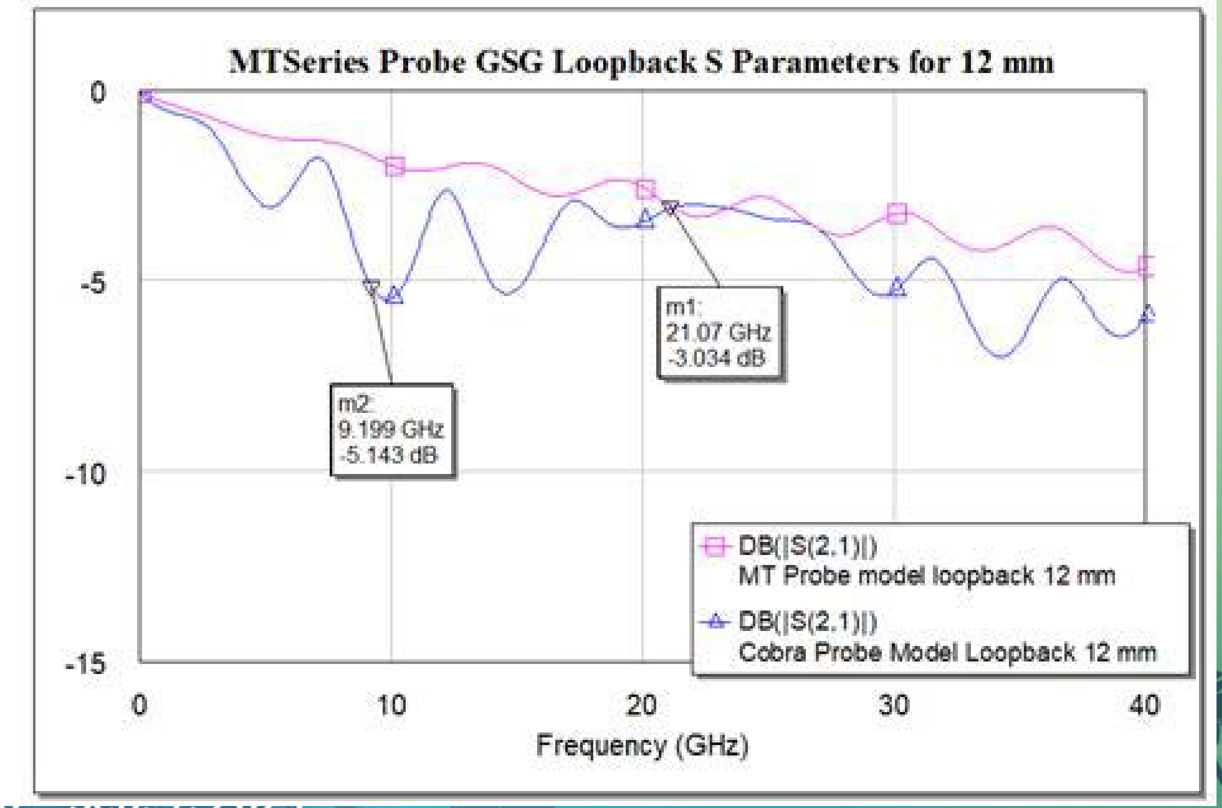


Return Loss



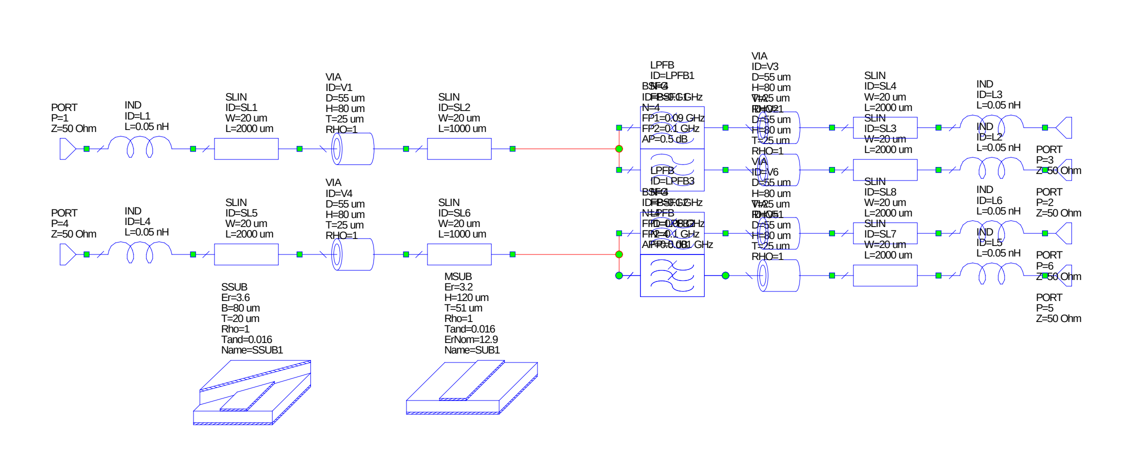
Loopback Performance

- **Loopback = Probe + MLO + Probe**
  - MLO Loss ~= Probe Loss
  - Performance gated by MLO length and probe loss
- **NRZ ~ 32Gbps**
- **PAM4 ~ 64Gbps**



Model for Loopback with Tap

- **The use of a tap to the tester comes from a worry about false positives**
  - Bringing a signal back to the tester ensures confidence in the test coverage.
- **The two channels to do not operate simultaneously**
  - One is for full speed PAM4 test, while the other is at a much lower speed
  - Low speed is at 100 Mbps
- **In order to separate the two channels, a filter was included to maintain performance**

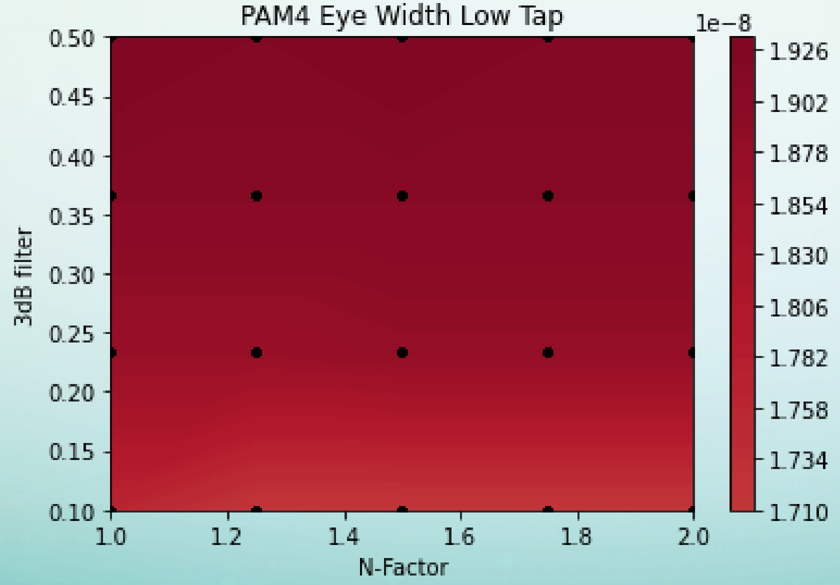


Model for Loopback with Tap

- Some of the factors that we looked at are:
  - What is the 3 dB point on the filter for the cross over between the two signal paths?
  - Should the 3 dB point of the high speed and low speed lines be the same? Should there be a factor (N-factor) separating them that can improve performance?

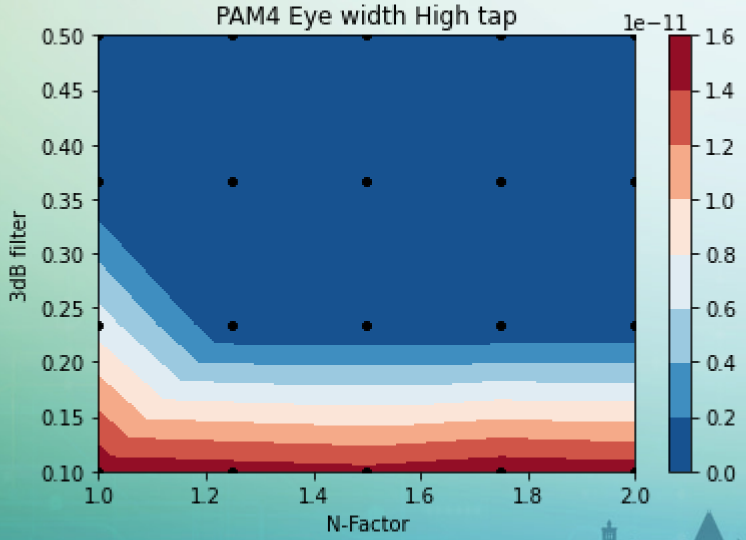
Low-Speed Side

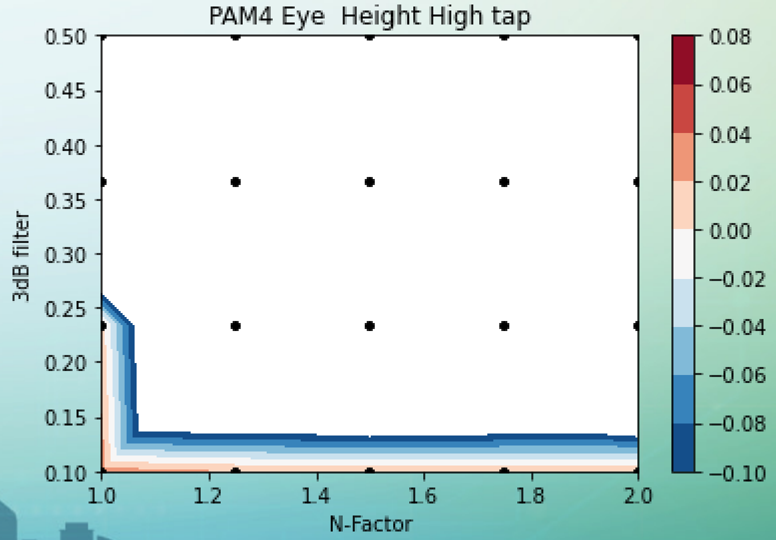
- **The low-speed side always has overall good performance, no matter on where the 3 dB point is, as well as the N-factor**



High-Speed Side

- **The high-speed side appeared to be much more sensitive to the N-factor, as well as the 3 dB point**
  - **The best performance was when N-factor = 1, and the 3 dB point stays close to 100 MHz (the frequency of the low-speed signal)**

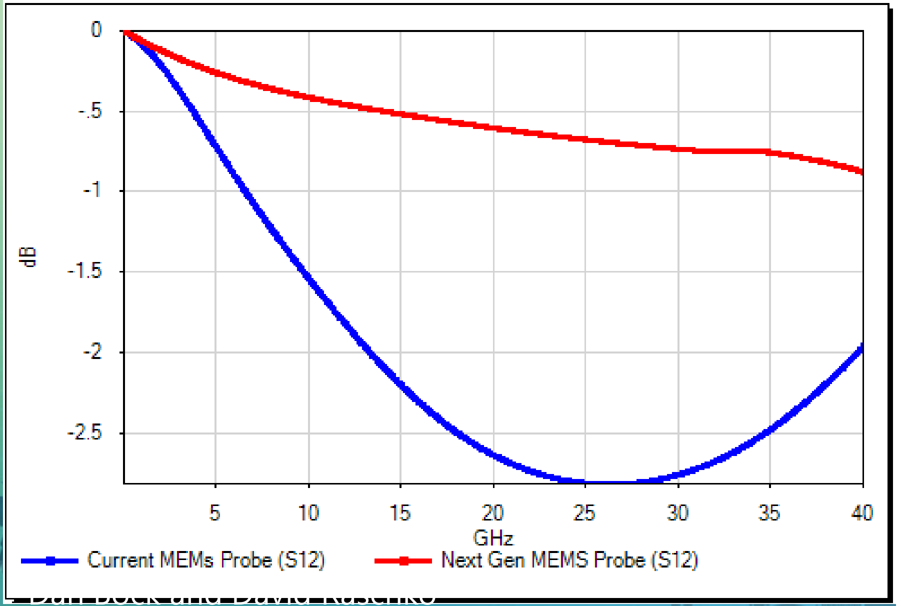




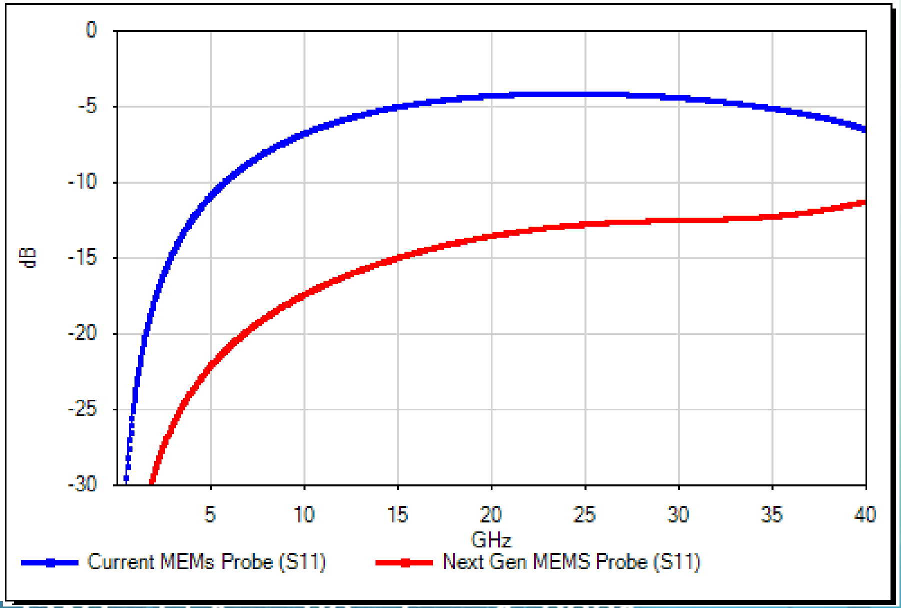
FFI Products

- **Next Gen MT Series MEMS probe for High-Speed Test**
  - Probe is 20% shorter for reduced inductance
    - >-0.5 dB Insertion Loss at 16GHz (PCIe 5/6)
    - <-15 dB Return Loss at 16 GHz (PCIe 5/6)
  - MT Series Probe Available for Evaluation by the end of 2021

Insertion Loss



Return Loss



Current MEMS Probe meets requirements for PCIe 3 and PCIe 4

Test Summary

- **PAM-4 specs will need to be tighter compared to NRZ:**

Digital Protocol Type	Insertion Loss Spec	Return Loss Spec
NRZ	-5 dB	-10 dB
PAM4	-3 dB	-10 dB

- **Testerization has problems with path length loss limiting performance to ~10Gbps**
- **MLO Loopbacks have significantly lower loss, but the probe begins to become the dominate loss factor**
- **Loopback taps require that the filter between the two sides have the same 3 dB point, as well as keep it as close to the maximum frequency of the low-speed test**

Conclusion

- **The requirements for PAM4 vs NRZ indicate that probe card specifications should be more stringent than that for NRZ probe cards**
- **Loopbacks with a tap to the tester is possible, but require care in design, as well as full speed test to tester is not going to be possible most of the time**
- **FFI Products are ready for the challenges being presented by the move to PAM4 with custom solutions**