Aug 2021

Qualcomm

The Future Growth and Challenges of Semiconductors From Fab to Test to Hardware

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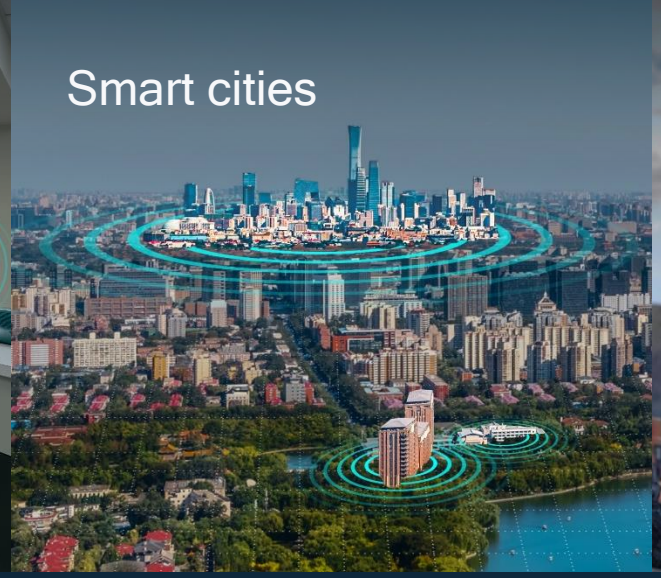
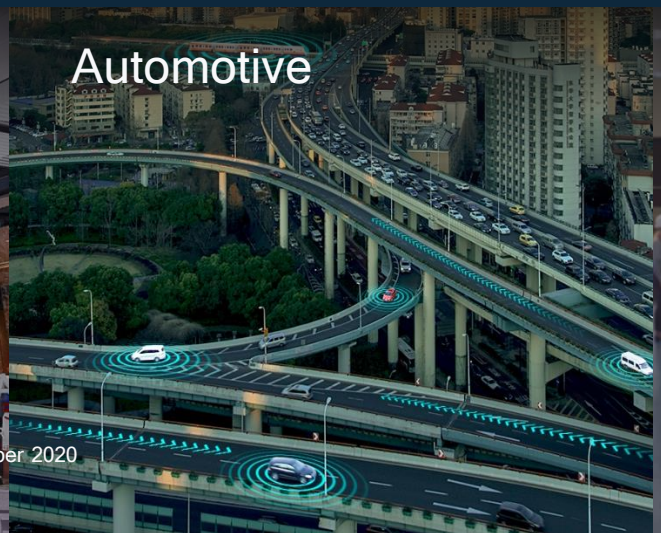
VP Engineering
Qualcomm Technolgies, Inc.


Intelligent
Connected
Mobile
Highly integrated

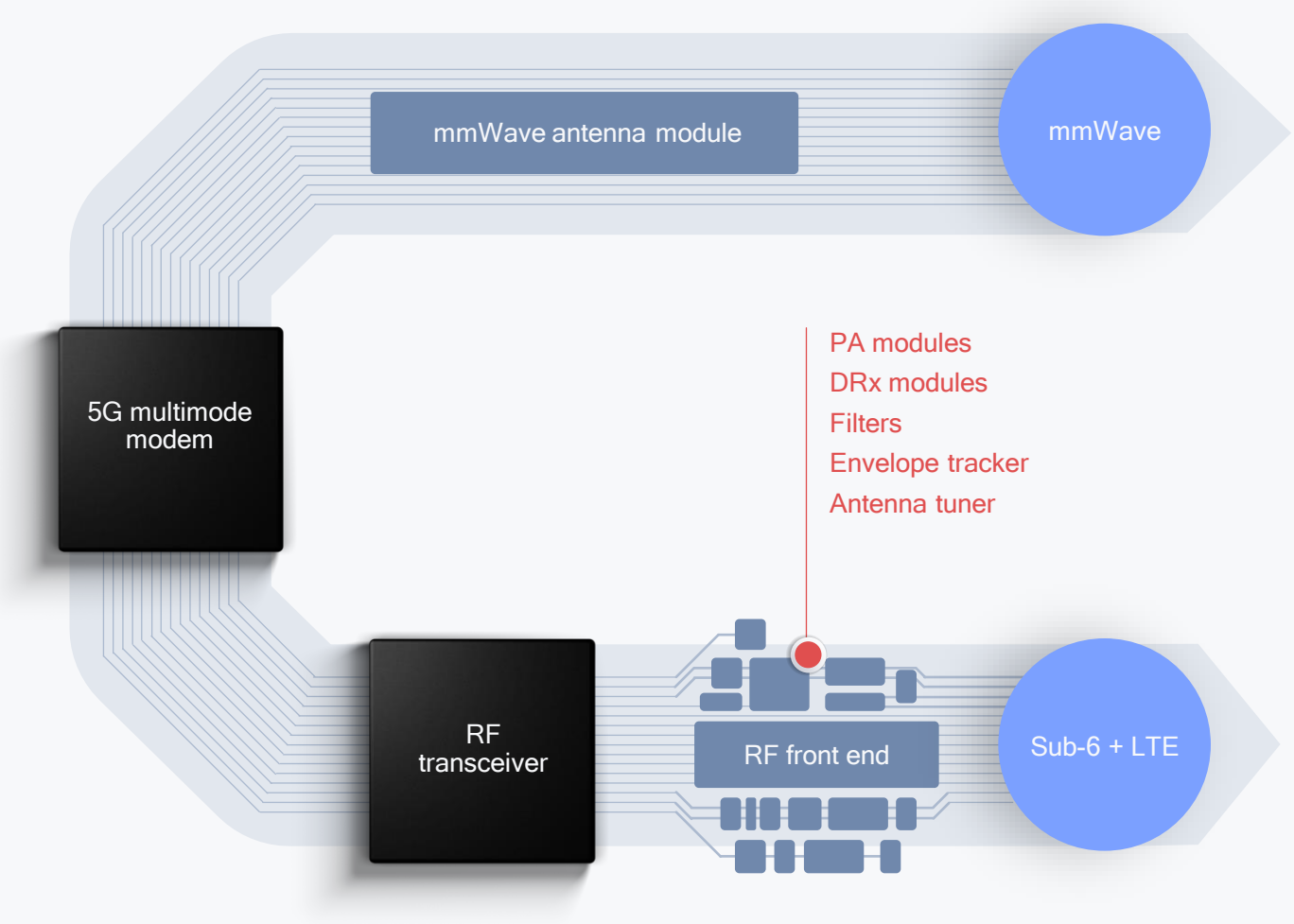


Driving more than a decade of digital transformation

More than $13 trillion in economic activity enabled by 5G in 2035

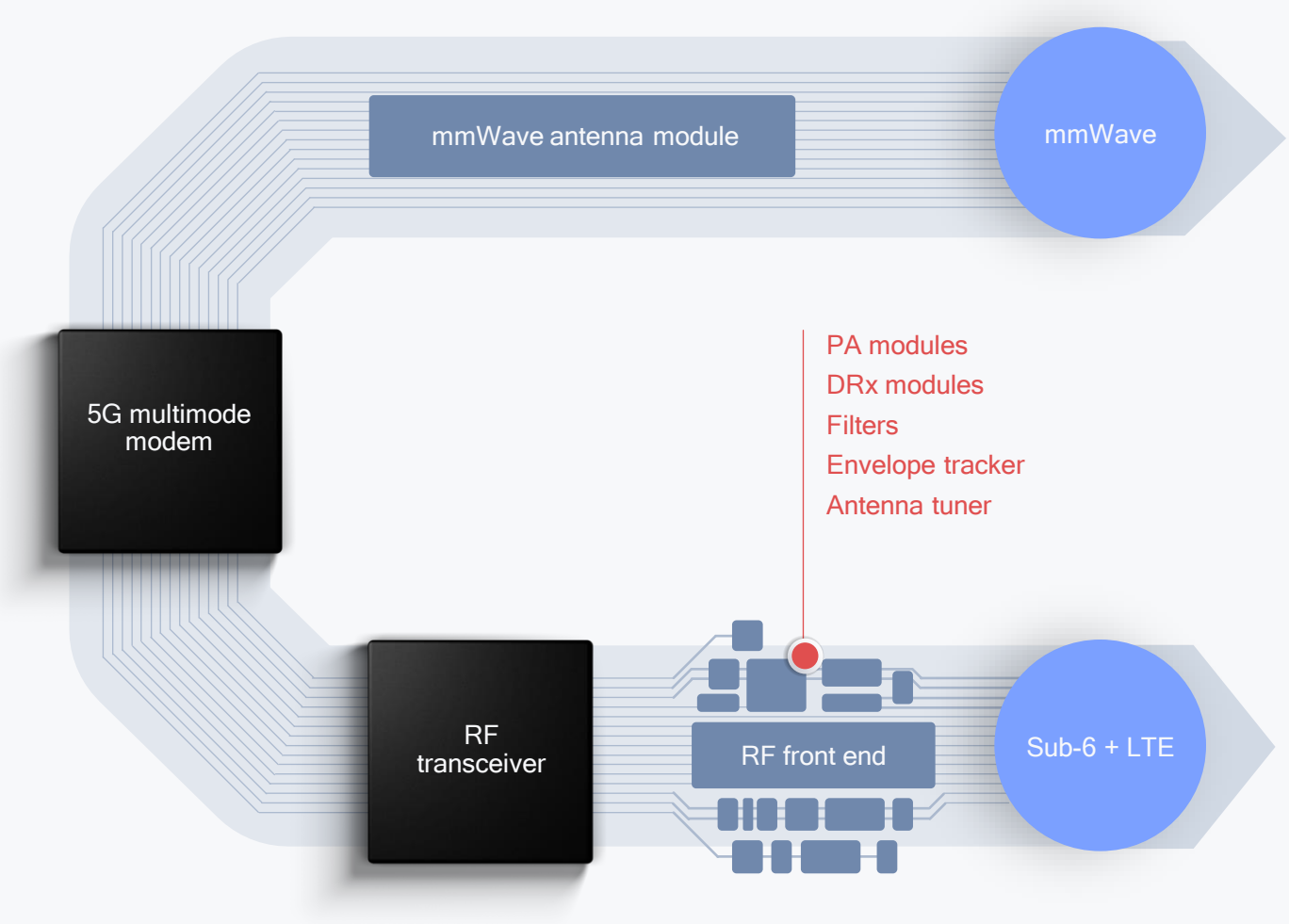


Source: The 5G Economy, an independent study from IHS Markit, commissioned by Qualcomm Technologies, Inc., November 2020



5G demands complex integration

- Increased performance
- Lower power
- Improved thermal performance
- Smaller form factors
- Faster time-to-launch



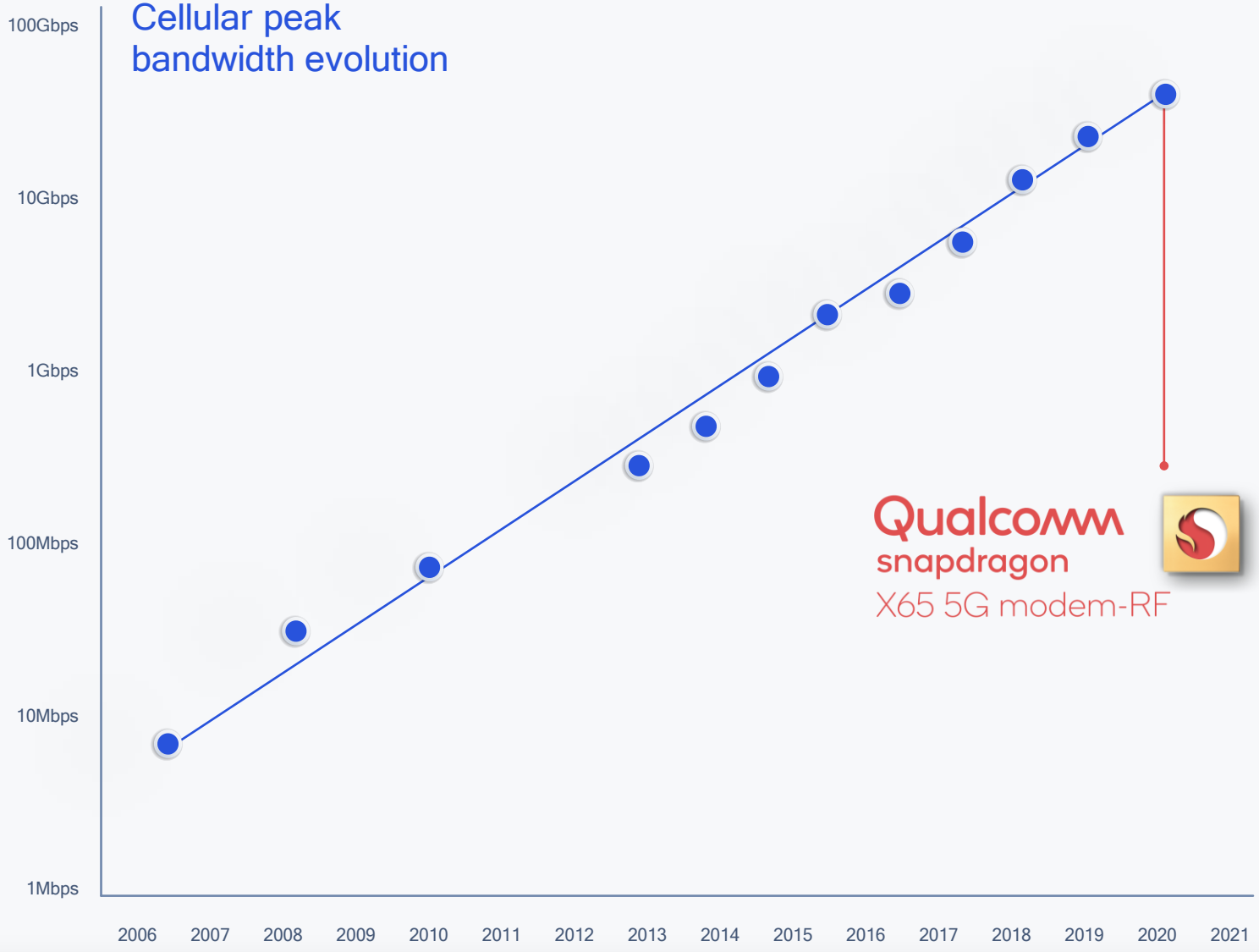
Building a modem-RF system

100+ active and passive ICs

Performance a strong function of integration architecture

Wide range of semi-technologies

- 3/4/5nm CMOS
- 0.15nm PMIC
- Fin-Fet RF
- RF SOI



Sustained innovation is driving cellular performance

Snapdragon
5G Modem-RF Systems
are realizing Edholm's Law

Source: ABI Research, QTR2 2021

Mobile technology powers edge devices across industries

5G enables AI to reach its full potential

Mobile handsets

RF front end

Wireless infrastructure and networking

Auto

Voice and music Wearables

IoT

Mobile broadband (Fixed wireless access)

Mobile compute

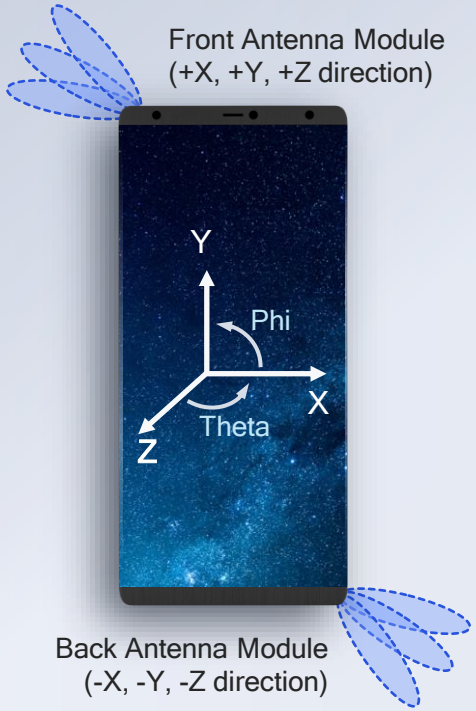
XR

RAN processors and RFFE

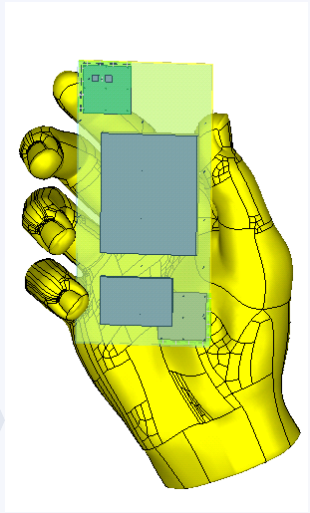
Cloud/edge AI inference

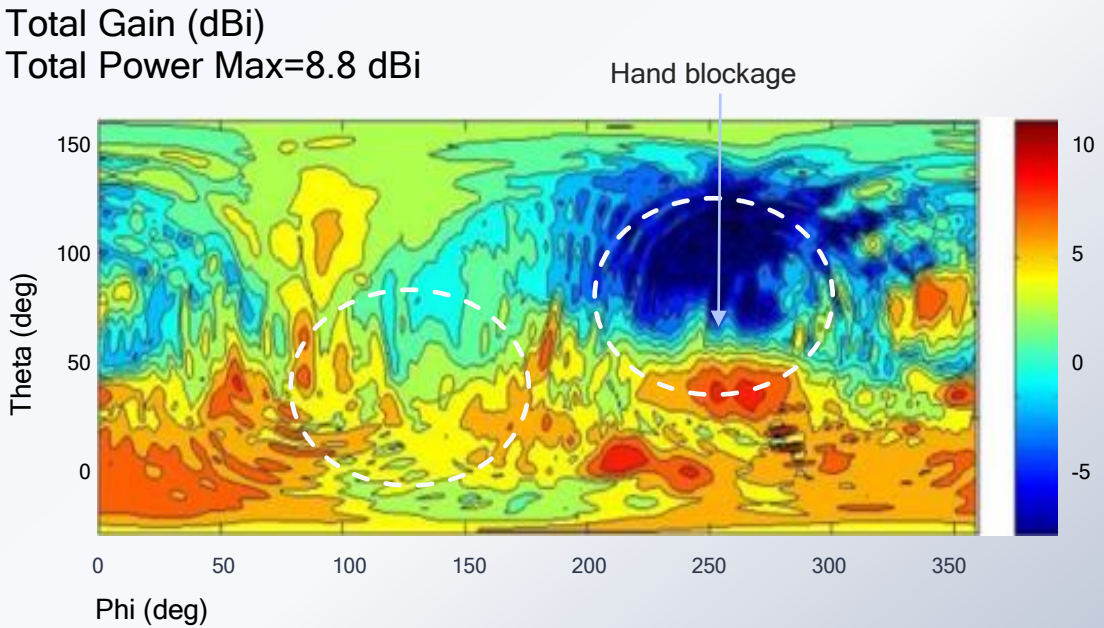
A significant opportunity ahead

Improving reliability utilizing device antenna diversity



Provides nearly spherical coverage in free space





Qualcomm Research Simulations

Mitigates hand-blocking and reduces impact of random user orientation

Results drove commercial products – Qualcomm® QTM052 5G NR mmWave antenna module

Source: Qualcomm Technologies data

Accelerating the future of

automotive

Over 100 million vehicles using Qualcomm® Automotive solutions

5G

Accelerating globally

165+
Operators with 5G commercially deployed

270+
Additional operators investing in 5G

500M
5G smartphones to ship in 2021

750M+
5G smartphones to ship in 2022

1B+
5G connections by 2023 – 2 years faster than 4G

3.8B
5G smartphones to ship between 2020-2024

Sources – 5G commercial networks and operators investing in 5G: GSA, Jun 2021. 5G device shipment projections: Qualcomm estimates, Feb 2021. 2023 5G connection projections – average of average of ABI, Jun 2020; Ericsson, Jun2020; and GSMA Intelligence, Aug 2020. Cumulative 5G smartphone shipments: avg of CCS Insight (Sep/Nov 2020), CounterPoint Research (Dec 2020/Jan 2021), IDC (Nov 2020), Strategy Analytics (Dec 2020/Jan 2021).

Advancing high-performance, low-power computing

Requires leading edge technology and continued process innovation AND TEST INNOVATION

Premium tier smartphones

Automotive central compute architecture

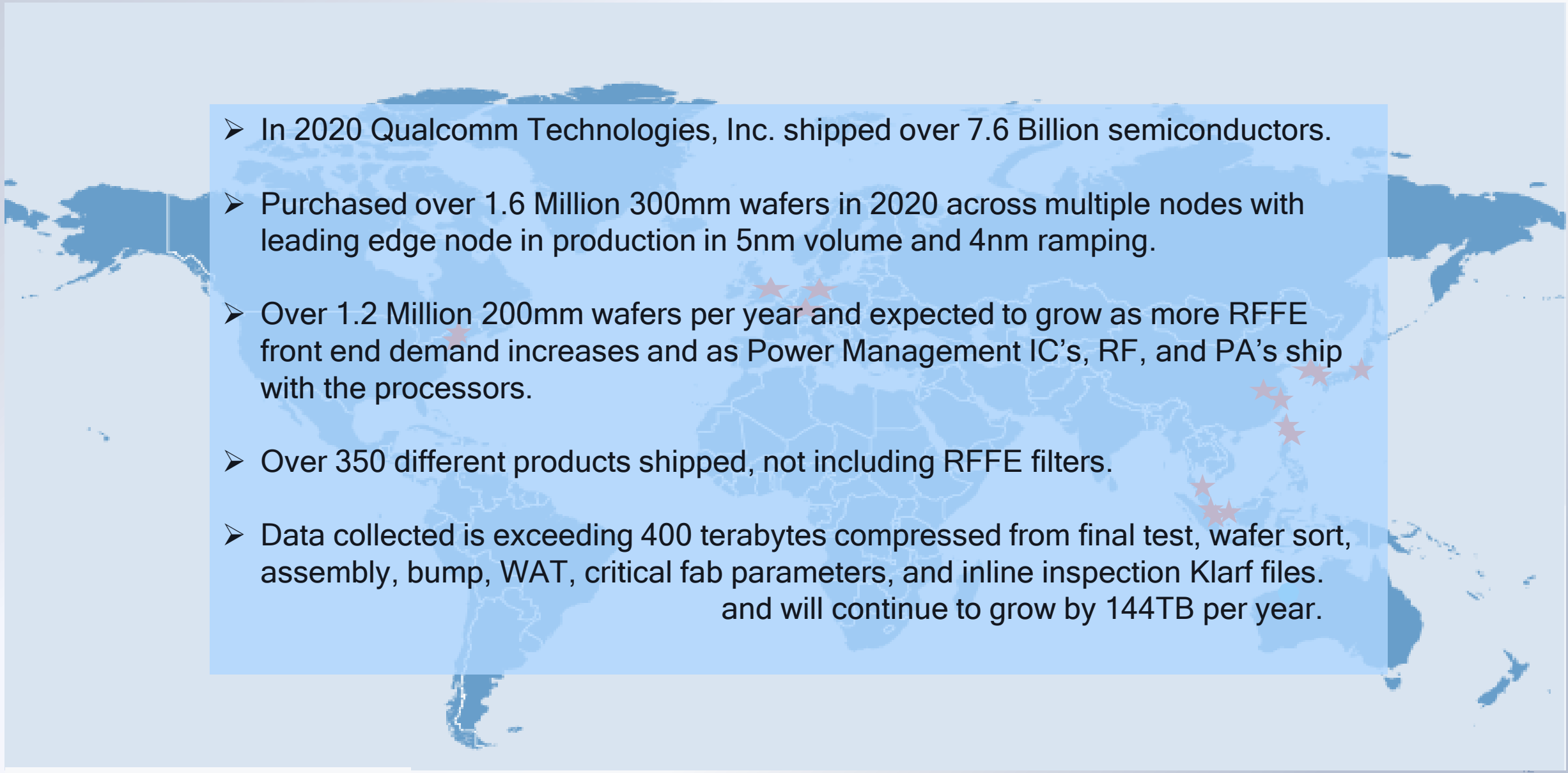
Extended reality

Always On, Always Connected PC

Continuing to scale performance, power, and area

Supporting new silicon partitions | High-performance computing

Qualcomm suppliers from across the globe to meet our demands



- In 2020 Qualcomm Technologies, Inc. shipped over 7.6 Billion semiconductors.
- Purchased over 1.6 Million 300mm wafers in 2020 across multiple nodes with leading edge node in production in 5nm volume and 4nm ramping.
- Over 1.2 Million 200mm wafers per year and expected to grow as more RFFE front end demand increases and as Power Management IC's, RF, and PA's ship with the processors.
- Over 350 different products shipped, not including RFFE filters.
- Data collected is exceeding 400 terabytes compressed from final test, wafer sort, assembly, bump, WAT, critical fab parameters, and inline inspection Klarf files. and will continue to grow by 144TB per year.

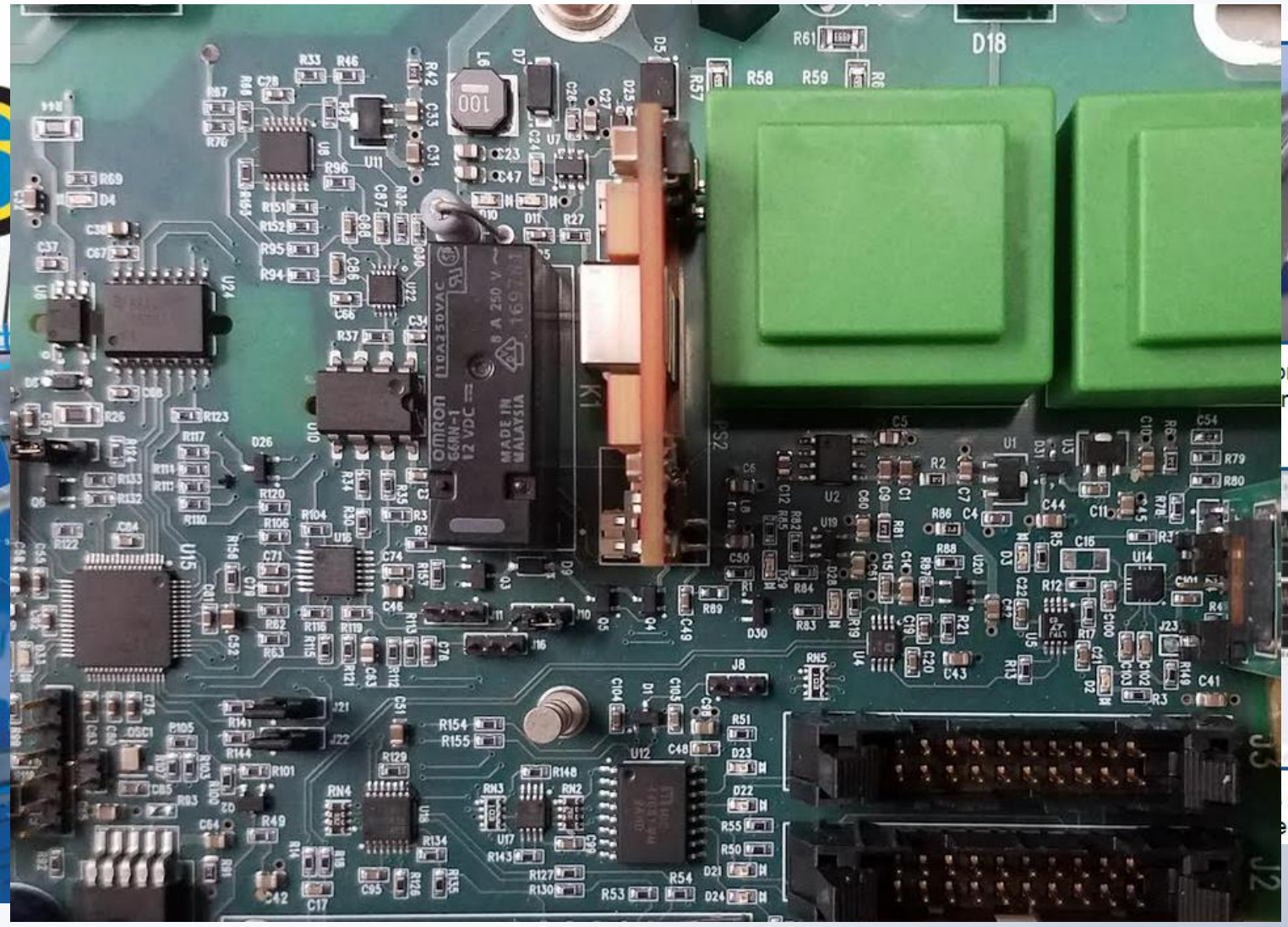
Source: Qualcomm Technologies data

The Semiconductor Shortage Affecting Many Sectors

Testers: Average 2-3 months Lead Time have increased to 6-8 months… and increasing

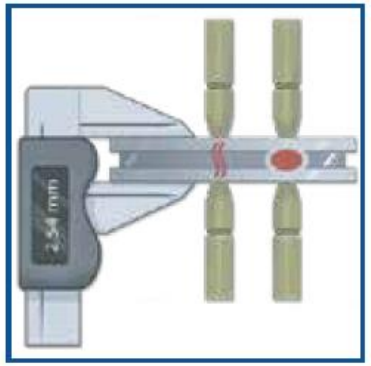
Components: Average of couple of months increased to 12+ months for certain components.

Even sectors you would not think would be affected ARE: Such as Spot Welders



Audio & Video Playback

For

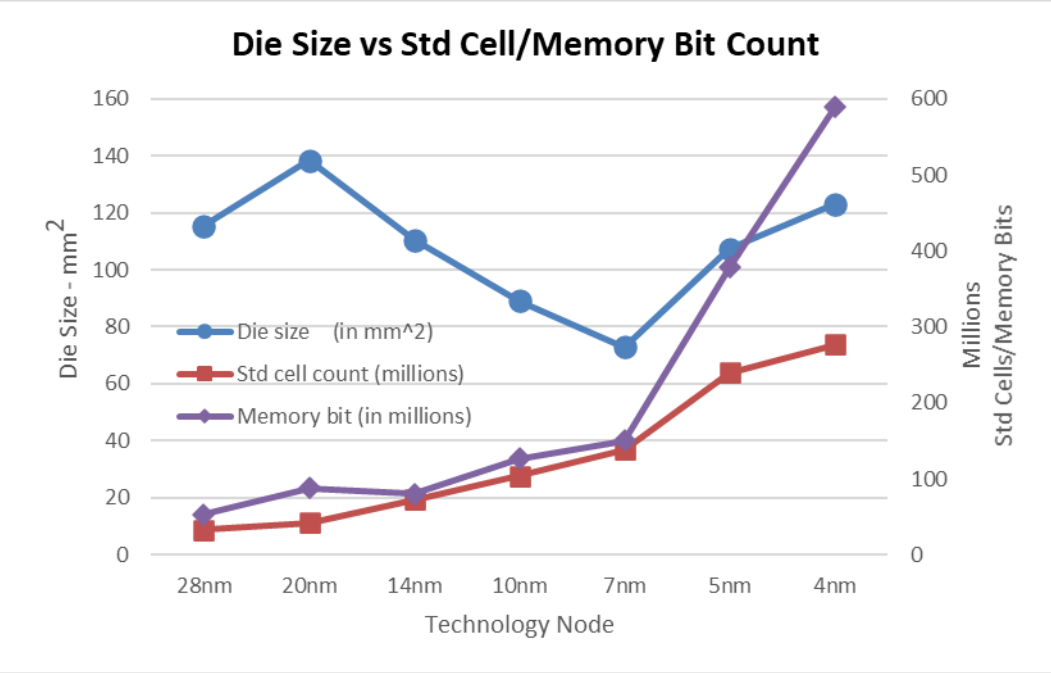


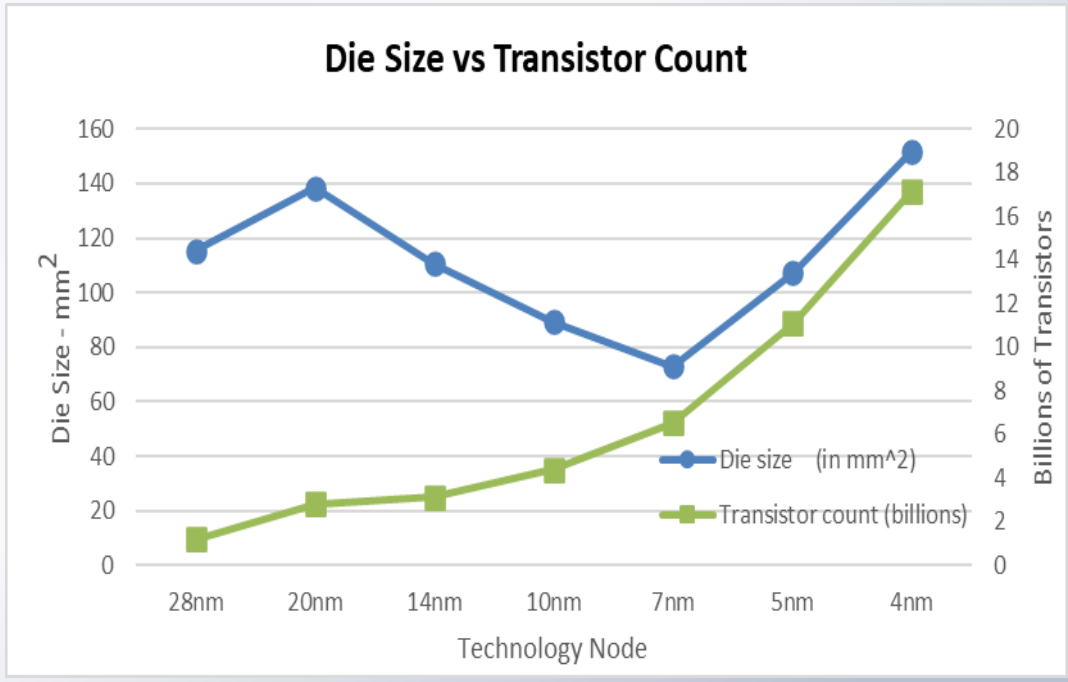
Auto Weld

By Permission from President
Pro Spot International, Inc.

Technology Migration has Enabled Snapdragon Capabilities.

- Die size decreased over 45% thru 7nm but is now increasing back similar to 20nm
- The number of transistors has increased over ~12x from 28nm and 2x from 7nm
  - Additionally, the standard cell and Memory Bits have increased ~ 8-11x
  - Giving higher performance and lower power…..
- However, the trend of growing die size / and content is not slowing, even with EUV and with significant challenges to yield and to contain power.





Source: Qualcomm Technologies, Inc.

Industry demands are driving more capability and faster Time to Commercialization.

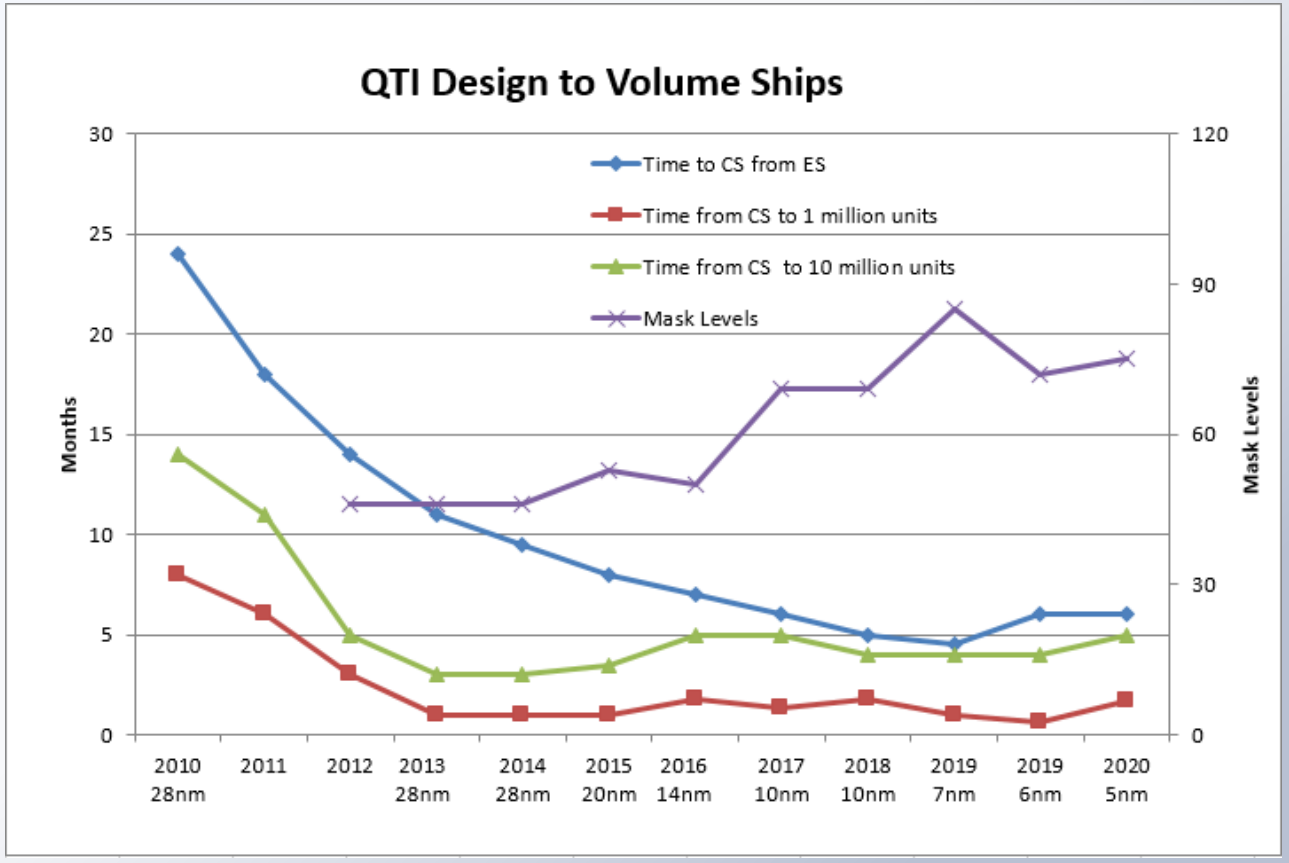
- As a result the QTI model continues to adopt to the changing industry requirements.
  - QTI is at the leading edge of technology with our foundries/osats to meet the insatiable need of the market:

Always connected, Best Graphics, Multi Camera/Video, GPS, and the Latest App, etc

…… and of course the Longest battery life

This forces faster time to YIELD !!
And Quality.

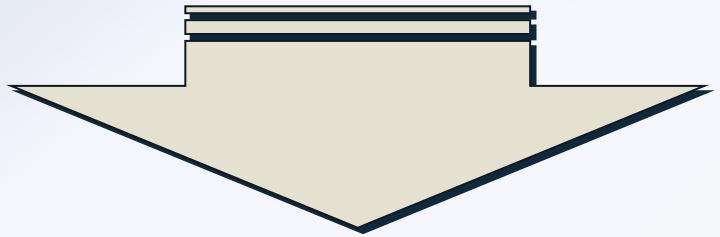
Much more difficult when on the leading edge of a technology introduction which QTI has done on 20nm, 14nm, 10nm, 7nm, 5nm and now 4nm.



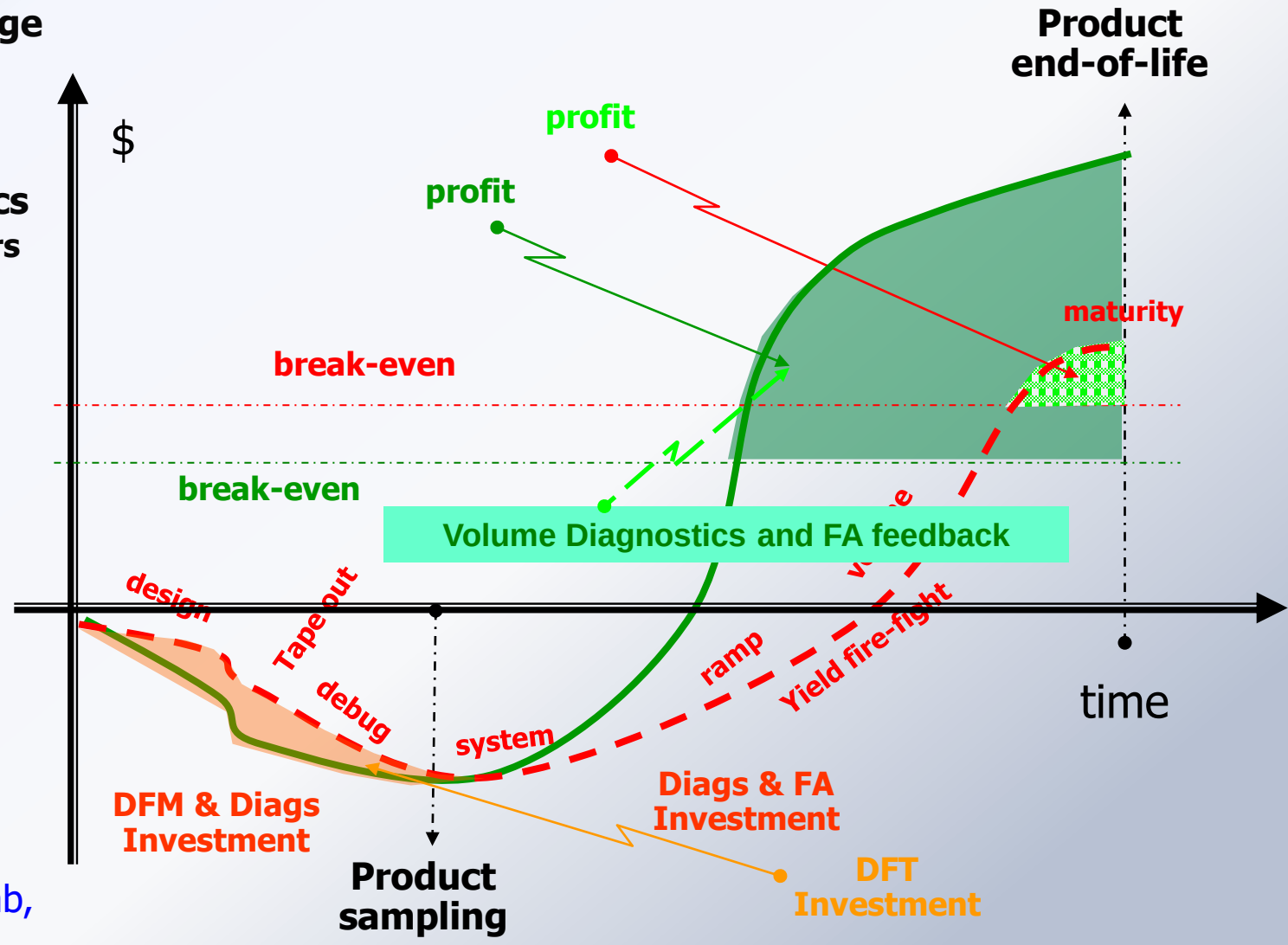
Source: Qualcomm Technologies data

Business Need- Rapid & predictable yield learning to increase profit

- **Return on design & development investment comes when there is volume shipments.**
- **Time to yield, especially on new "leading edge nodes, is critical to recover investments.**
- **DFM, DFT, advanced Diagnostics are investments to accelerate yield learning.**
- **Further Acceleration thru Volume Diagnostics**
  - **Diagnostics enables FA of critical yield limiters and enables faster learning.**
  - **Decreases the total investment and Shortens the investment period**
  - **Increases and Prolongs the return period**



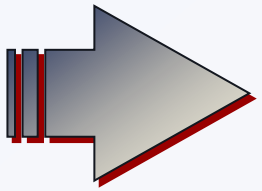
- **Faster Yield Learning via DFT/DFM/Volume Diag's Goes Straight to the Bottom Line**
  - Anything that can be done to accelerate and improve yields faster/sooner is good for the business
  - Requires tight collaboration and sharing w/Fab, Design, ATE, Assembly and now Sys. Test

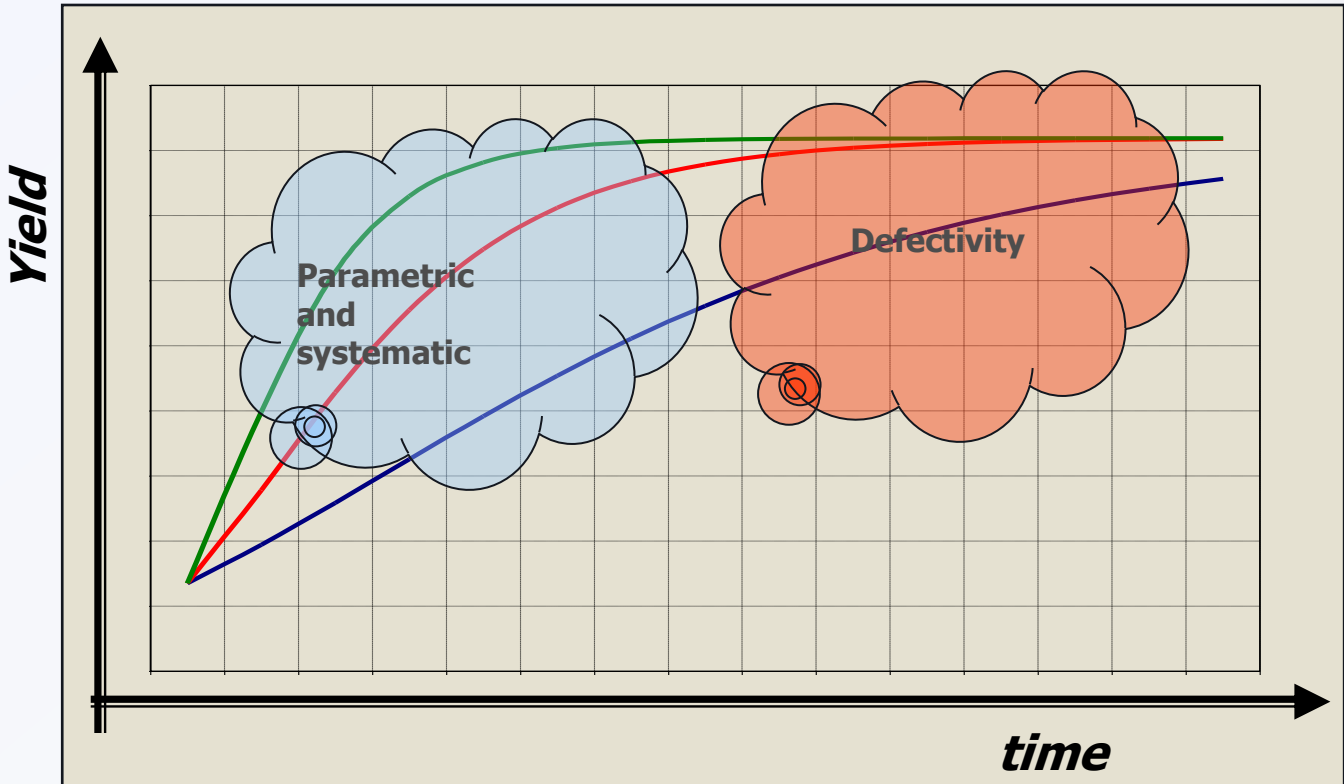


Source: Qualcomm Technologies data

Yield Distribution & Process Maturity

- Yield vs Process Maturity
  - Yield Learning Rate is critical
  - Test is crucial to understand yield drivers.
  - Yield learning rate models are required for optimized design.
- Ramp Dominated by Defectivity and Process-Design Interactions
  - Failures - Design, Process, Both???
  - Systematic & Parametric Issues
  - Design & Process Tuning
  - Test Diagnostics and FA drive FAB/Design fixes.
- Mature Yield Dominated by Process Defectivity
  - Dirt, equipment, materials or equipment limitations
- Much more Testing and Test data required.
  - Collect volume fail data.
  - Requires much more Continue On Fail Testing (COF)
  - Which Drives Diagnostic, FA, and Correct Actions





Yield learning acceleration is a competitive advantage.

We are partnering with our foundries to drive high yield learning rates and the lowest possible DD.

Today's Data Set has Higher *Usable* Dimensionality

New Set of Parameters Available Enable Strong Signals

Aggregated Attributes
- Failure Analysis
- Customer Returns
- Quality Excursions
- Design

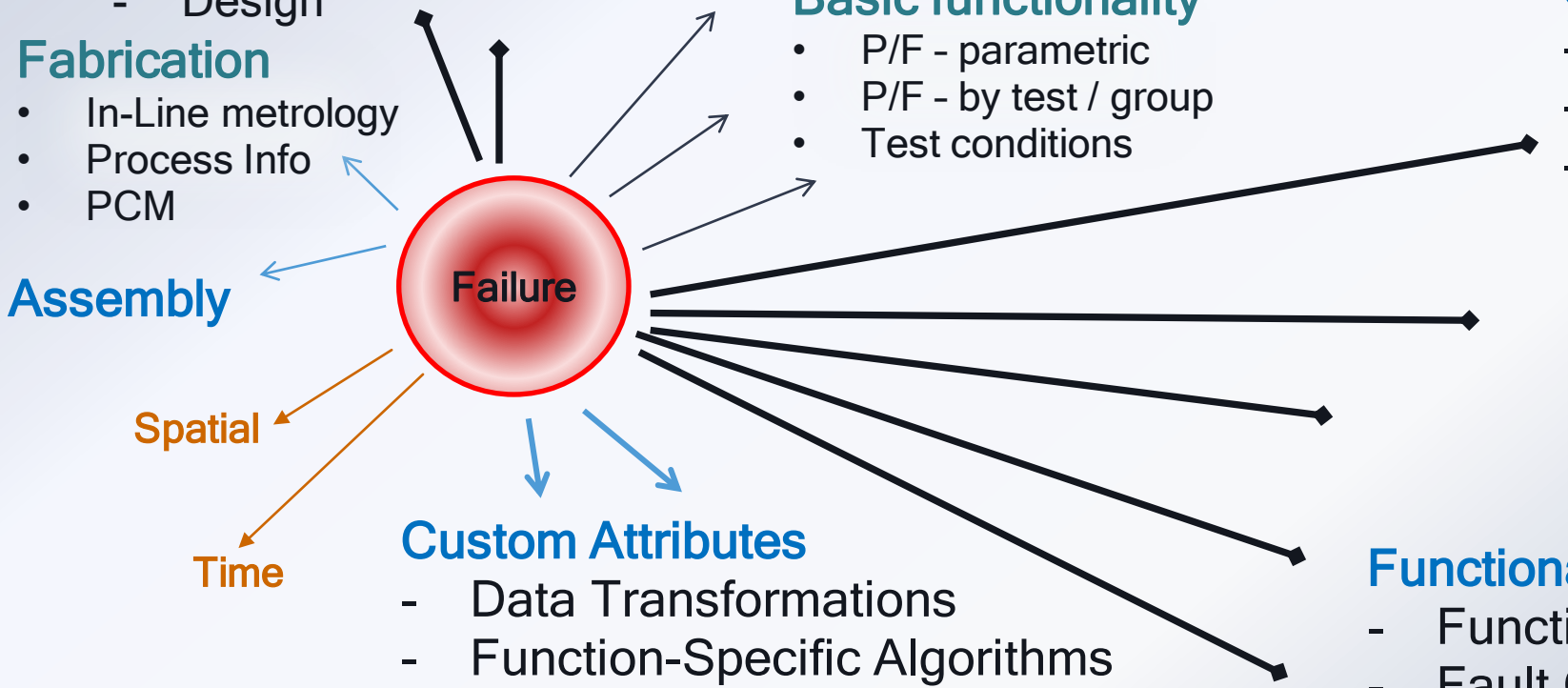
Design
- All timing paths
- Hold, capture , skew
- PVT corners

Enhanced Test Data - all Test Operations
- Test Attributes of all Test
- Test Attributes of both Good & Bad Device

Fabrication
- In-Line metrology
- Process Info
- PCM

Basic functionality
- P/F - parametric
- P/F - by test / group
- Test conditions

Structural Attributes
- Slack, Set-up, Hold
- Fault Type
- Domain Classification



Physical Attributes
- Topology
- Layout

Custom Attributes
- Data Transformations
- Function-Specific Algorithms

Functional Attributes
- Functional Classification
- Fault Coverage

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Source: Qualcomm Technologies data

ATE Evolution & Challenges

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Basic Functionality

- Pass/Fail
- IDDQ
- Voltage/Power
- Frequency

Single Insertion

Datalogs in KB

Single Site - X1

VM in KBs

Data Generator & Throughput

- Wafer-Level
- Package-Level
- System-Level/Func.
- Down-Binning
- Shmoo
- Freq. Response
- Calibrations
- Fuses (up to 1M)
- Hard Bin
- Soft Bin
- X, Y
- Test Site
- DFT via HSIO
- Pass/Fail
- IDDQ
- ATPG Core Based
- SAF, TDF, PDF
- Cell Aware
- Voltage/Power
- Frequency
- Current
- Profile over time
- Temp. Sensor
- Ring Oscillator
- HW ID
- Test Cell ID

Multiple Insertions: Cold, Hot, Room, etc.

Enhanced Diagnostics = Datalogs in GB

Higher Multi-Site

VM in 100s of MB and up to GBs

Innovation needed

ML-Based Analytics
- Outlier Detection
- Clustering
- Classifications
- Regressions
- Adaptive Testing
- Self Trained Models
- Abnormal Behavior

ATE Development
- Auto Test Program generation
- M: Adaptive coverage
- Native Machine learning

EDA Integration
- Adaptive Coverage
- Automatic test coverage generation
- Bi-directional Scan chains

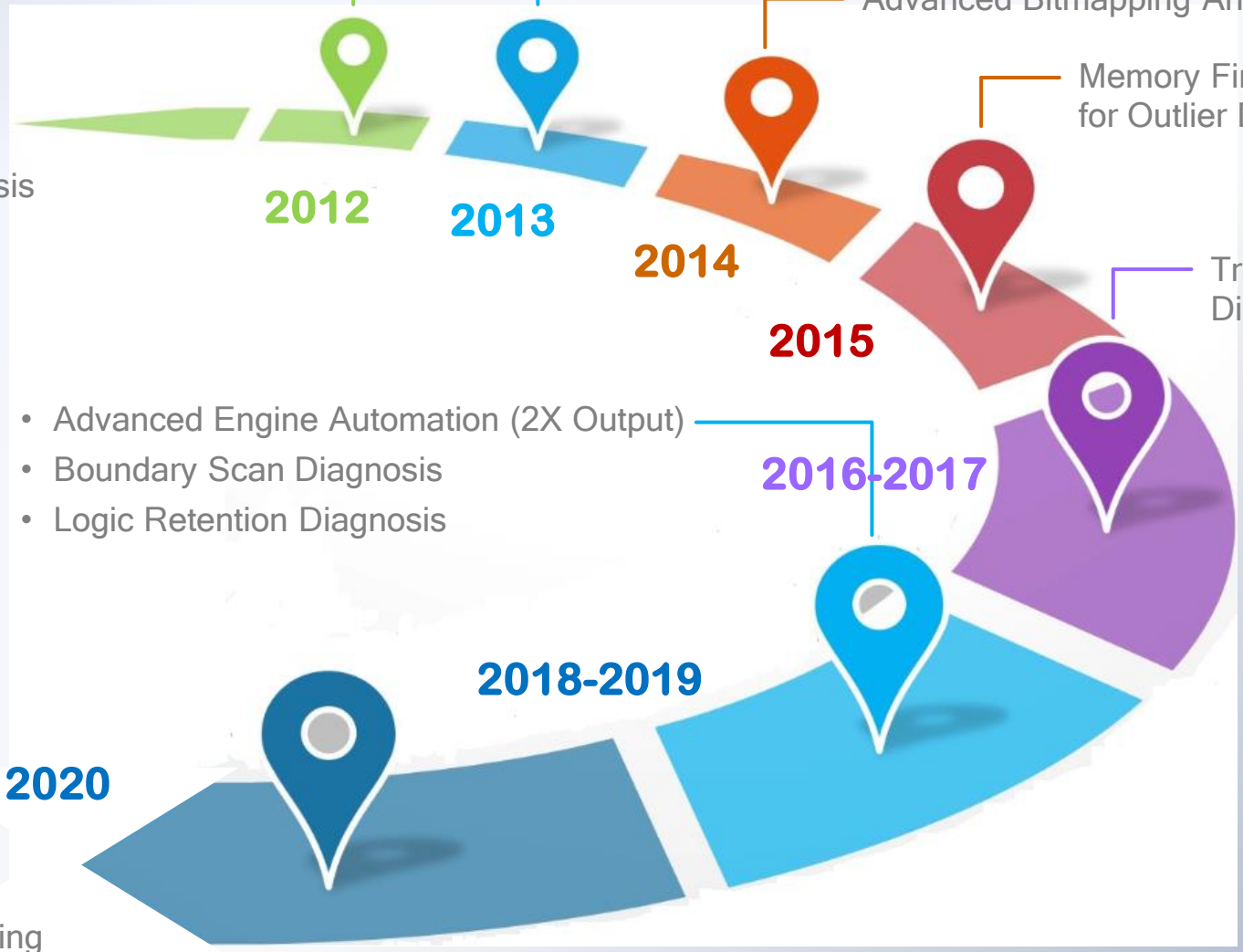
Data Integration
- Feed Forward enabled
- Feed Back capable
- Meta-Data generator

Is Structural & System & Functional Tests increasing?

• Process • Design • Physical Design • DFT • SW Engineering • Operations • Reliability • Quality

Source: Qualcomm Technologies data

Silicon Diagnostics Evolution at Qualcomm Technologies



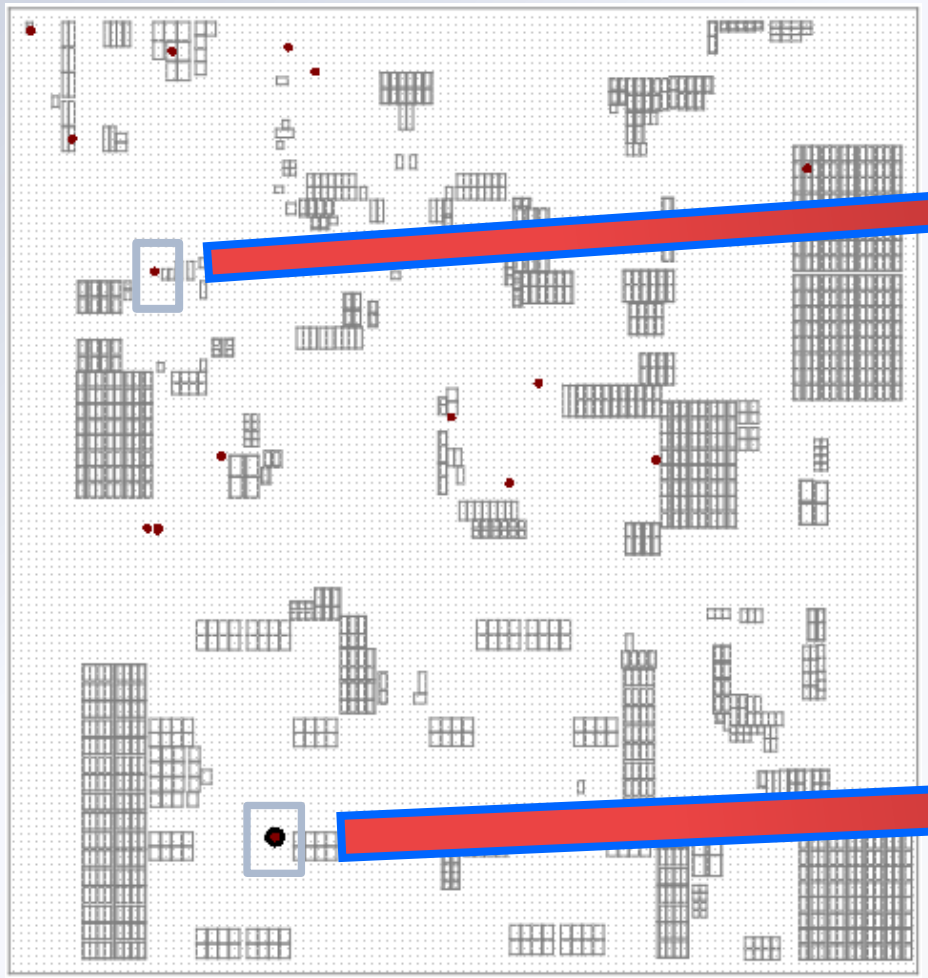
Development in Progress

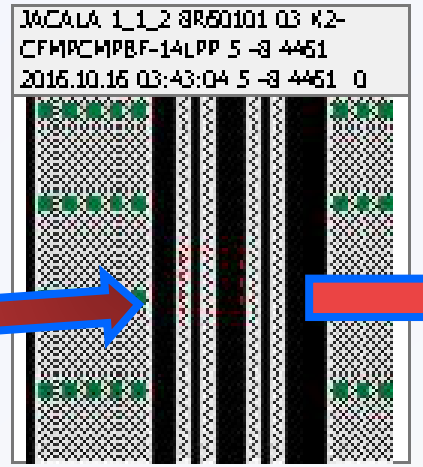
- Ultra-high Precision Diagnosis
- Reversible Scan Chain Diagnosis
- SRAM Peripheral Diagnostics
- On-chip Bitmapping
- SRAM Transistor Fault Isolation
- Pattern Recognition Machine Learning

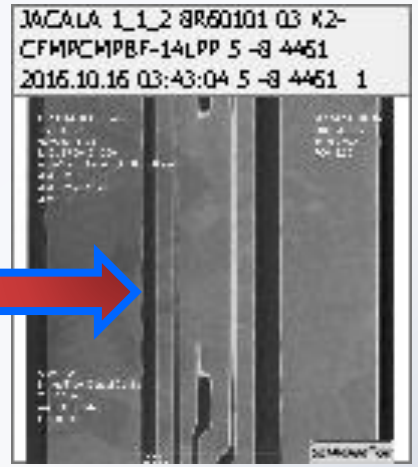
Source: Qualcomm Technologies data

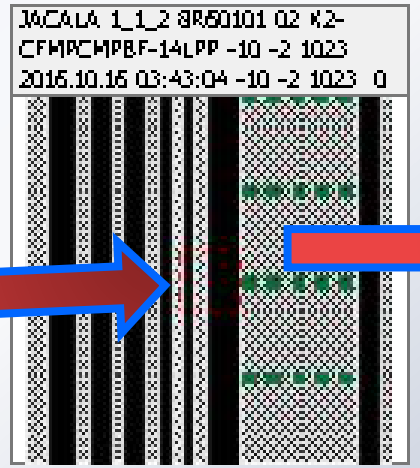
Diagnostic to Scan “Hits”

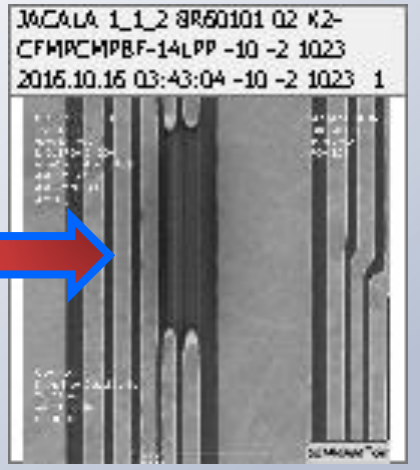
SHORT’s









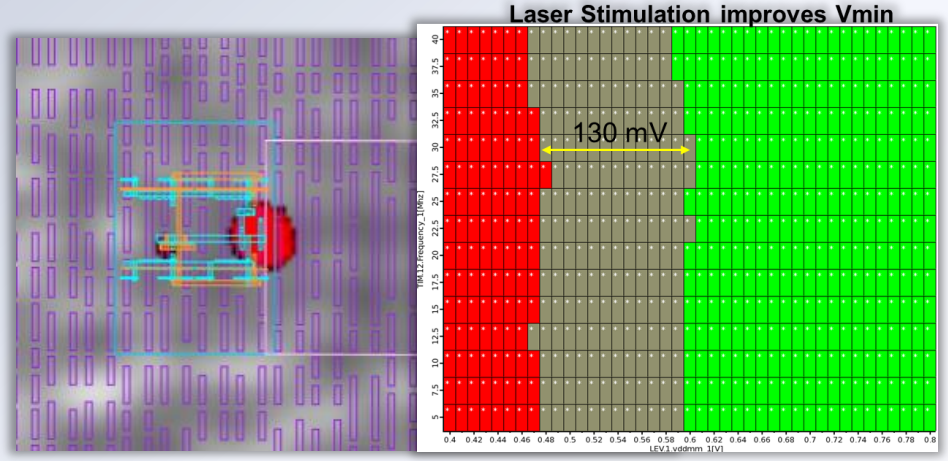


OPEN’s

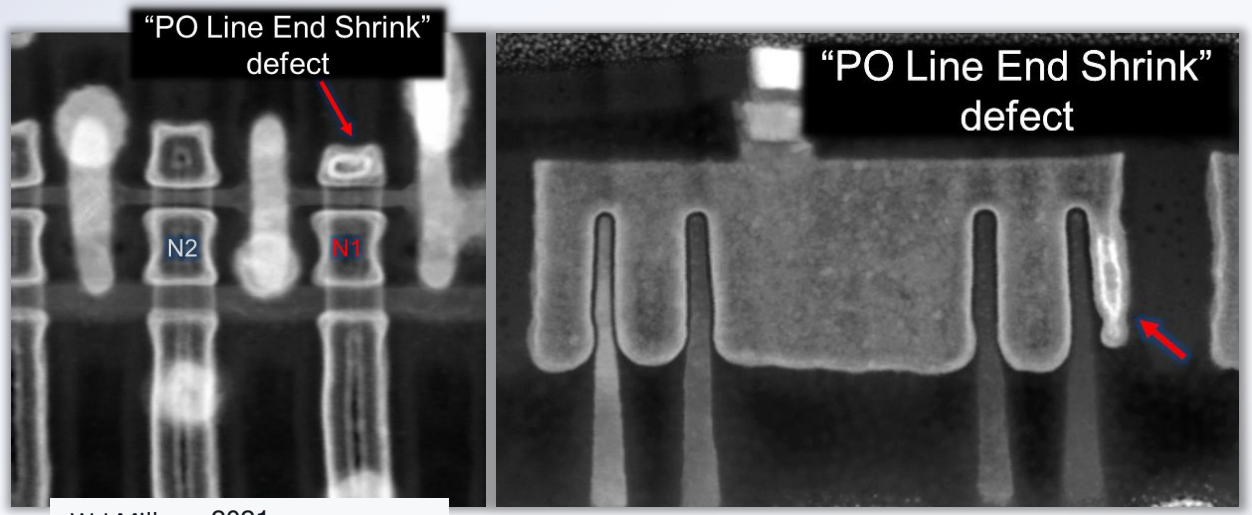
Source: Qualcomm Technologies data

7nm Graphics ATPG high yield fallout

- ✓ Fault Isolation using DLS showed sensitivity to clock inverter within fail flop.
- ✓ Nanoprobe analysis shows DLS site clk nmos to have 20% lower Isat and ~70mV higher Vt
- ✓ TEM analysis reveled “PO line end shrink” defect

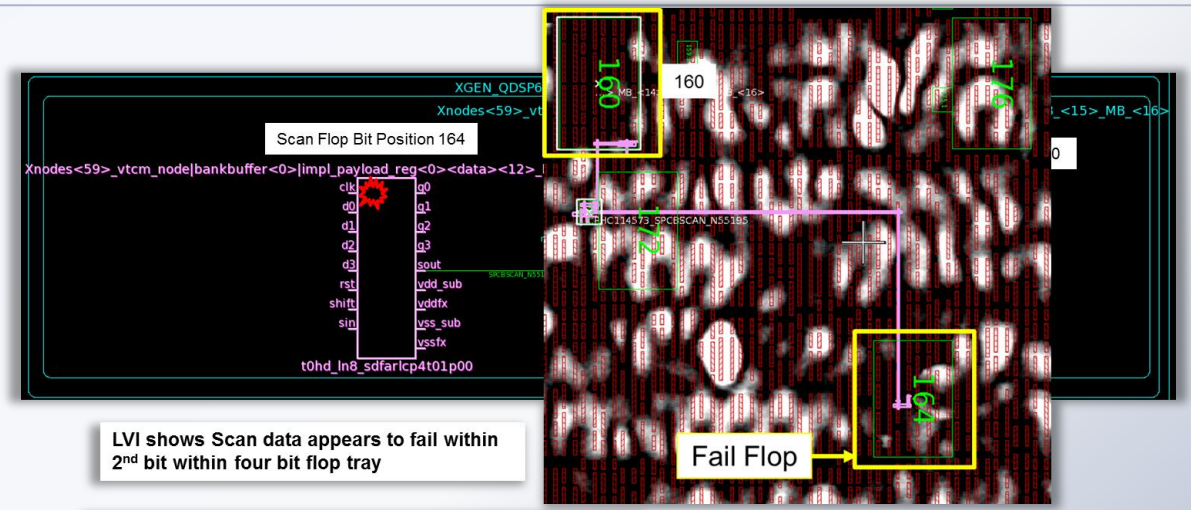


DLS Fault Isolation localized “clk” inverter within Flop

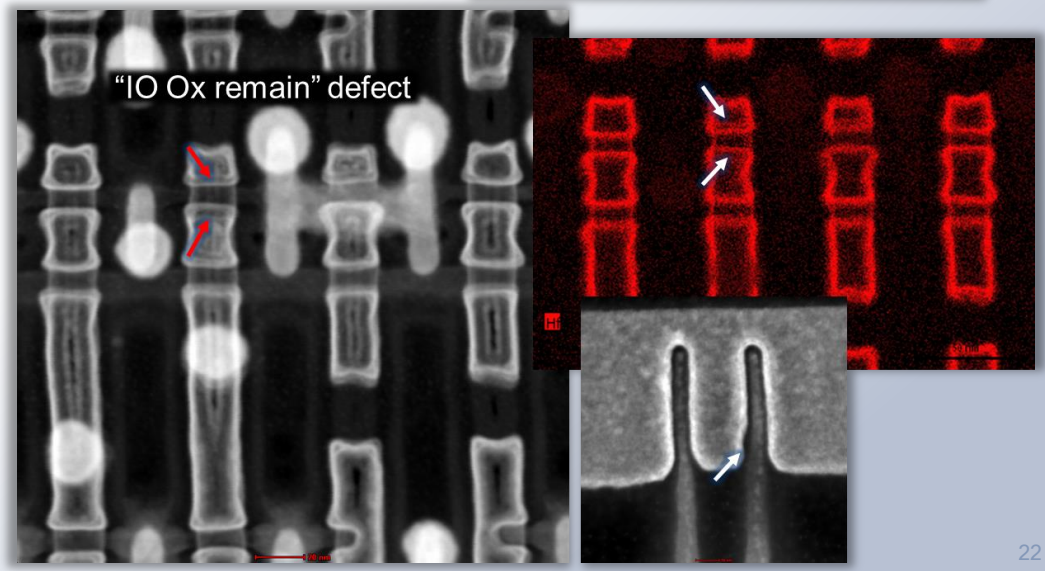


7nm Chain Integrity Vmin Fail

- ✓ Higher fallout on FF parts.
- ✓ LVI analysis data propagation fails within flop tray and likely not global timing related. DLS and PFA analysis confirmed “IO OX remain” defect.

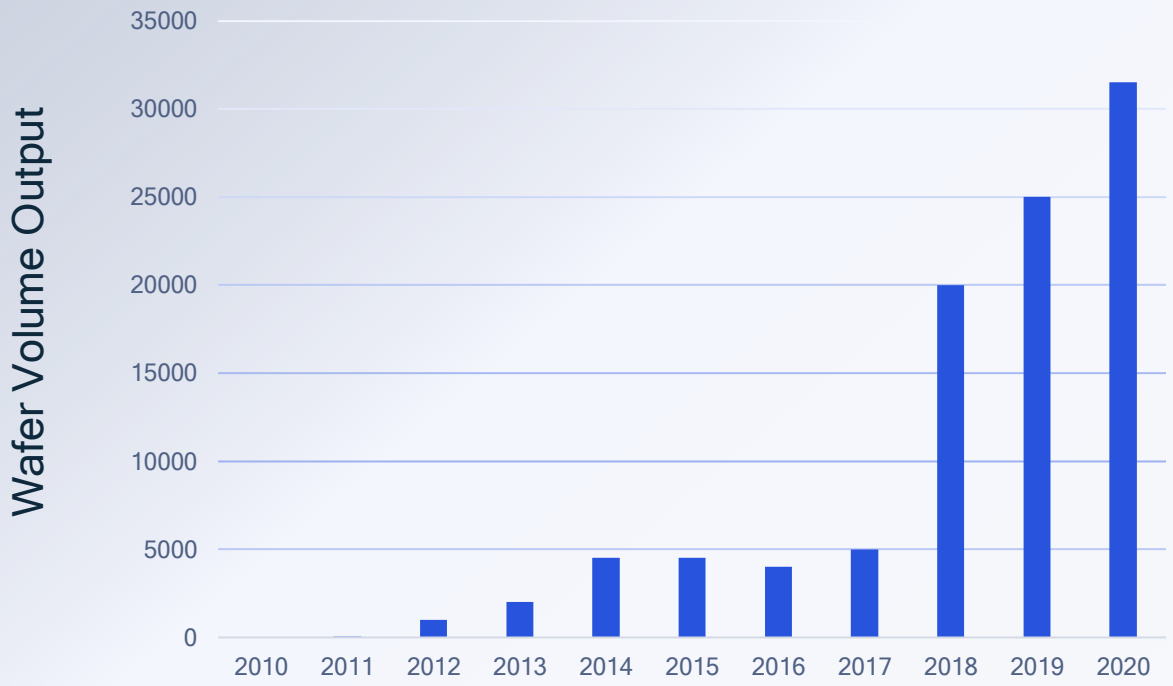


LVI shows Scan data appears to fail within 2nd bit within four bit flop tray



Source: Qualcomm Technologies data

Achieving Statistical Volume Diagnosis



- Advances in diagnostics engines, automation, and data operations management increases output
- Diagnostic for statistical diagnosis now available for all products

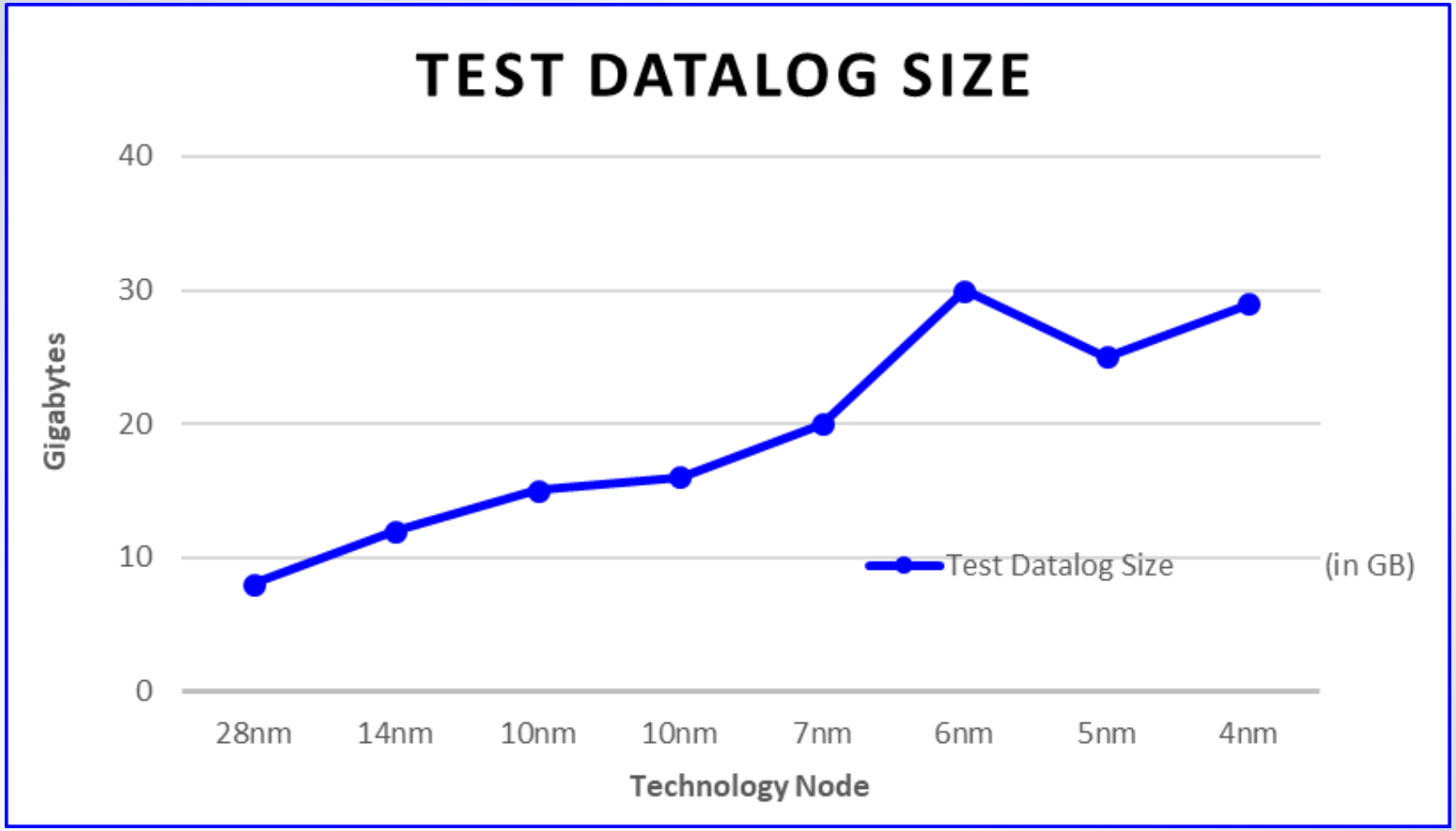
2011

2021

- Single die diagnostics data of key Mobile Digital SOC only
  - ***High wafer volume for statistical analysis limited by tester capacity and capabilities.***
  - Need for more COF testing
  - Data combined with design, STA, fab process, inline metrology, PCM, WS, FT, and EFA/PFA data for normalization & correlation analysis
  - Integrated data flows with Foundries / SATS for fast data sharing & joint analysis

Source: Qualcomm Technologies data

Tester Data Log Growth By Technology node



Increased number of cores / more test corners drive Data Log Size

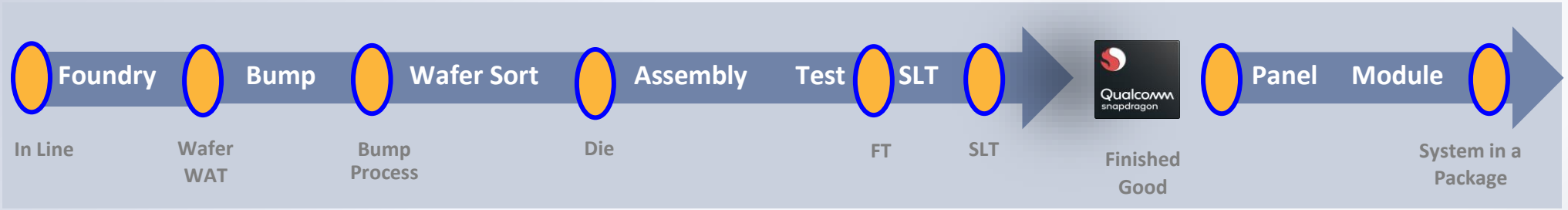
Along with increased amount of COF Testing for Diagnostics

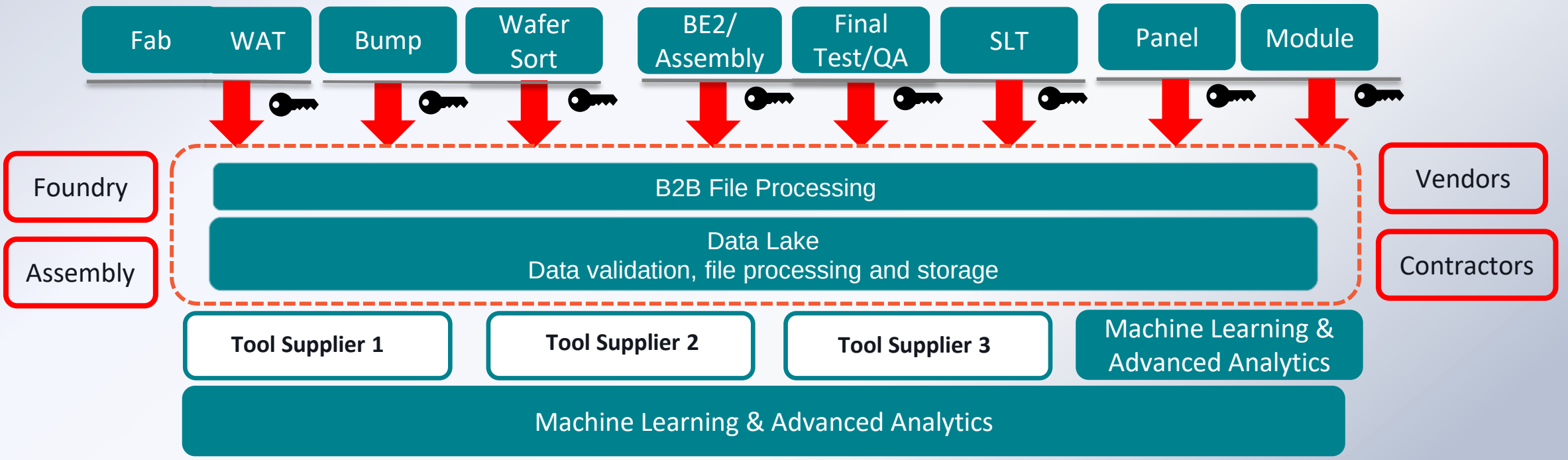
Source: Qualcomm Technologies data

Time to data available for predictions

Security required at every stage of the flow

How is the application/solution protecting our IP/Data?

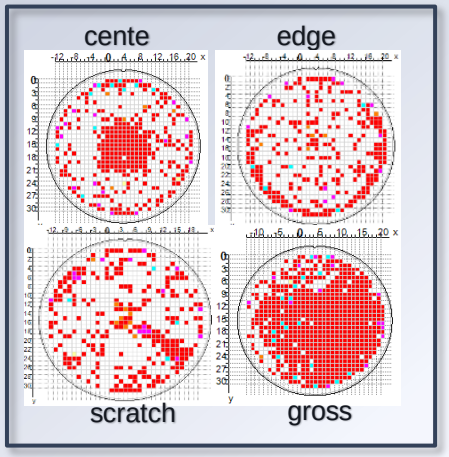


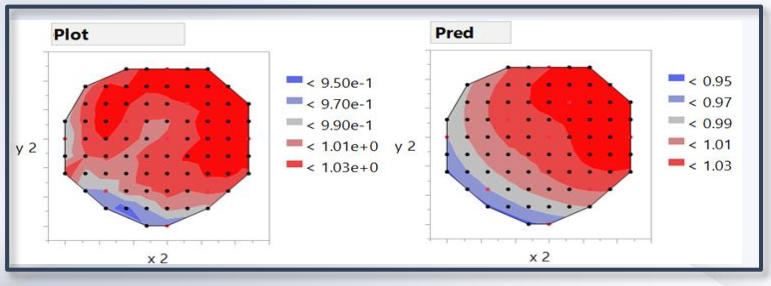


Source: Qualcomm Technologies data

Machine Learning: Reducing Virtual Metrology Error
>10X Improvement. Better Data = Better Analysis

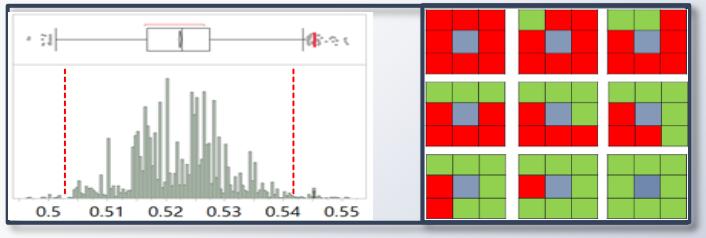
AUTOMATED DISPOSTIONING



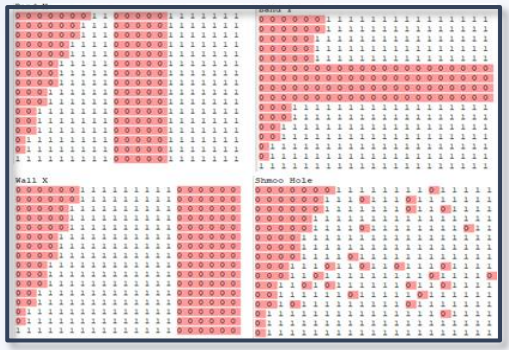


Machine Learning Use Cases

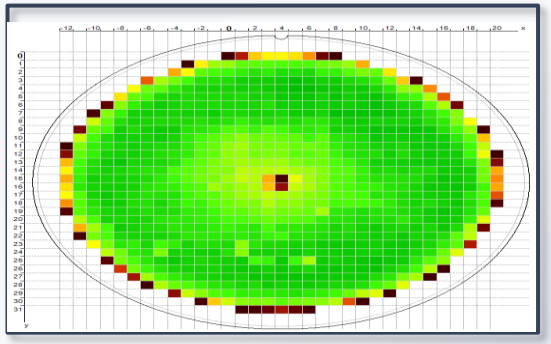
IMPROVED OUTLIER DETECTION
Reduced Overkill



AUTOMATED SI. CHARACTERIZATION
More Complete Data. Lower Labor Costs



'Lean Test Coverage Test models'



YIELD/DPPM PREDICTION - CAUSABILITY
Driving more effective DOEs and Corrective Actions

Rank	Feature	Importance
1	PARAMETER A	0.125
2	PARAMETER B	0.11518
3	PARAMETER C	0.09309
4	PARAMETER D	0.08911
5	PARAMETER E	0.05448

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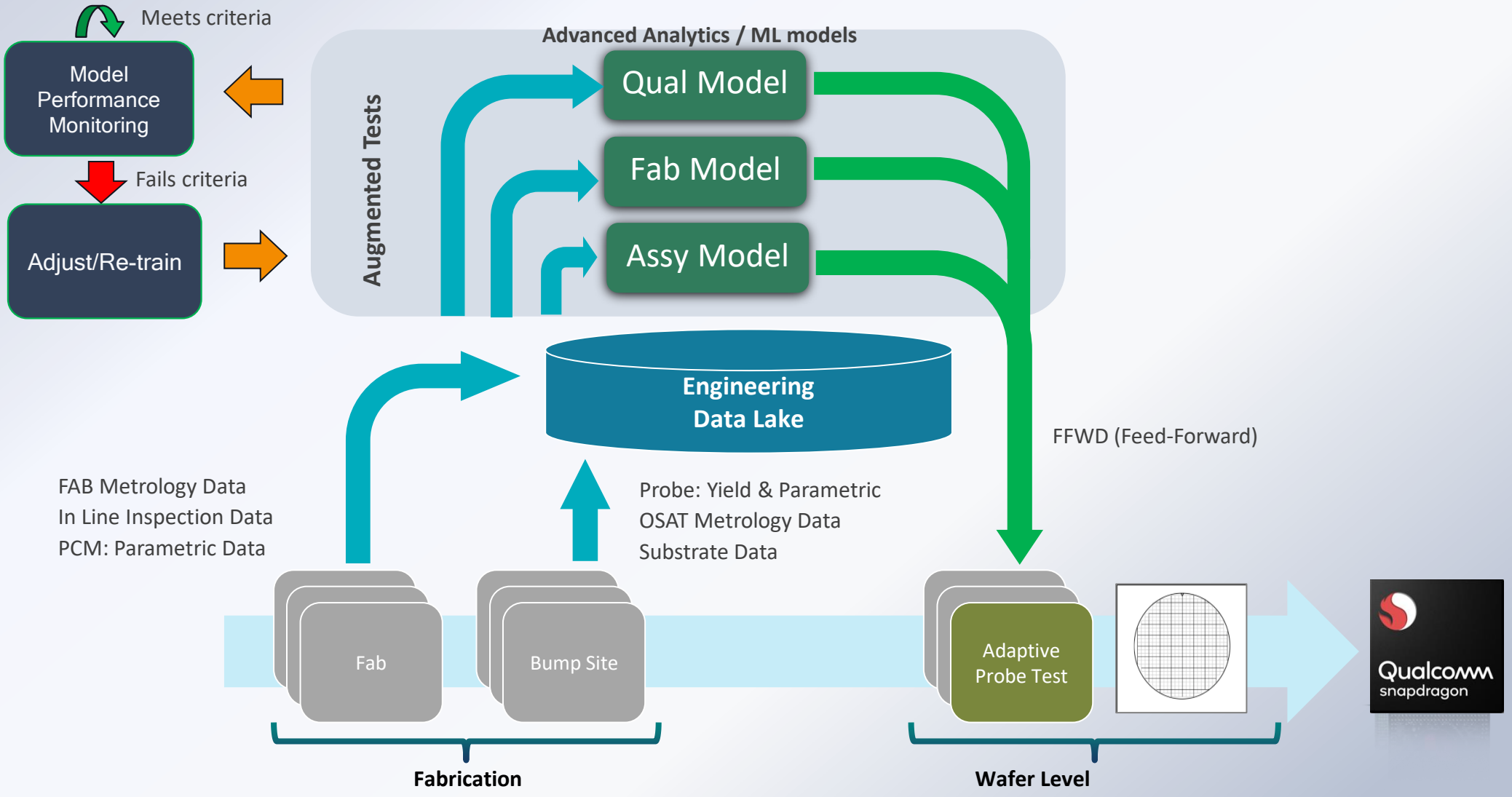
Source: Qualcomm Technologies data

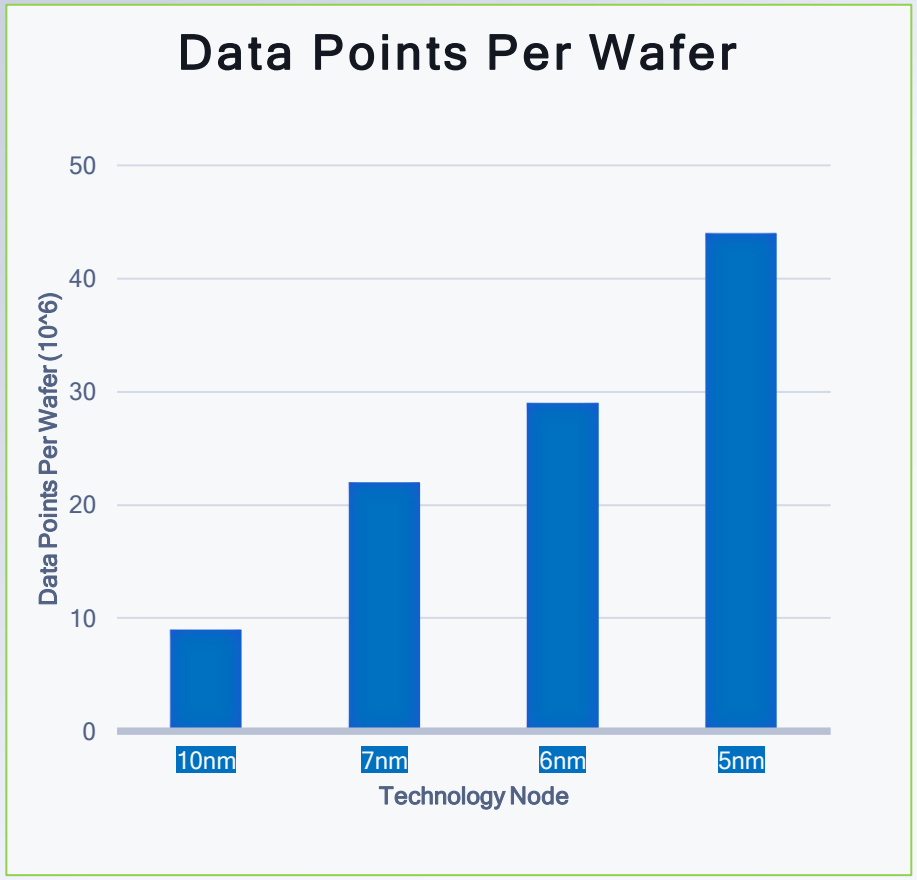
Forward Looking implementation in production (FFWD)

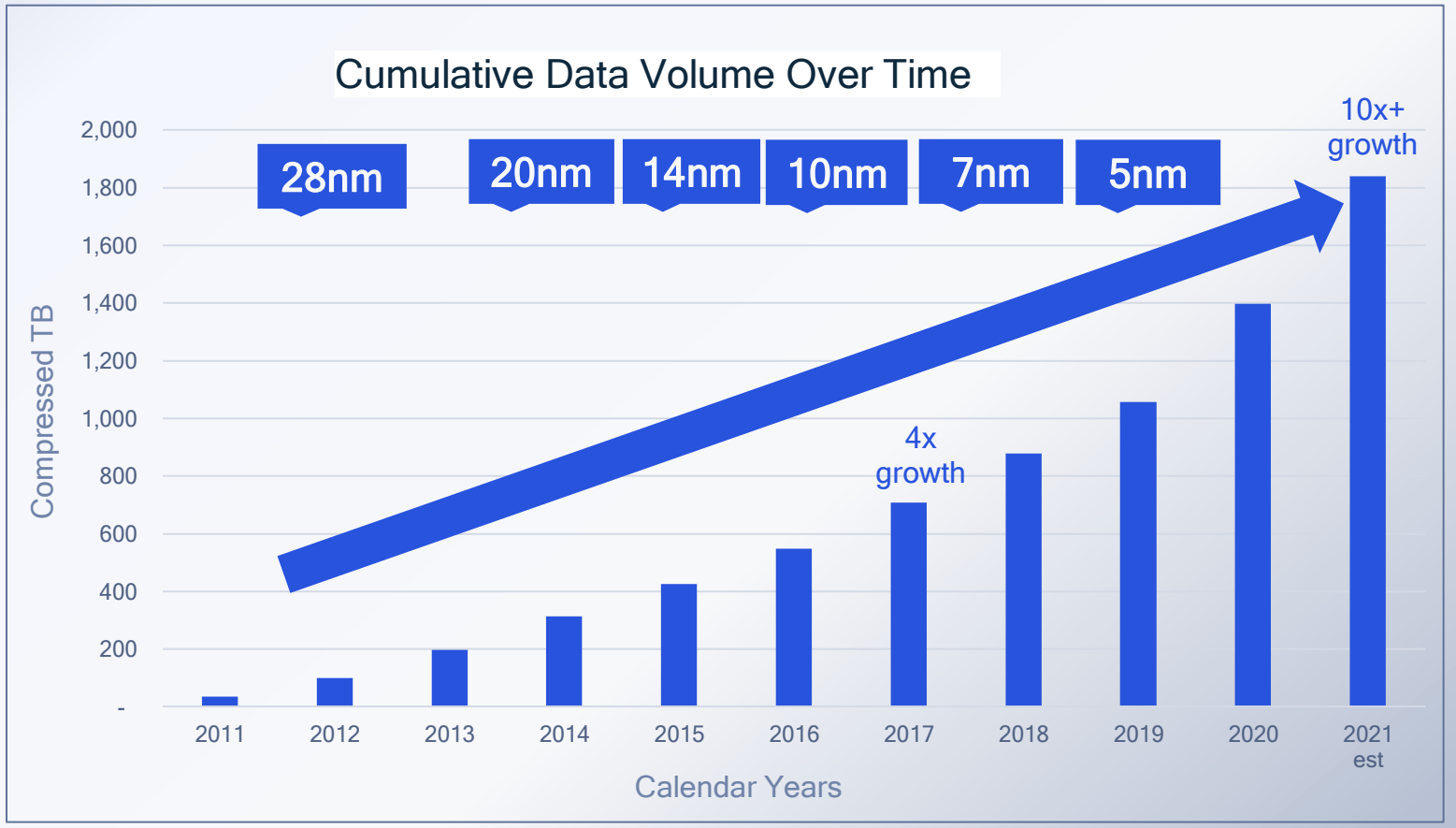


Source: Qualcomm Technologies data

Manufacturing & Yield Data Continues to Increase

ALL manufacturing data is received, stored & analyzed



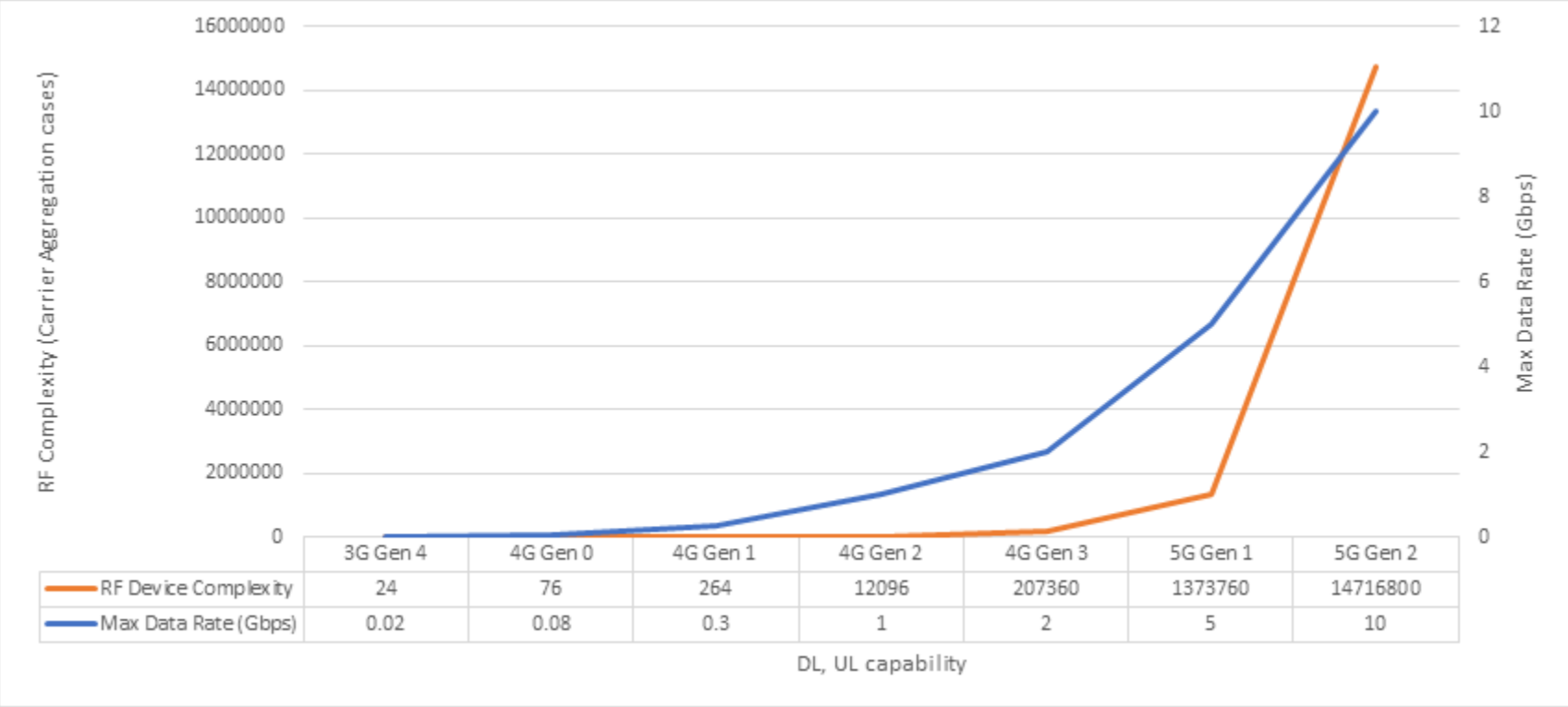


Increased Design/Process/Test/In Line data is driving data volume.

Machine Learning increasingly required to detect data shifts.

Source: Qualcomm Technologies data

RF Transceiver Device Complexity Also Increasing. Wafer production is now in Fin Fet technology



	3G Gen 4	4G Gen 0	4G Gen 1	4G Gen 2	4G Gen 3	5G Gen 1	5G Gen 2
RF Device Complexity	24	76	264	12096	207360	1373760	14716800
Max Data Rate (Gbps)	0.02	0.08	0.3	1	2	5	10

- Premium Tier driving higher data rates year over year
- 4G to 5G transition grows the characterization requirements exponentially
- Peak Data rates increased from 0.6 Gbps to 5Gbps from 2015 thru 2019 (8X increase)
- RF complexity increased from ~250 to >1.37 Million (1000X increase) combinations of Carrier Aggregation

Source: Qualcomm Technologies data

Direct Far Field Chamber

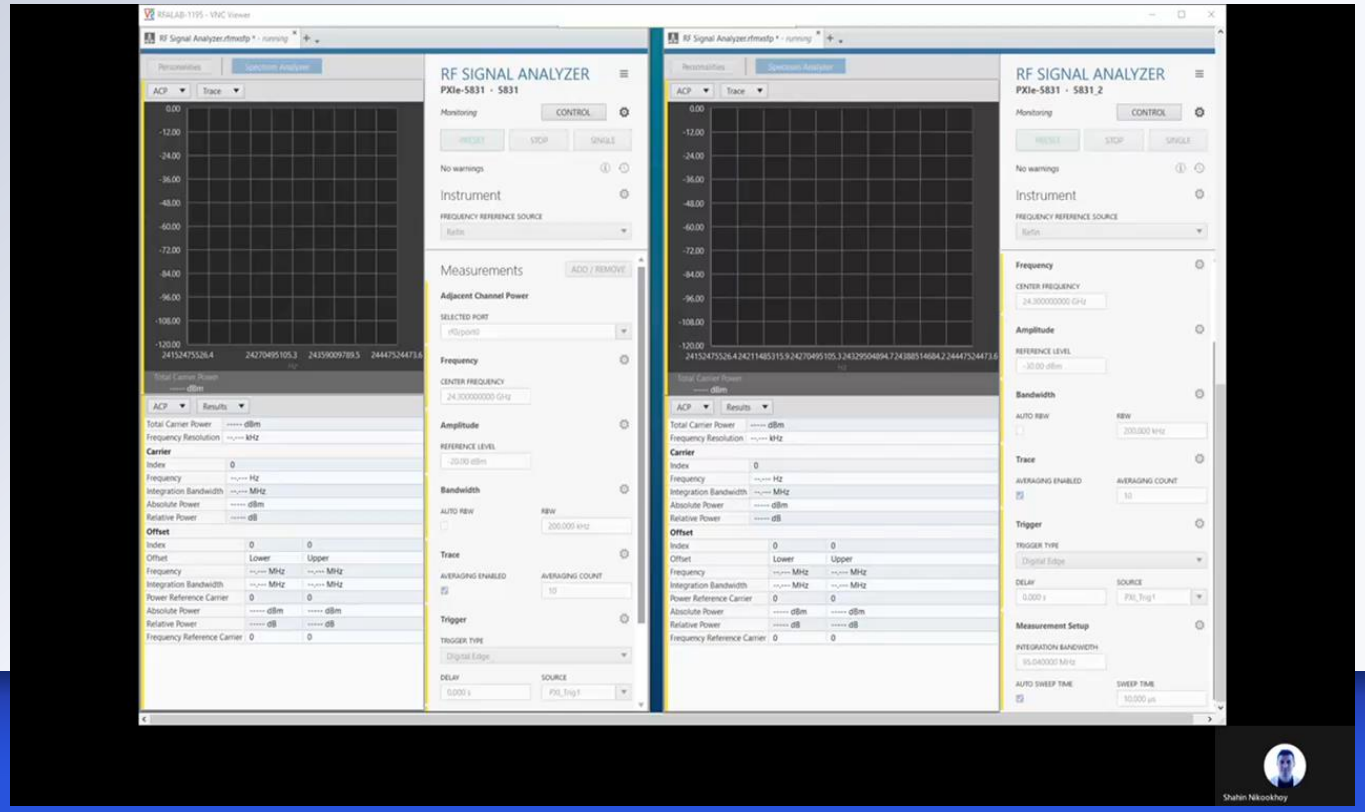
Working with vendors to improve :

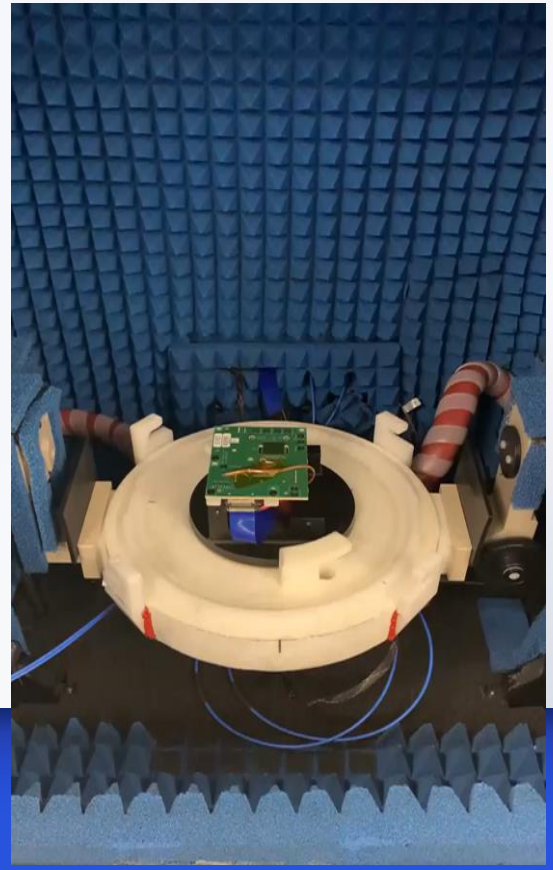
- Improved Over the Air characteristics
- Reduce test times
- Develop extended temperature support

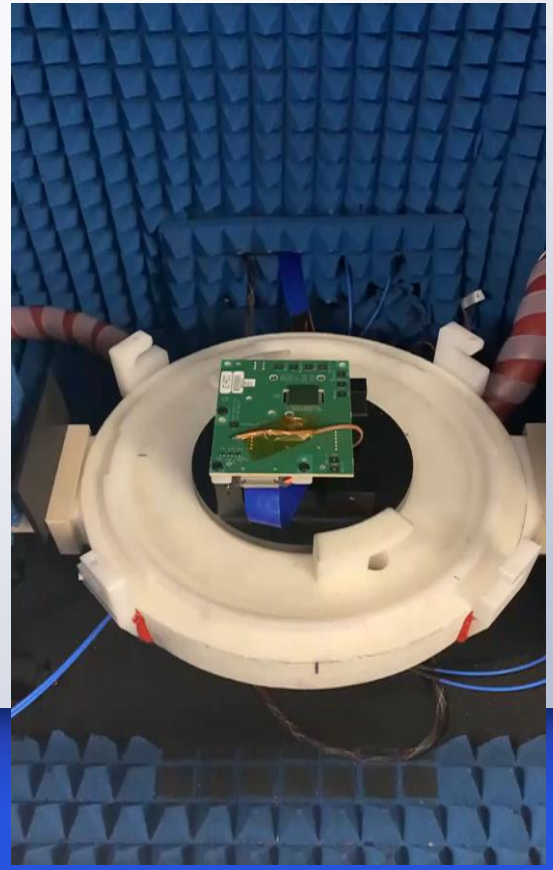
Source: Qualcomm Technologies data

Phase Aligned Dual Head System for Simultaneous Horizontal / Vertical polarization captures

- Phased Aligned measurements with ~40% TTR vs Single head system

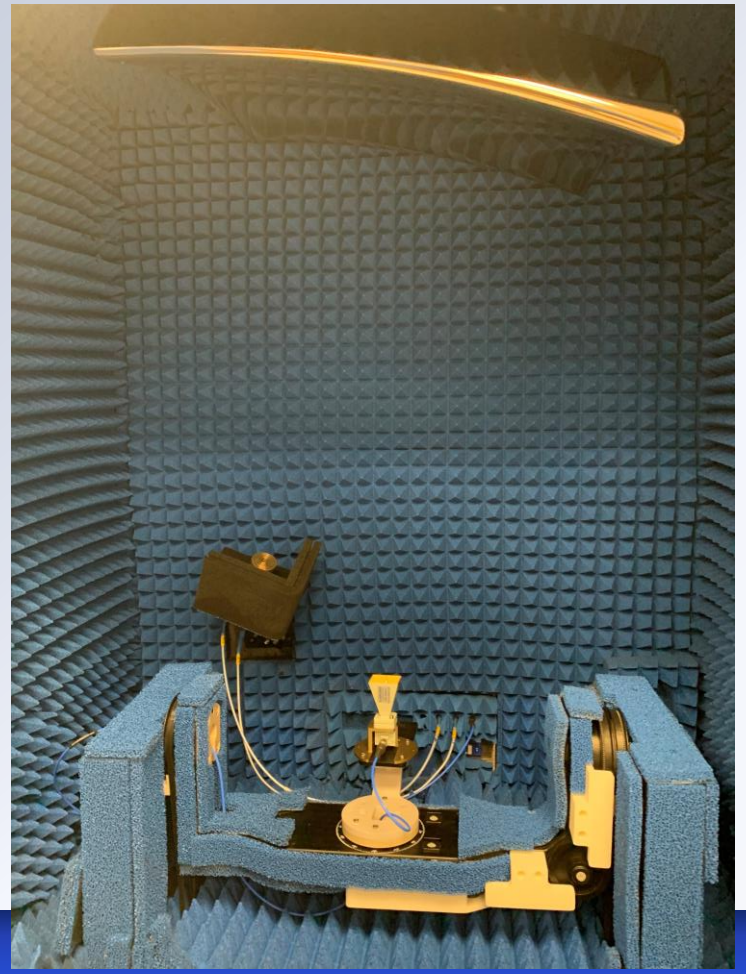


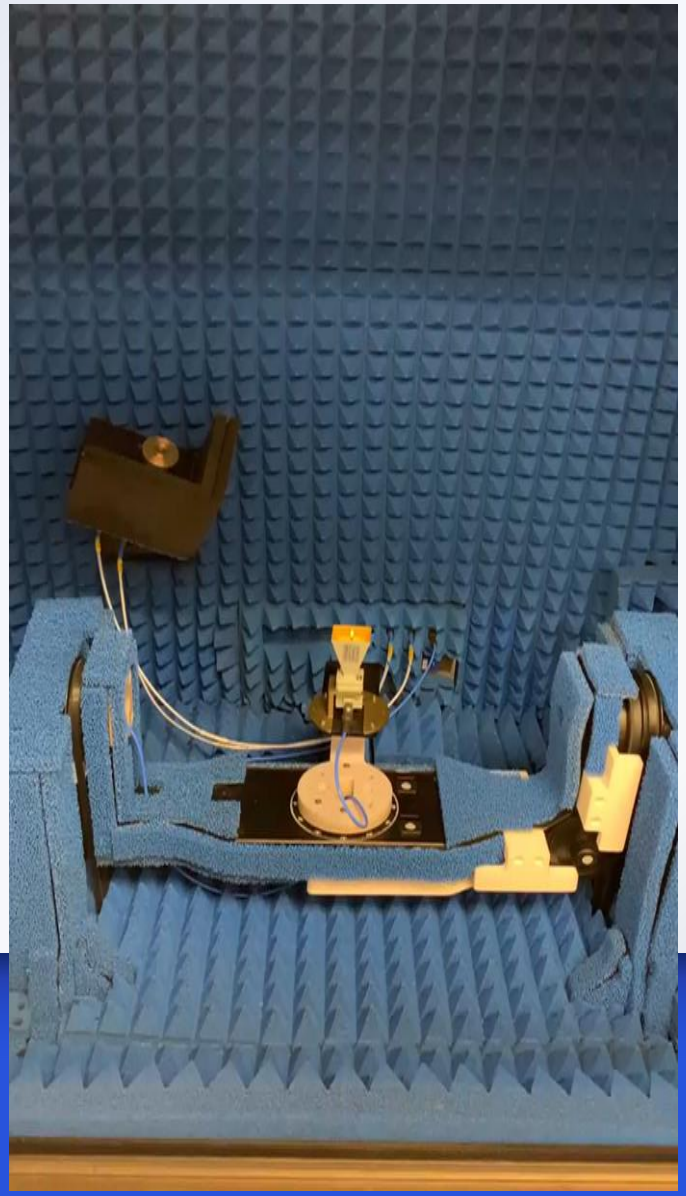


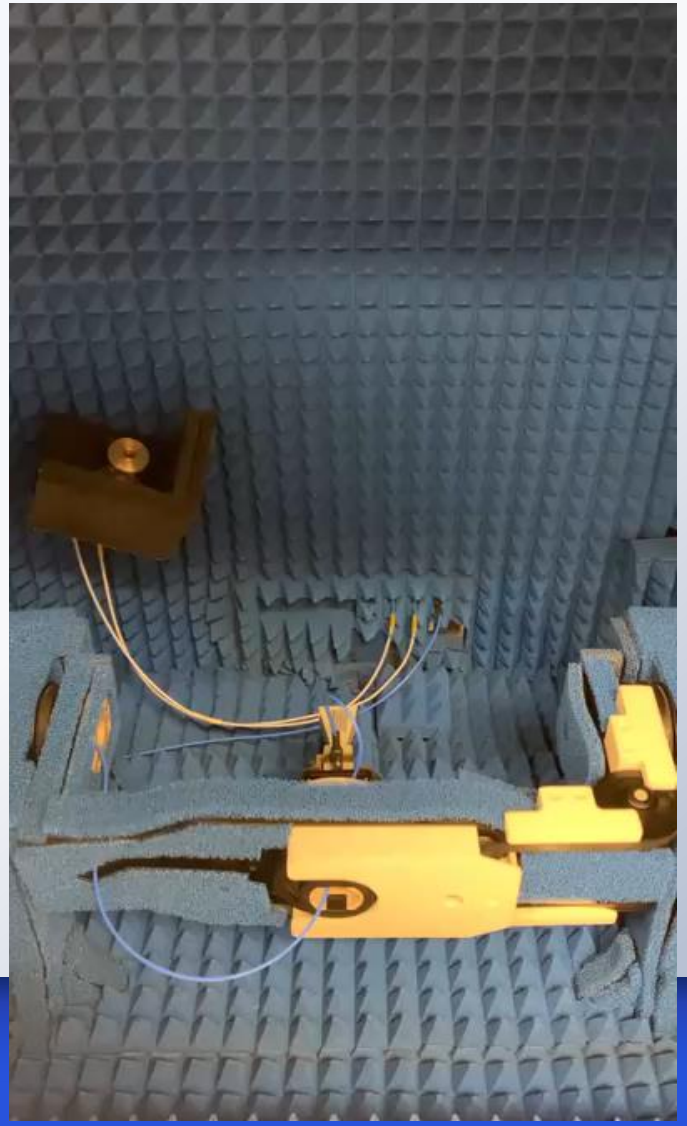


Source: Qualcomm Technologies data

CSM – CATR Characterization Platform Evaluation







Source: Qualcomm Technologies data

RF & RFFE Test, Tester, Probe challenges

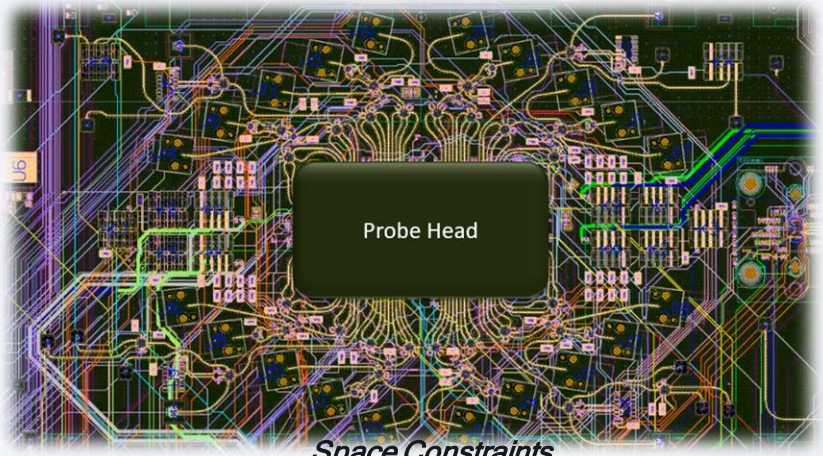
- Signal integrity versus mmWave /high band specification versus port count density
- Routing : challenge of routing multiple DUT and high port count (32/DUT) RF performance, and component placement
- DUT application space for components (i.e. multiplexers, RF switches and cables) versus stiffener stiffness and tester resource allocation / placement
- Challenging mechanical specifications with competing requirements:
  - Probe: Length versus overtravel compliance. Tip length versus signal integrity versus lifetime
  - Stiffener : Stiffness versus weight , application space
  - Tester: Higher channel count/ docking force versus system deflection (few 10's of um)
  - Probe card: Planarity versus probe area for larger DUT count
  - Bump Damage
- Cost of Ownership: Probe card lifetime versus throughput , utilization rate , and cost of ownership
- Parallelism with all the challenges above versus throughput versus cost of test
- Probe card testability (QA or Repair)
  - Test coverage versus mmWave specifications
  - Test time versus DUT count
- CCC versus test requirements (higher current demand , DVS)

Source: Qualcomm Technologies data

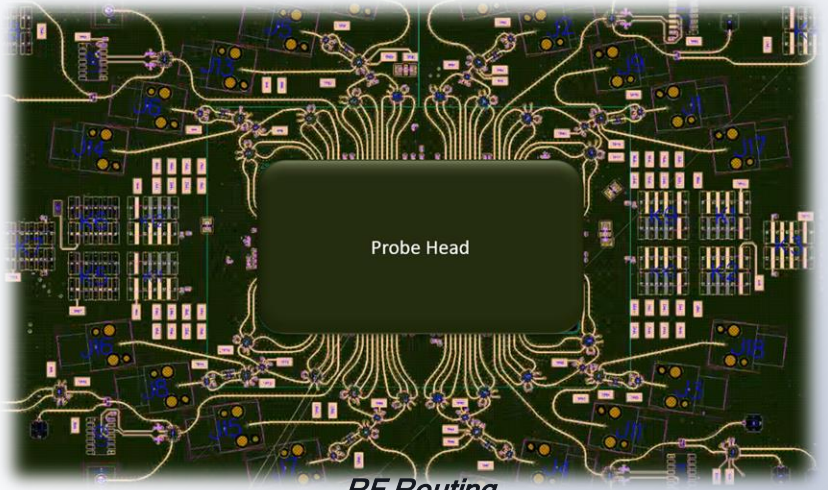
Key Challenges

- RF Signal Integrity (ex Isolation, Return Loss)
  - Focus on end-to-end simulation capabilities (probe head + board)
- Parallelism (ex space constraints, RF routing & cabling congestion / connector placement)
  - Focus on expanded application space, smaller component footprint, planarity, cable flexibility, novel stack-up approach
- Service-ability (ex NPI and production environment compatibility)
  - Focus on modular design and in-region field support
- Cycle Time (ex design, fab, assembly, and bring up)
  - Focus on resource availability / skillset and robust supply chains along with metrology
- Cost (ex probes, cables, connectors)
  - Focus on standardization and multi-company partnerships

Cabling Congestion



Space Constraints

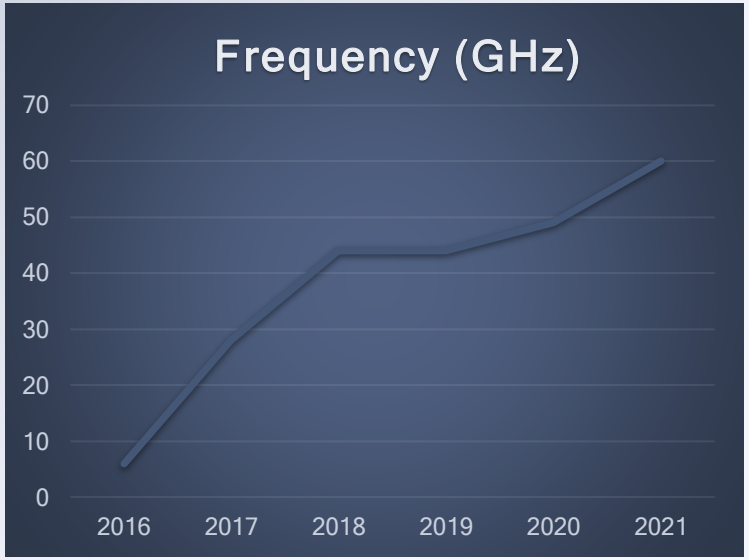


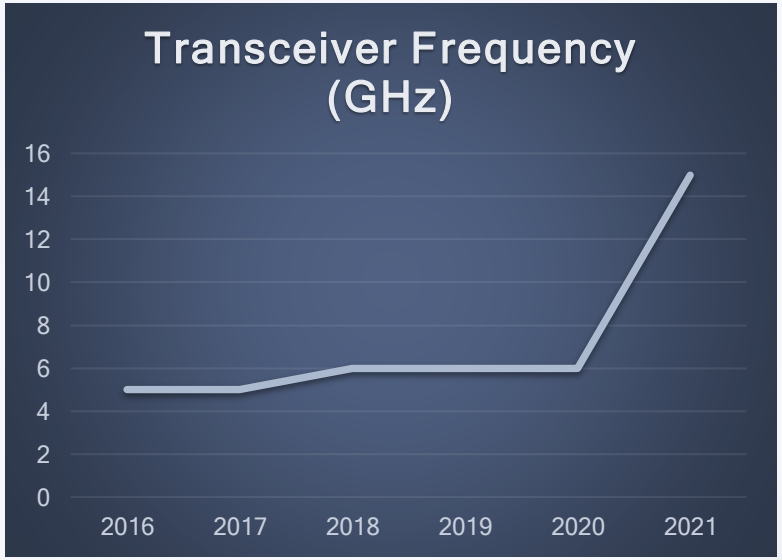
RF Routing

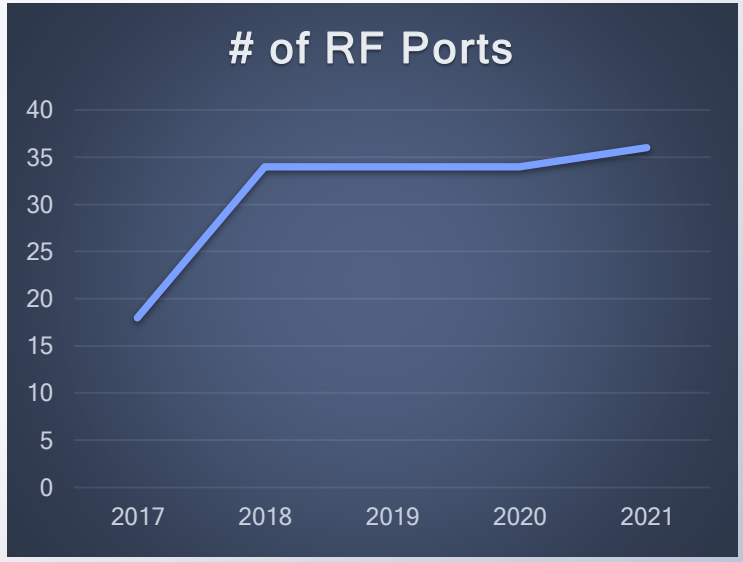
Connector Placement

Source: Qualcomm Technologies data

Frequency & RF port count greatly increased with the advancement of 5G

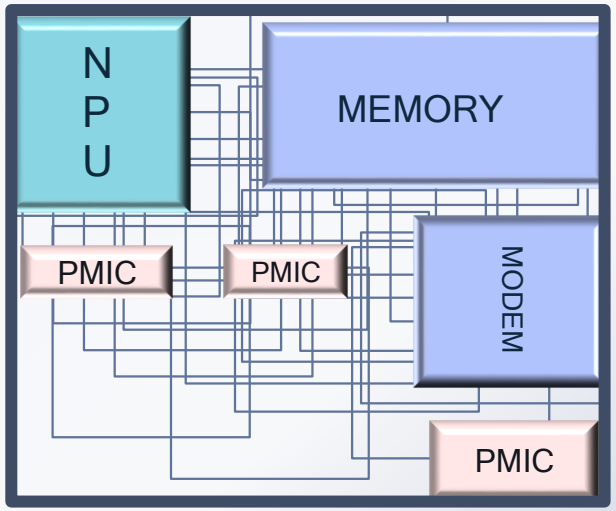






Source: Qualcomm Technologies data

CHANGE IS COMING …



Moore's Law is:

- Slowing down or flattening out
- Innovation will have to accelerate to fill the gap.
- GAA will be a challenge…. Beyond the FinFet challenges?
- Power Distribtion from the backside?

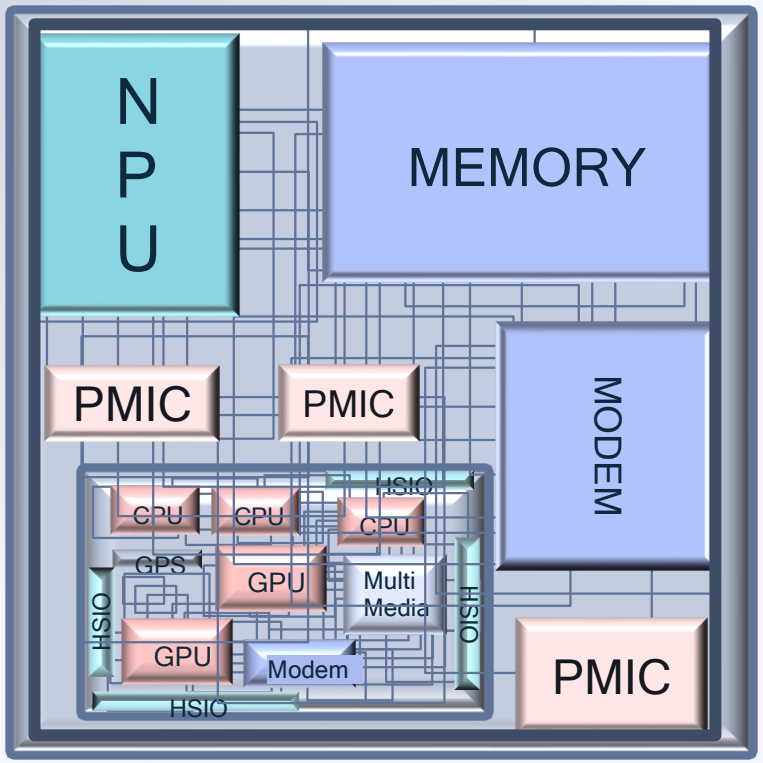
Is Heterogeneous Integration the next disruptive innovation? If so:

- Embrace packaging technology as part of front-end simulations.
- Apply SOC techniques, concepts, and tools to Advanced Packaging Solutions.
- Strive to develop end to end solutions & tools for test

Source: Qualcomm Technologies data

Packaging Technology …

Heterogeneous Integration is coming, and it does impact test.



REQUIRES THE SAME SOLUTIONS AS SOCs

- ✓ High Fault Coverage
- ✓ Fault Isolation
- ✓ Effective Pre-Silicon Simulation
- ✓ Effective/Diagnosable Functional Test
- ✓ Functional verification
- ✓ System Testing

POTENTIAL ISSUES:

- ✓ Only externally facing IO pads
- ✓ Chip to chip Scan chains
- ✓ Timing closure for interconnected components
- ✓ Fault models for the system
- ✓ System test to Structural test correlation for Fault Grading

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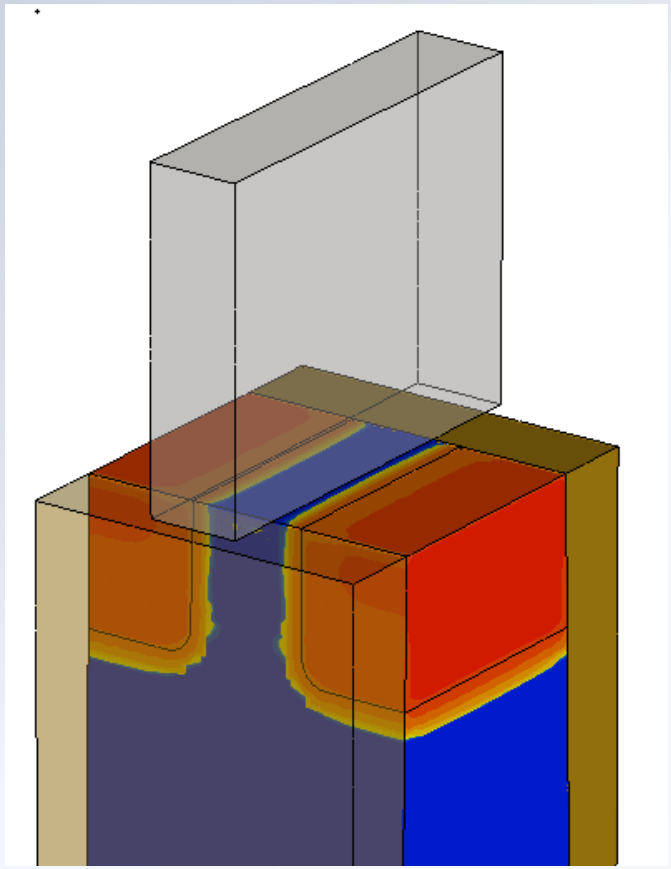
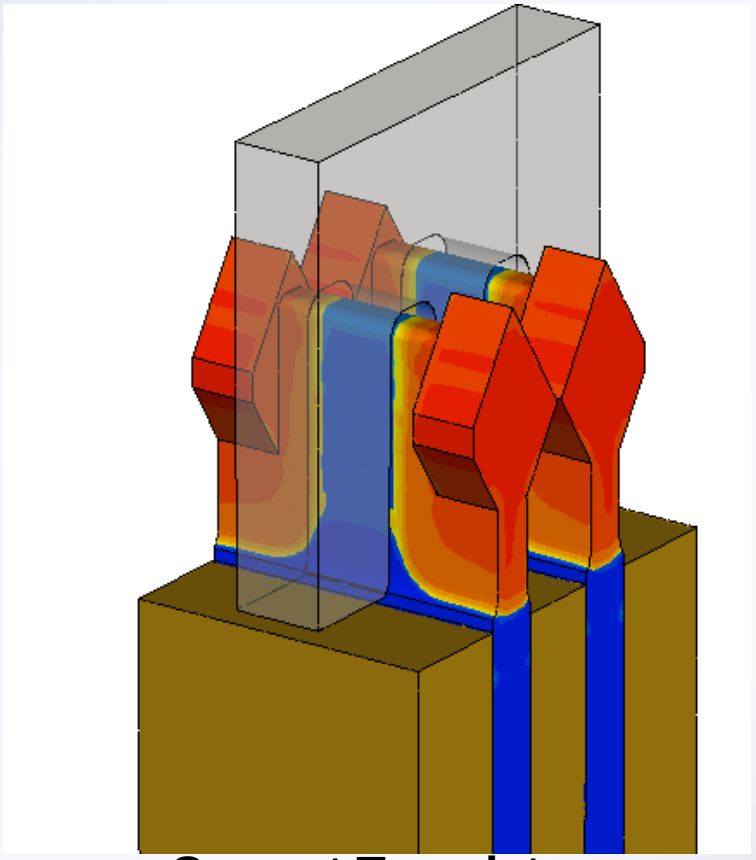
Source: Qualcomm Technologies data

The Future is coming !

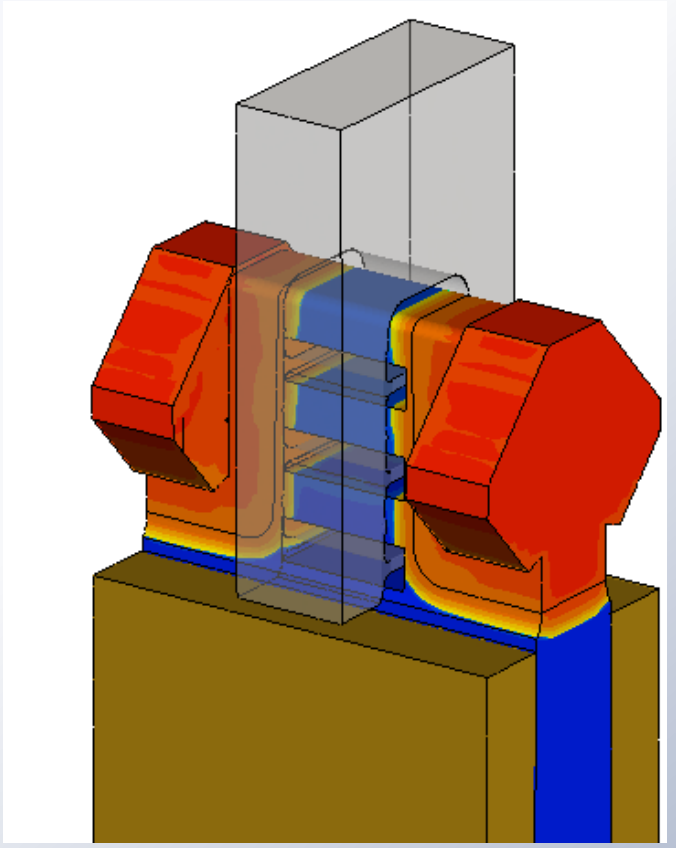
Transistor evolution



Past Transistor
Gate ; 1side (Planar)



Current Transistor
Gate ; 3side (FinFET)
60~70mV Vdd reduction



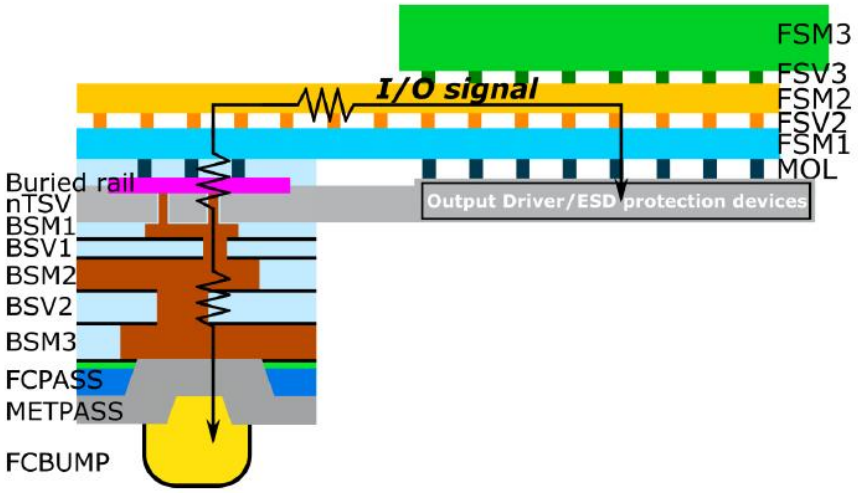
Future Transistor
Gate ; 4 side (All-Around)
Additional 50~60mV Vdd reduction

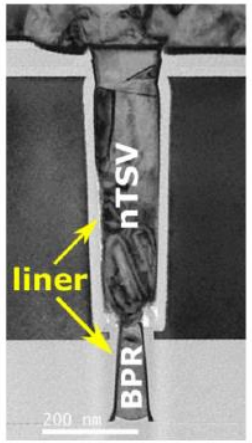
Source: Qualcomm Technologies data

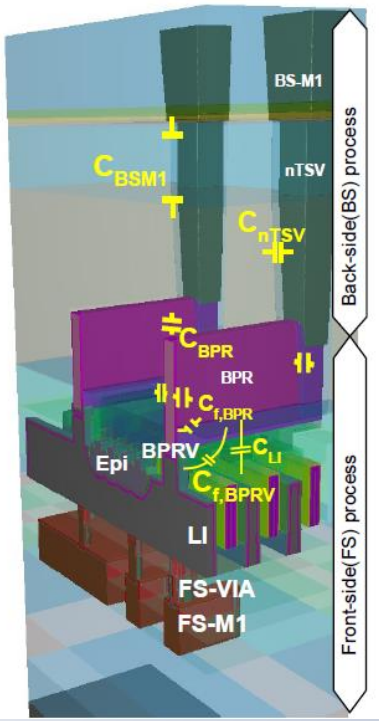
Transistor evolution

External I/O in fully BS connection

- Parasitic RC
  - \+ Decoupling the noise for power delivery
  - – Deteriorate performance of signal delivery







By Permission from IMEC

Source: Qualcomm Technologies data

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Thank you

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