SWTEST
2021 CONFERENCE
PROBE TODAY,
FOR TOMORROW

30TH ANNIVERSARY

High Power goes Vertical

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T. I. P. S.

CREA
SEMICONDUCTOR TEST EQUIPMENT

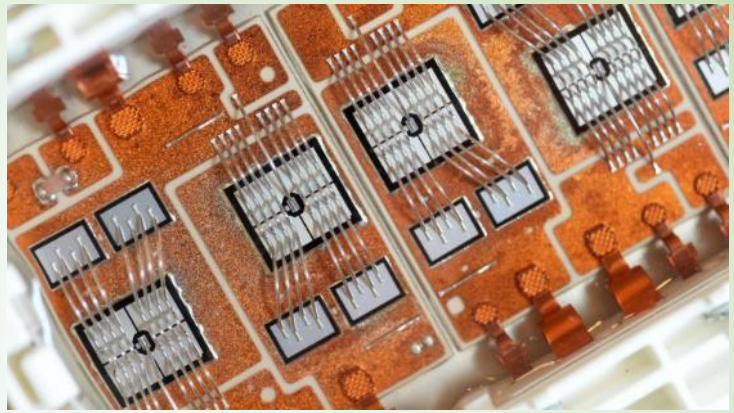
Aug. 30 – Sep. 1, 2021

Overview

- Motivation
- Current Density on Chip - Cantilever vs. Vertical Probes
- Chip Pad Metallization – Cres Stability
- Probes Protection
- Conclusion

Motivation

- **Power modules used in Electro-automotive application**

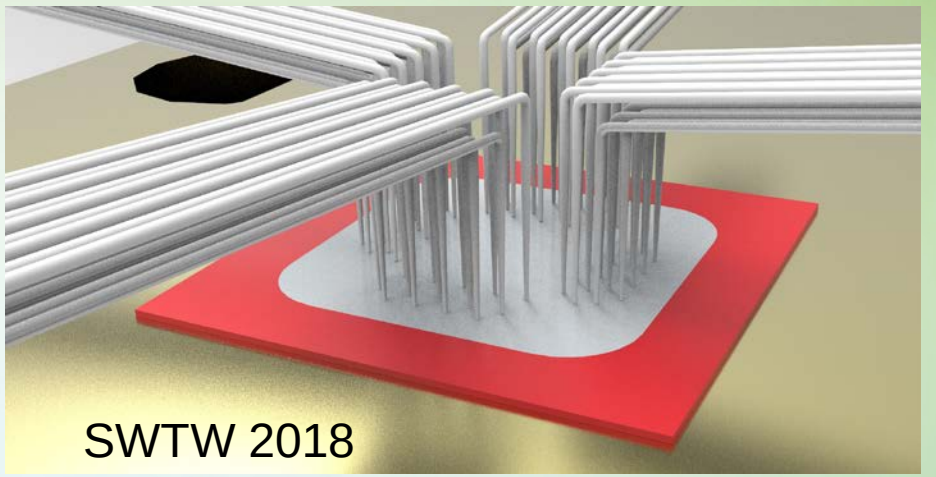


Extremely harsh test conditions for power devices (IGBTs, Diodes, MOSFETs) dictated by Automotive application

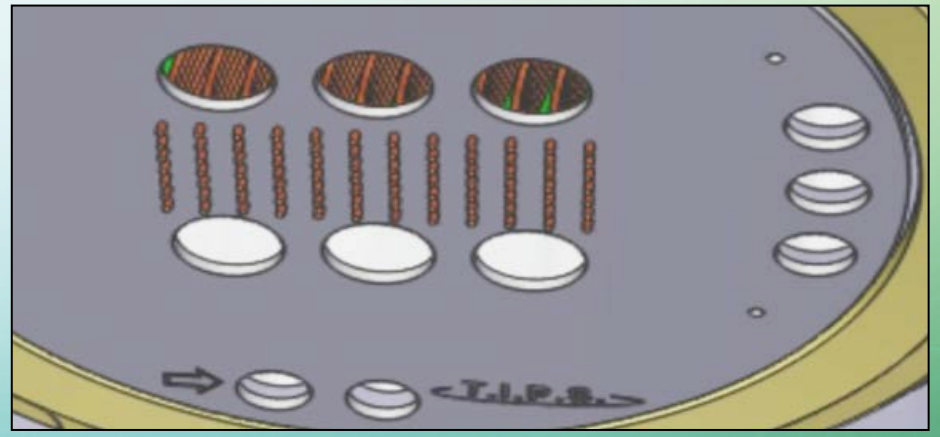
- short circuit test (SCT) at up to 10x rated device current (shooting pulses of up to 3000 A on a single chip...)
- highest current densities - made possible by SiC devices
- at hot temperature
- high voltage dynamic switching tests
- bare die test (KGD)

Motivation - why going Vertical?

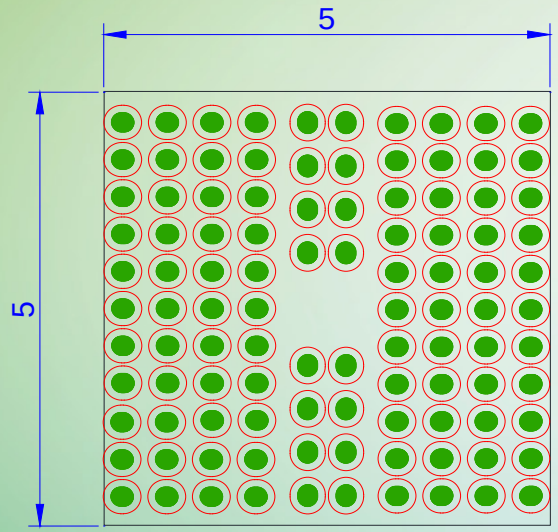
- **Cantilever probes technology is well established for KGD power test up to 1000 A**
  - runs into limitations at very high chip current densities (A/mm^2 on chip pad)

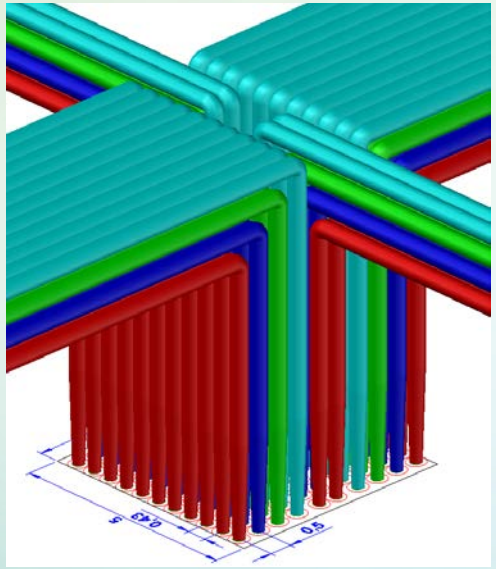


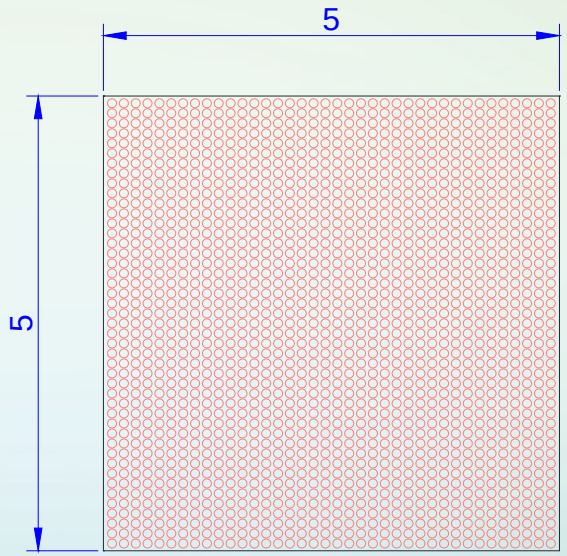
- **Vertical probes technology – an option?**

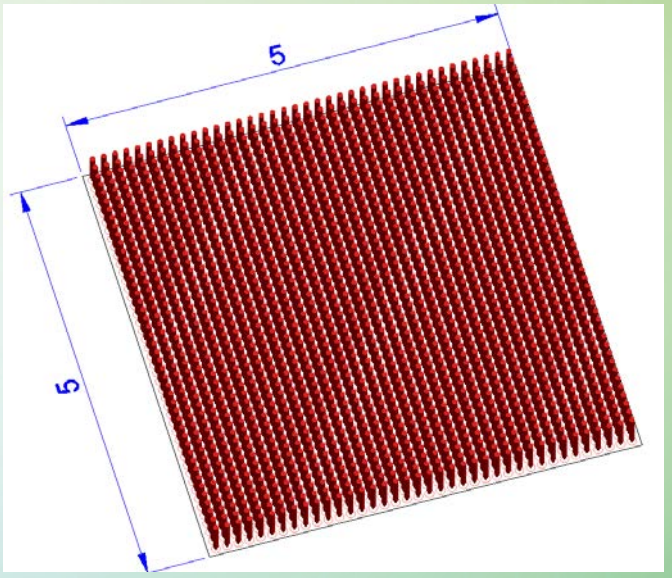


Current densities for cantilever and vertical probe cards
Small Chips – 5x5mm





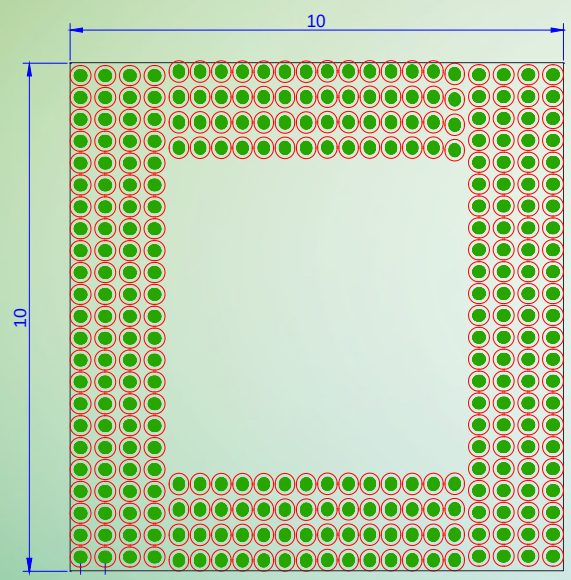


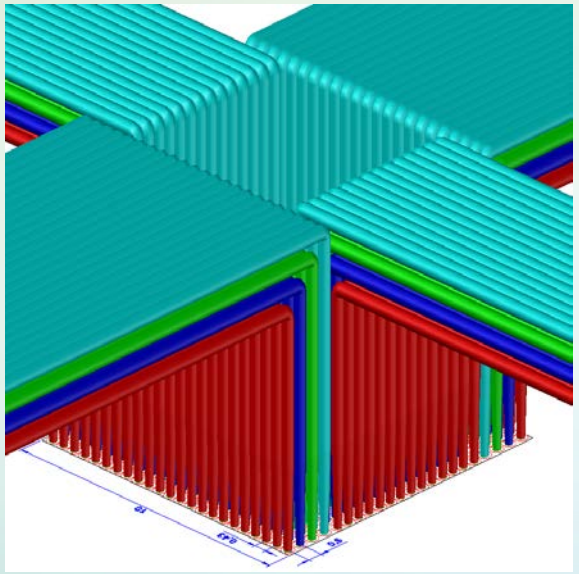


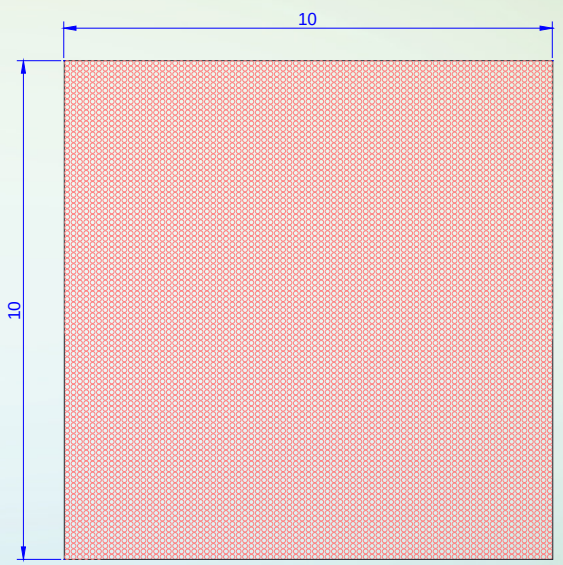
Cantilever 40A/mm²

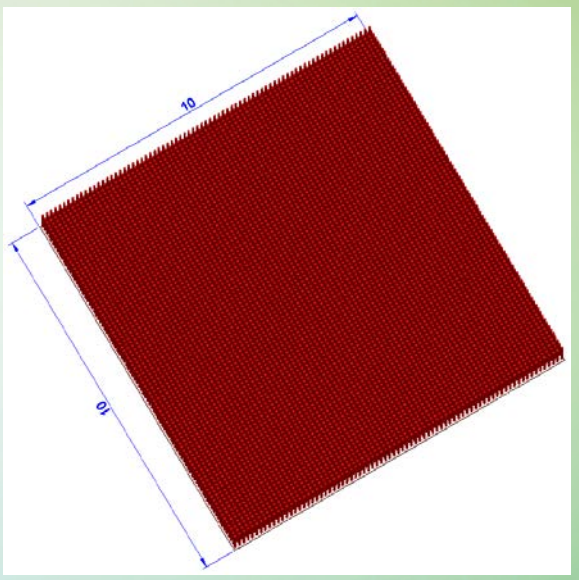
Vertical 70A/mm²

Current densities for cantilever and vertical probe cards
Big Chips – 10x10mm









Cantilever 30A/mm²

Vertical 70A/mm²

Current densities for cantilever and vertical probe cards

Conclusion:

- Due to geometrical constraints regarding number of needle layers, current density of cantilevers decreases with increasing chip size

- With vertical technology, the current density remains almost constant as the chip area increases

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- **Probes Protection**
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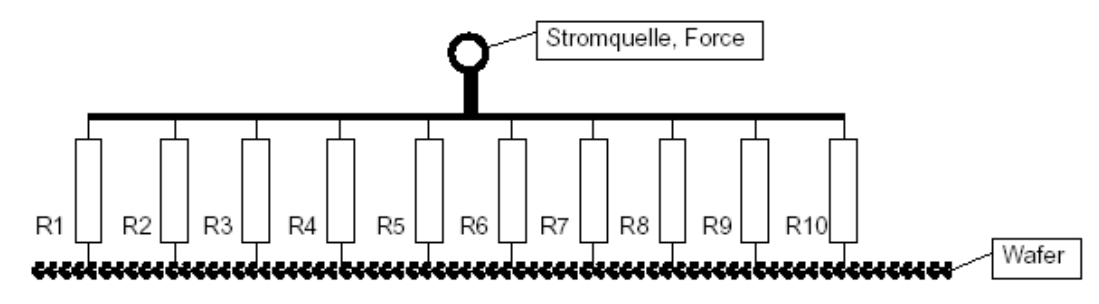
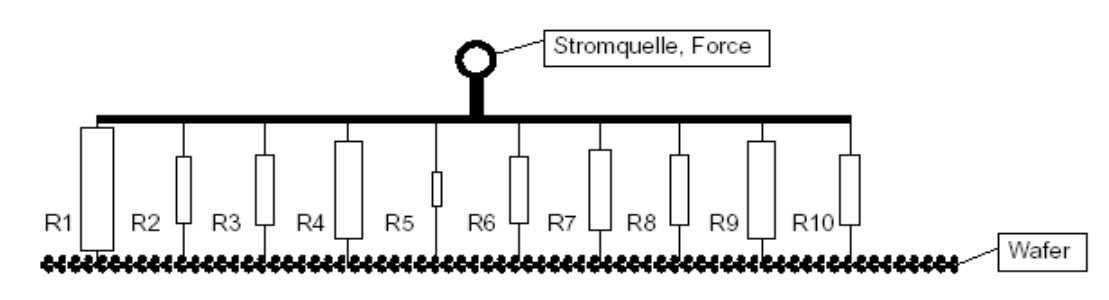
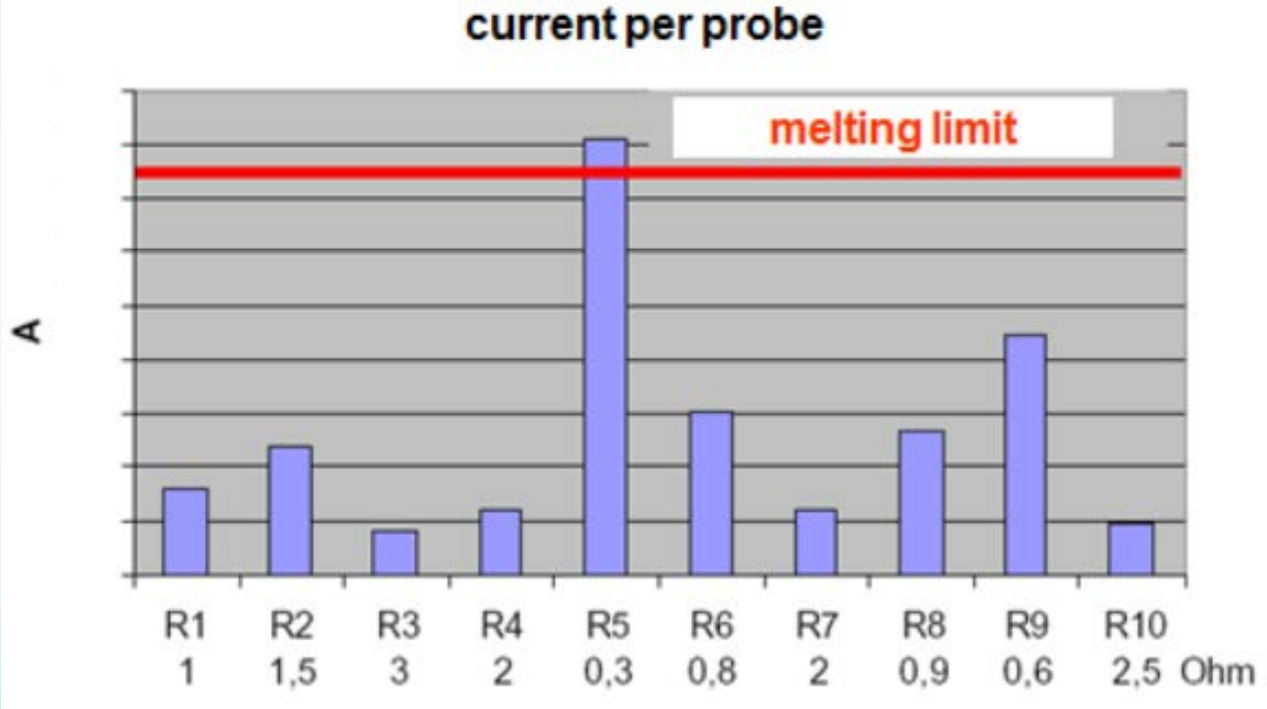
Cres effect on probes lifetime



Ideal probing condition- constant Cres

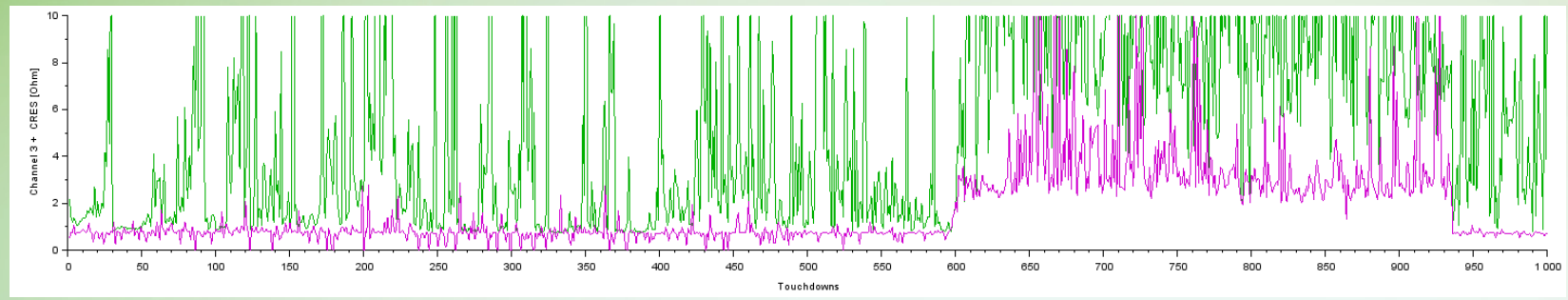


Less than ideal condition- varying Cres



Current imbalance – probe damage

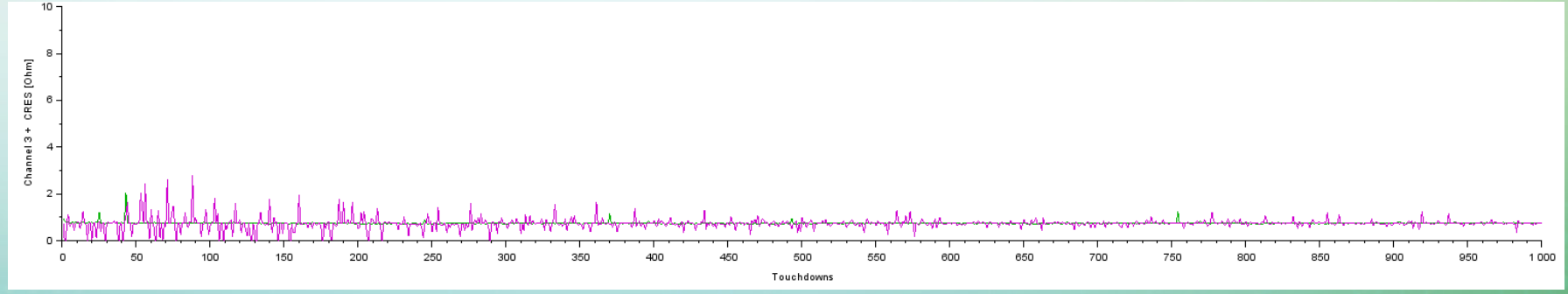
Contact Resistance vs Pad Material



Al pads

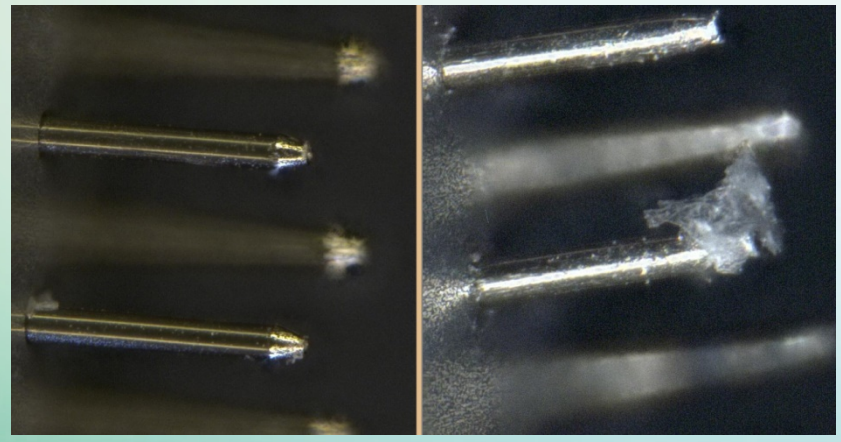
Pad material is extremly important in terms of contact resistance

Cu pads

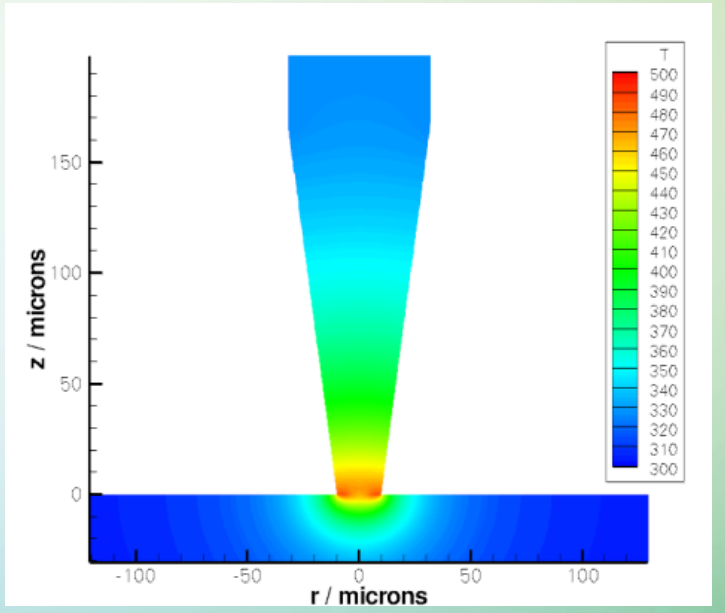


What matters…

- **Constant CRES is important for current balancing and needle wear**
- **Sensitive to tip contamination**



Before \ After



Probe tip heating in high current short pulse condition

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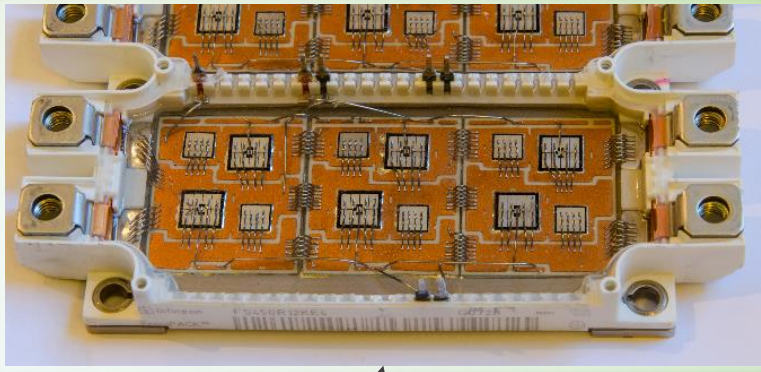
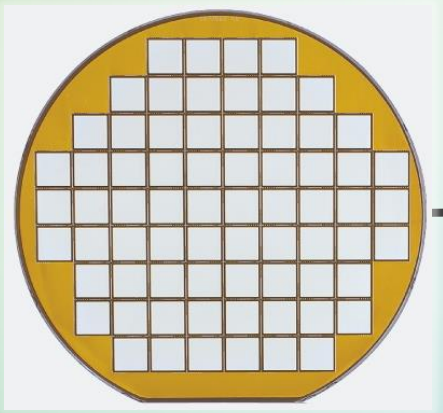
- **Probes Protection**
- **Conclusion**

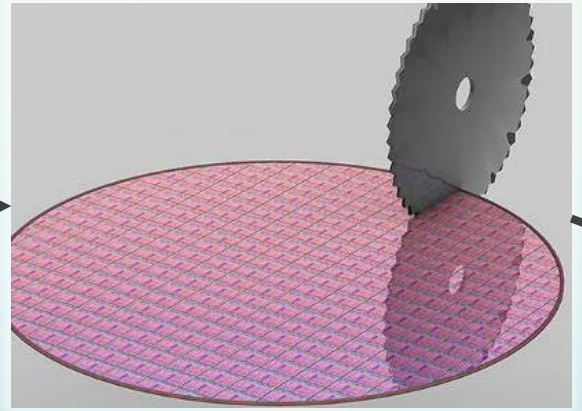
Probes protection

- **Power modules up to 32x**
  - For high module yield, every single diced chip needs to be tested





Wafer tested



Cutting damage,
Dicing yield

➢ ***High power KGD tests***

Probes protection

High Power KGD Tests

- **Various types of chip failures**
  - Some situations are critical for the probe card
    - Shorted D.U.T. within Avalanche test
    - Hot Spot
    - Etc.

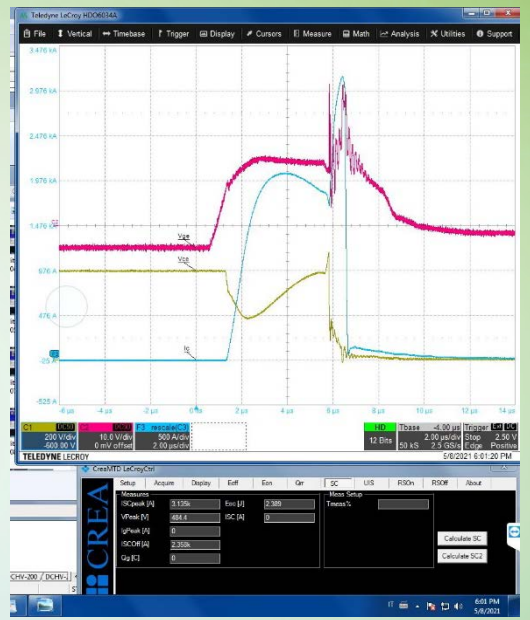
  ➢ ***Overload protection***

- **In general: Need for homogeneous current distribution amongst probes**

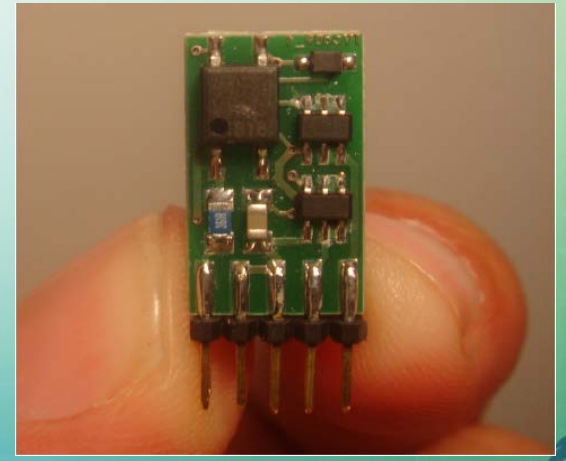
  ➢ ***Active current balancing between probes***

Probes protection

- **Active overcurrent protection**
  - Monitoring and limitation of current which is drawn at each tester channel
    - Realized by *CREA Semiconductor test equipment*

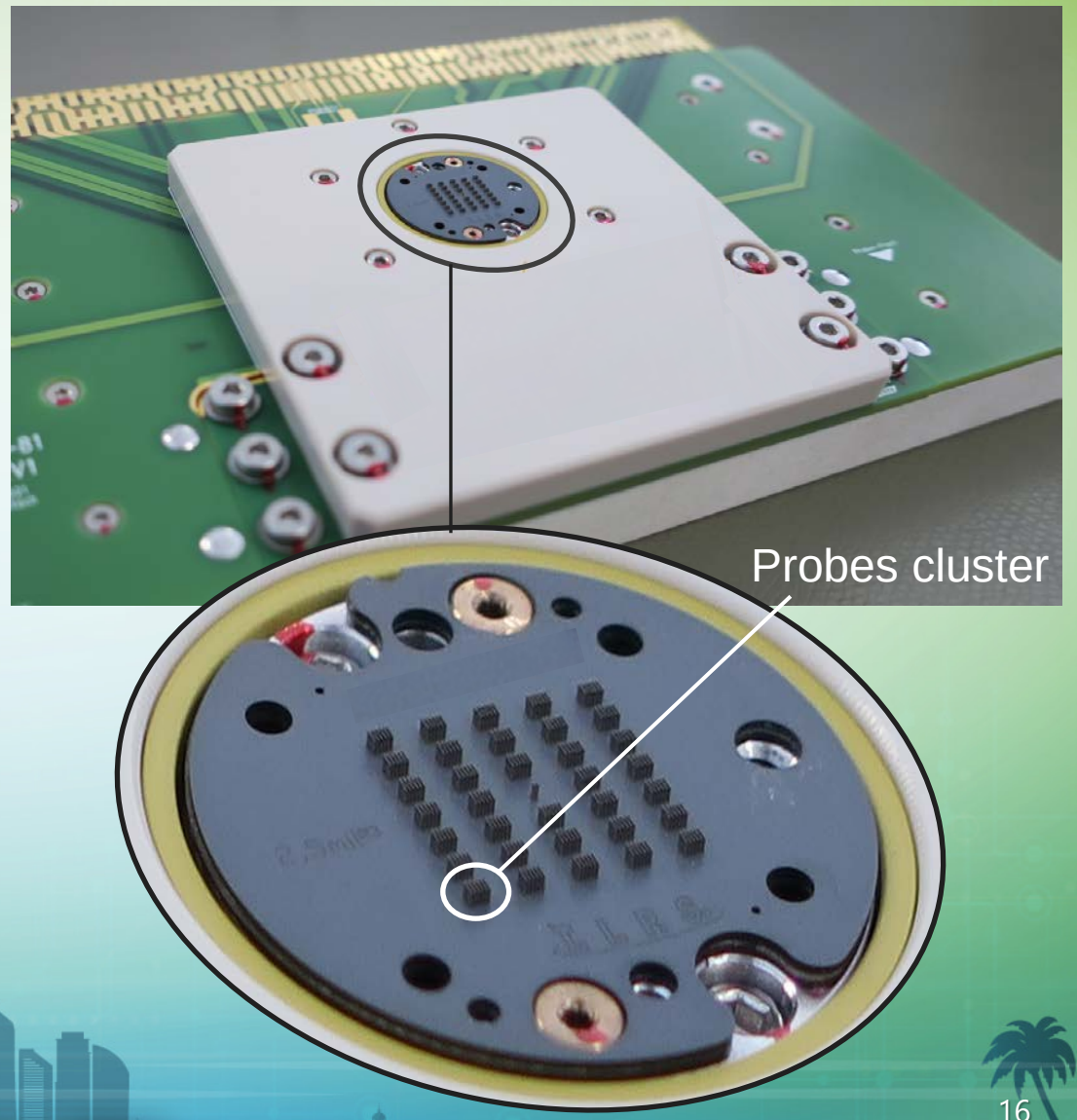


- **Alternative:**
  - T.I.P.S. Smart Clamp Technology
    - Active current balancing/limiting



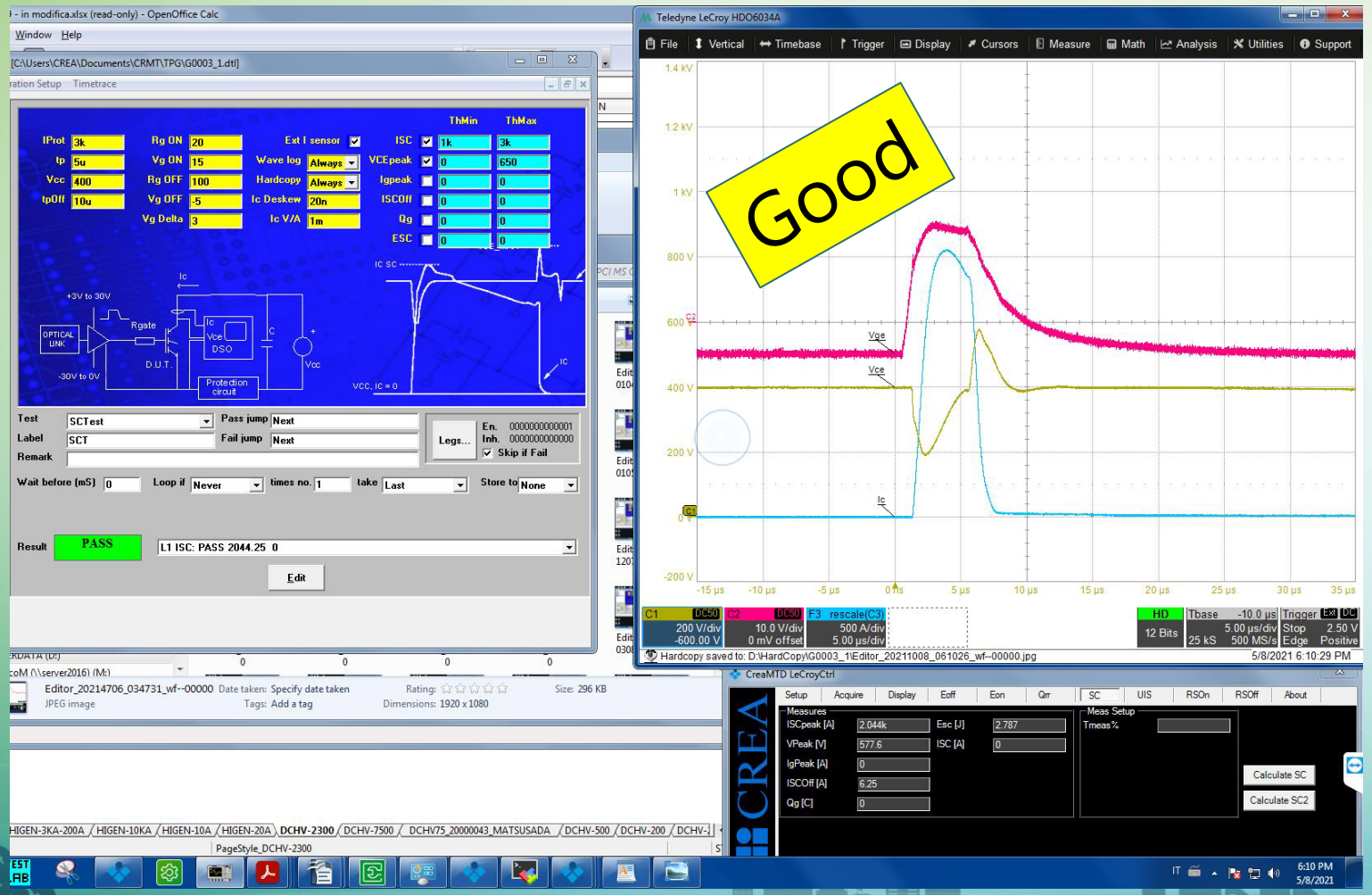
Probes protection

- **Ideal:**
  - Every probe has separate channel to monitor and limit current consumption
    - Not possible with more than a thousand probes
- **Real:**
  - Several probes are bundled to one “cluster”
  - Each cluster is separately monitored and protected (limited)



Probes protection

BENCH CHIP TEST: SCT TEST 5us @150°C 2000A@400V



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- Probes Protection - Overcurrent Protection
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Conclusion

- **Limits for high power KGD application can be pushed further:**
  - Vertical technology is means of choice
  - Overcurrent protection is required to protect probe card in case of chip failure

- **Investigations for higher current densities ongoing**
  - Optimize probes arrangement on chip pads
  - Reduce needle pitch
  - Increase maximum current per probes

Acknowledgement / Q&A

- **Thanks to everybody that was involved**
  - CREA Semiconductor Test Equipment
  - T.I.P.S. Messtechnik GmbH

- **If you need further information please contact:**

  - sebastian.salbrechter@tips.co.at

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