SWTEST 2021 CONFERENCE
PROBE TODAY, FOR TOMORROW

30TH ANNIVERSARY

"Towerless vs Towered Probe Solutions; What is the most effective application for my wafer test interface? "

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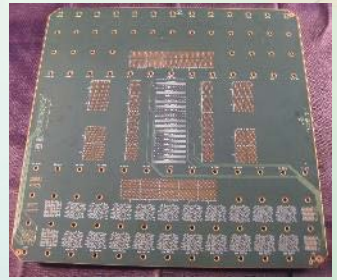
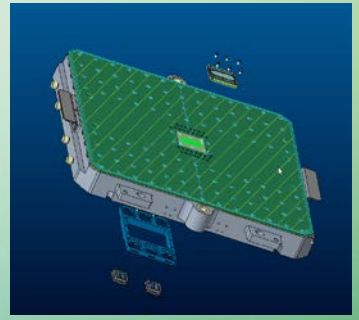
Overview

- Introduction/Glossary
- Objectives
- Towerless Test Cell Advantages
- Towerless Test Cell Disadvantages
- Towered Test Cell Advantages
- Towered Test Cell Disadvantages
- Summary/Conclusion

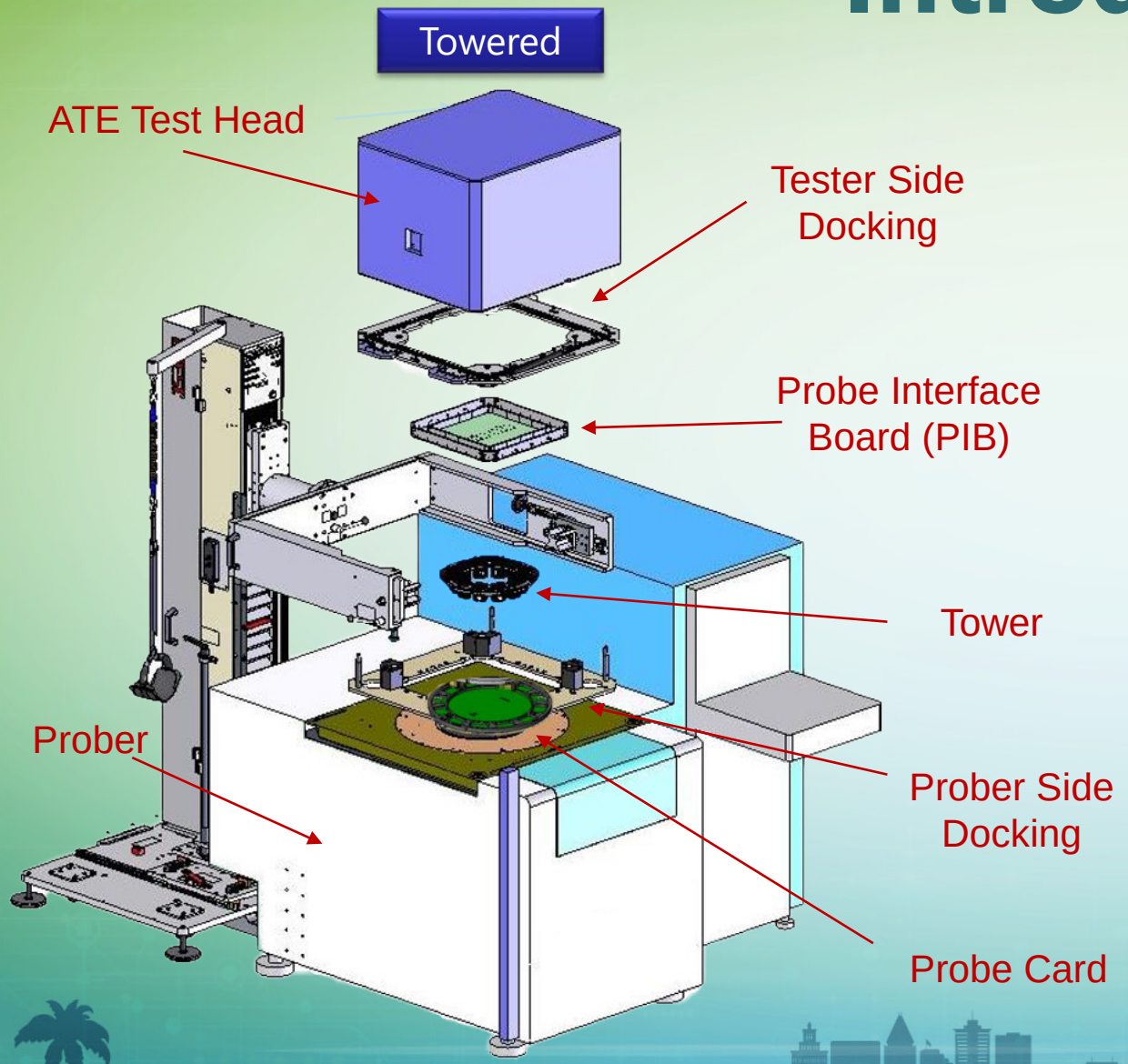
Glossary

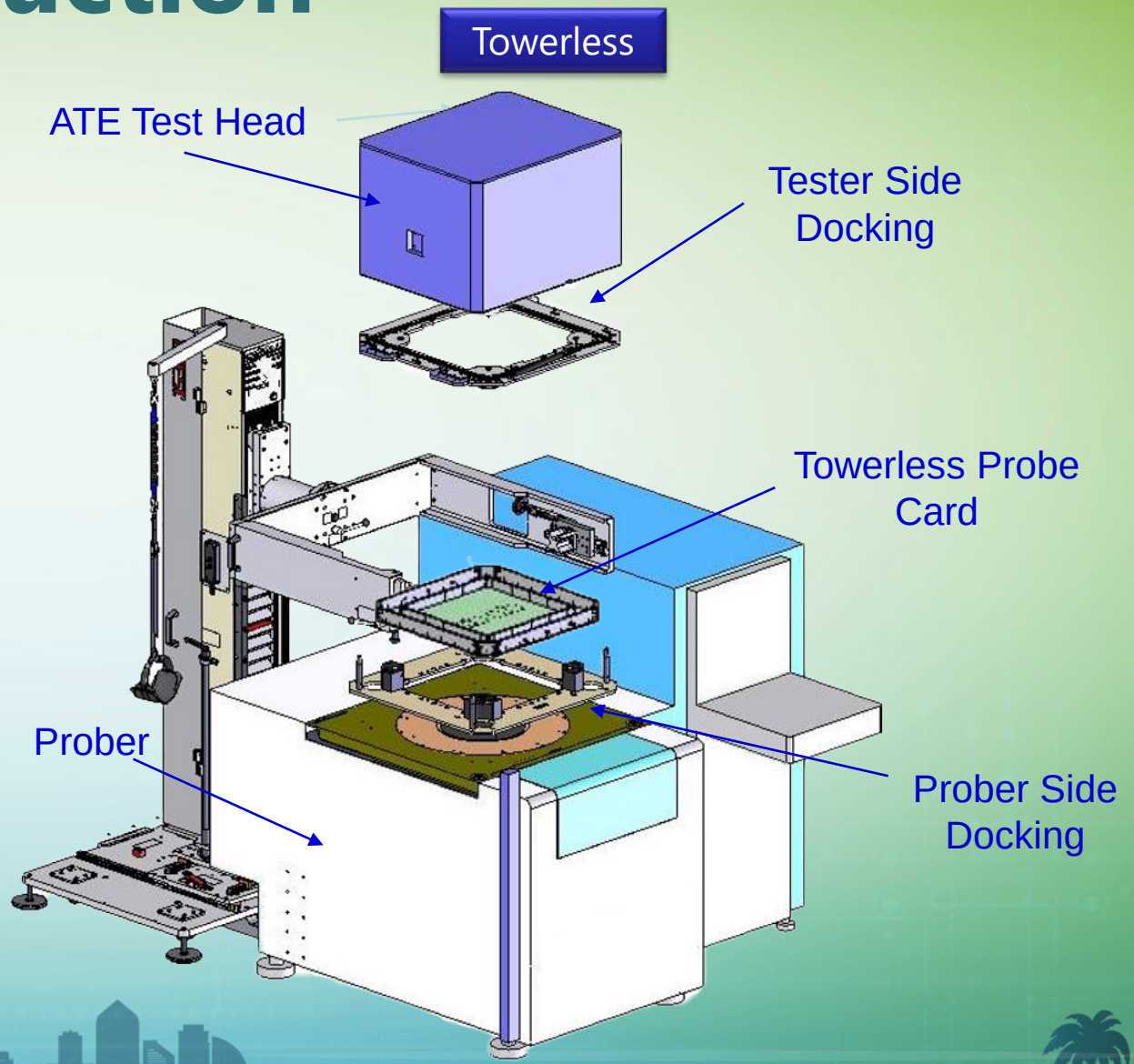
- **Tower ⇔ Pogo Ring ⇔ PPR (probe Pin Ring) ⇔ Interface, etc**
  - Terms for the electrical/physical transition between the PIB and the Probe Card.
- **Towerless ⇔ Direct Dock™⇔ UltraProbe™⇔ PIB Direct:**
  - Terms for the interface that directly mates the ATE to the DUT.
- **PIB (Probe Interface Board):**
  - Printed circuit board used to connect ATE instrumentation to tower connections.
- **Towerless Probe Card.**
  - Integration of PIB and Probe Card.
- **DUT**
  - Device under test.





Introduction



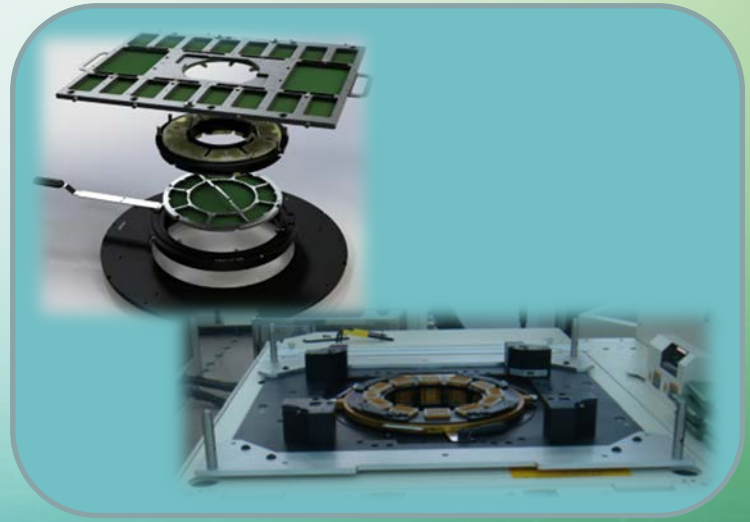


Objective

Identify the Pluses and Minuses of the two approaches

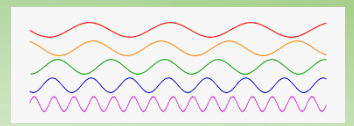
Describe best approaches for different applications

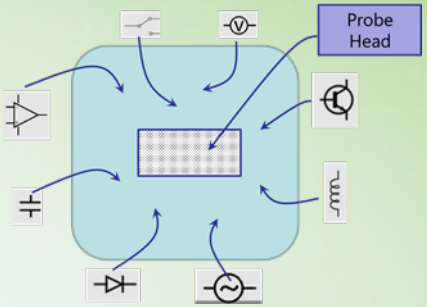
Provide the user with background/data to help choose the right solution.

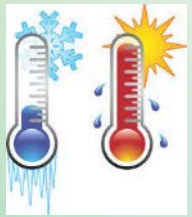


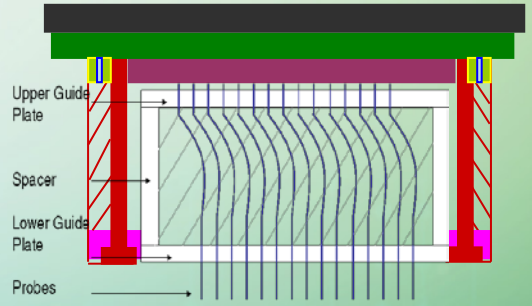
Parameters to Consider

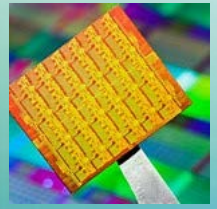
- Data Rates
- Available Application Space
- Probe Tip Depth Compliance
- Devices in Parallel
- Die Size & Contacts
- Environmental conditions
- Etc.

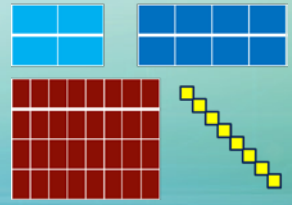








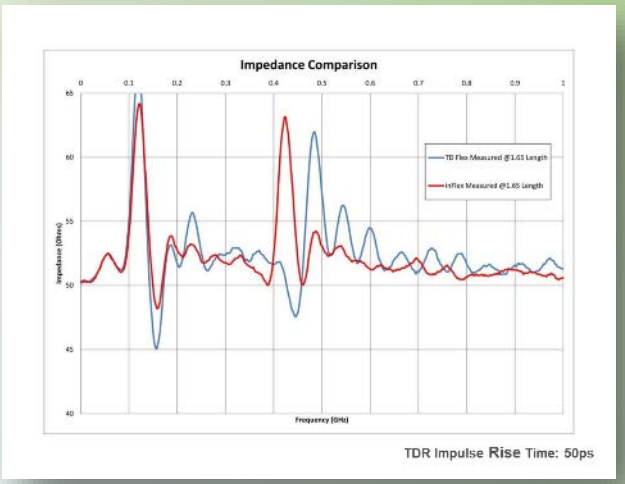




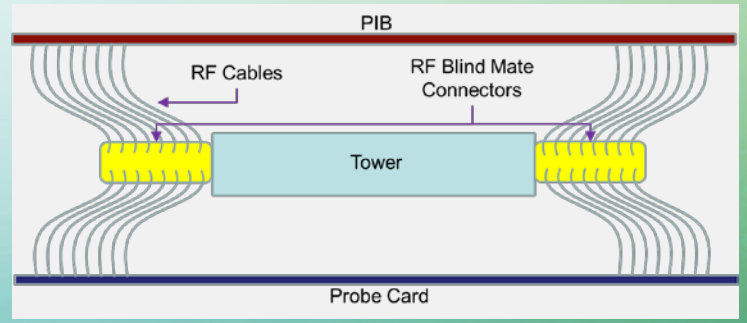
Towerless Test Cell

Towerless Test Cell Advantages

- **Less complex signal path between ATE and DUT**
  - Less impedance discontinuities.
  - Reduces the propagation delay of the signal paths.
  - Decreases the power supply loop area.
  - Faster test times, needed to meet latest RF Specs.
    - For 5G devices, no other choice.



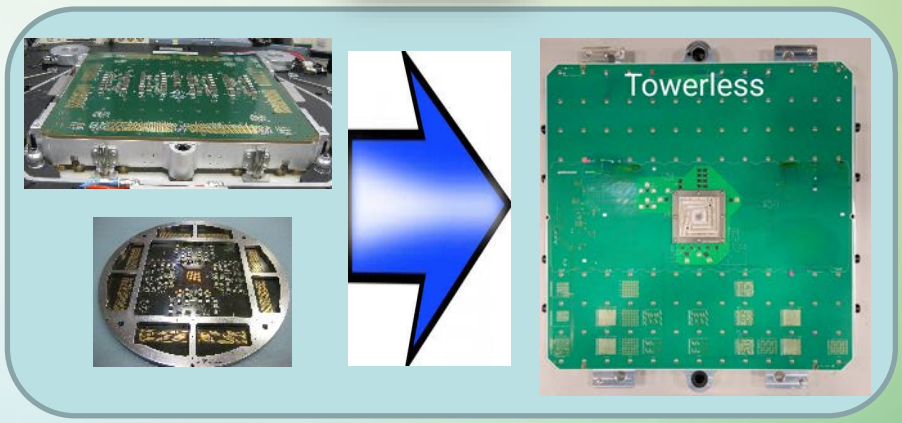
- **RF cable costs/availability**
  - Minimizes the number of RF cables, sometimes by 50%.
    - Lower RF component cost per interface.
    - Minimizes assembly time.



Towerless Test Cell Advantages

- **Lower initial hardware costs**
  - Assume new equipment purchases.
  - No PIB and No Pogo Tower.

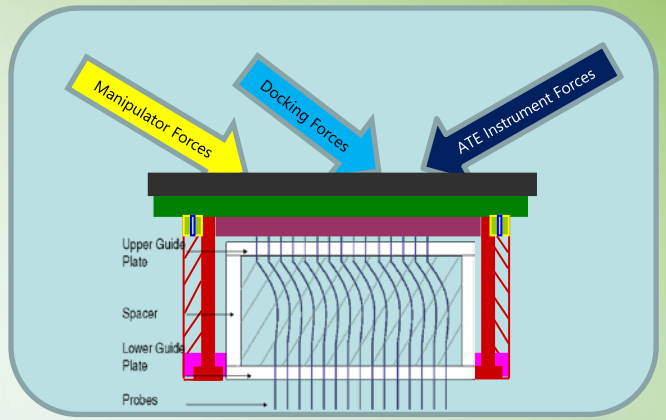
- **PIB becomes probe card (one entity, not 2)**
  - One design effort, not two.
  - If major changes to device design, one design change.



- **Less dependence on probe card debug tools.**
  - When required for software and product debug.
  - For Characterization.

Towerless Test Cell Disadvantages

- **Planarity**
  - The PIB becomes your probe card.
  - Docking, instrument and manipulator mechanical effects could affect probe/die interface and may need to be mitigated.
    - For towered interfaces, these forces are isolated at some level.

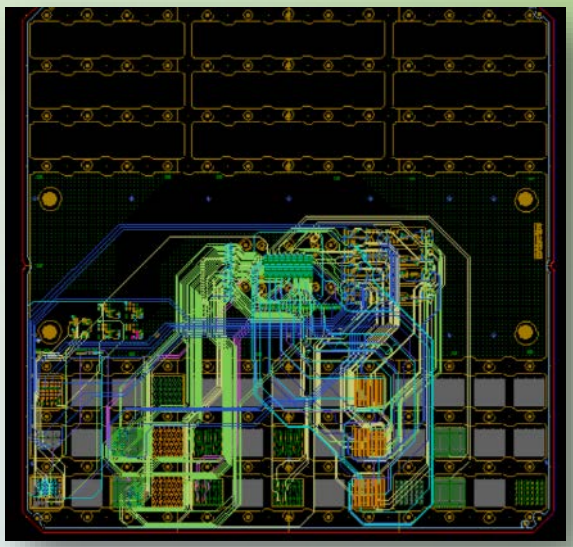


- **Metrology**
  - Unlike towered probe cards, towerless solutions may require custom motherboards for validation.
    - Physical/Electrical performance validation at probe card supplier.
  - Alternative is to validate on the ATE test cell:
    - Downside - $$, Time and Effort.

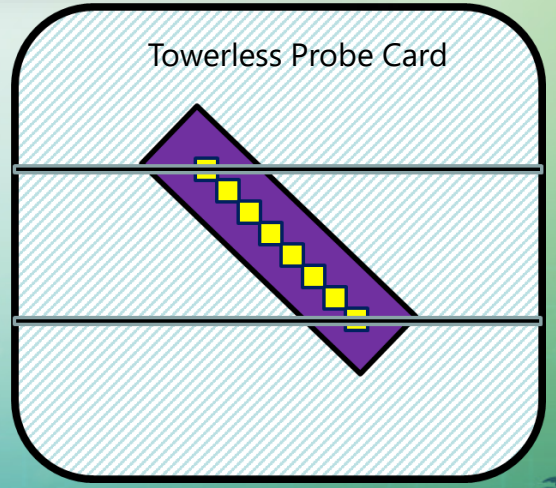
- **Towerless Probe Card PCB designs are more complicated**
  - Requires additional knowledge of ATE instruments.
  - Requires more capable PCB designer, longer development times and higher risks.

Towerless Test Cell Disadvantages

- **Restrictions in layout**
  - Managing component density
  - Specifically for RF designs, more ports creates additional space constraints.
  - Could affect parallelism when balancing RF layout.

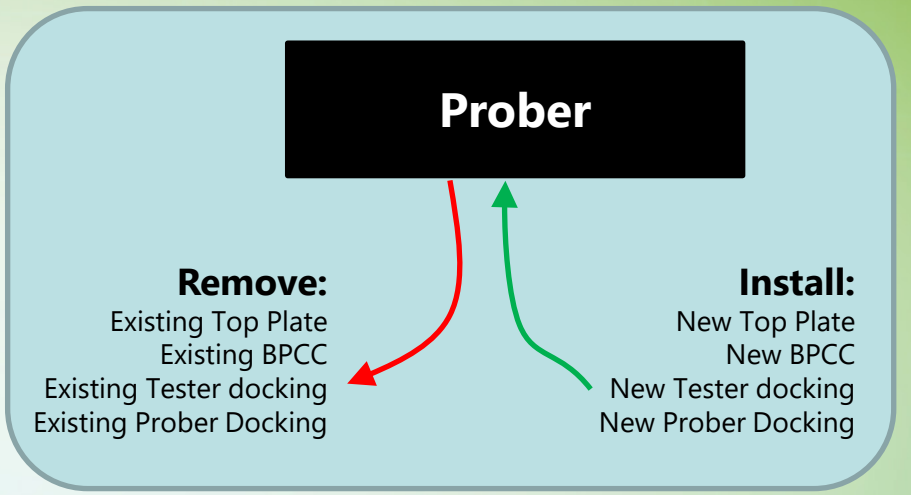


- **Probe head space limit.**
  - With the Application space limited to one PCB
    - High parallel probe head clearance competes with electrical test components and ATE instrument keep out space.
    - Need to balance electrical and mechanical specifications.
    - May require custom/modified stiffeners



Towerless Test Cell Disadvantages

- **Test cell upgrade/conversion cost/time**
  - If you have an existing towered product line,
    - Cost, lead time and effort could be significant.

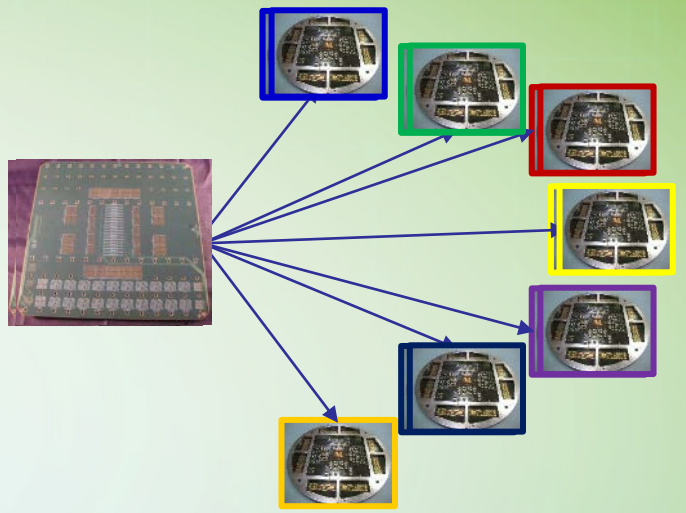


- **Higher Probe Card Cost.**
  - Towerless PCs are usually more expensive.
  - Tight pitch requirements may lead to multi-laminations, space transformers, Micro Vias etc. that increase costs.

Towered Test Cell

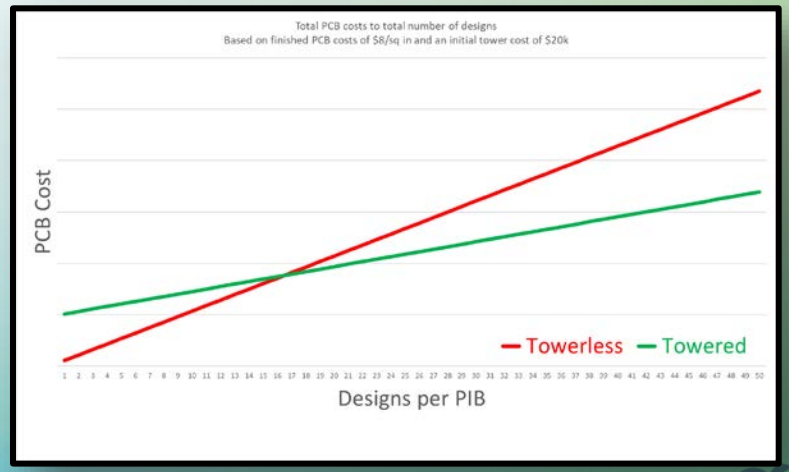
Towered Test Cell Advantages

- **Backwards compatibility**
  - Keeping a Towered solution provides backward compatibility to legacy products.



- **Hi mix scenarios**
  - With a high mix of similar products designed to use the same PIB there is no need to undock the tester when changing products.
    - For Top load setups.

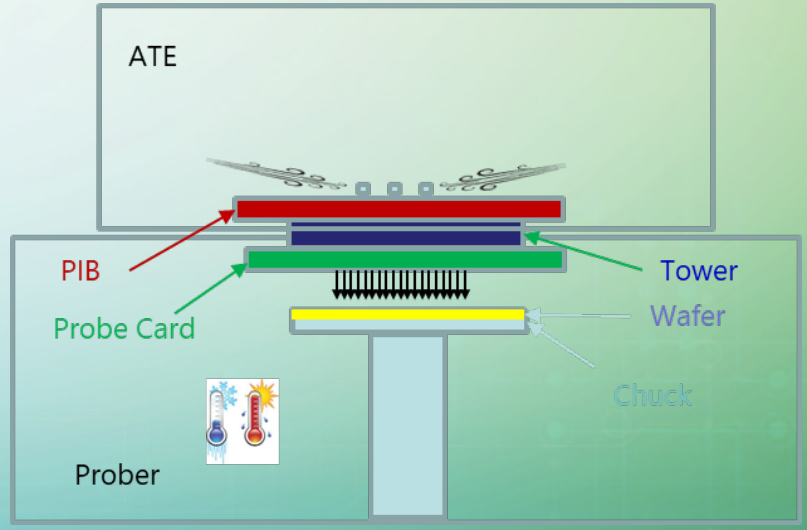
- **Develop known good PIB, reuse as a family board**
  - When designing the complete test solution for a mix of products the PIB can be designed for multiple products.
  - A product line could design a few different PIBs to accommodate a wide mix of products.
  - Debug may be quicker.



Towered Test Cell Advantages

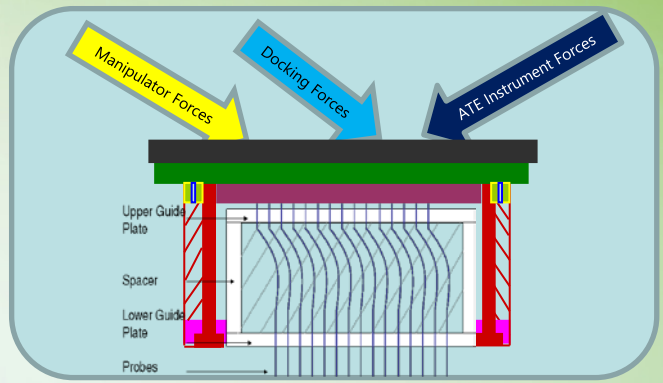
- **Reuse of known good circuits**
  - With a high mix of similar products using the same test circuits, this can be implemented on the PIB and reused.
  - When reusing circuits, debugging is eliminated after the first validation.
  - Expensive parts may be able to be used product to product.

- **Better temperature isolation of key components on the PIB**
  - With standard tester air purge, PIB components placed on the tester side experience closer to Ambient Temps.
  - Towered Probe card setups have smaller openings between tester and probe chamber creating a better seal.

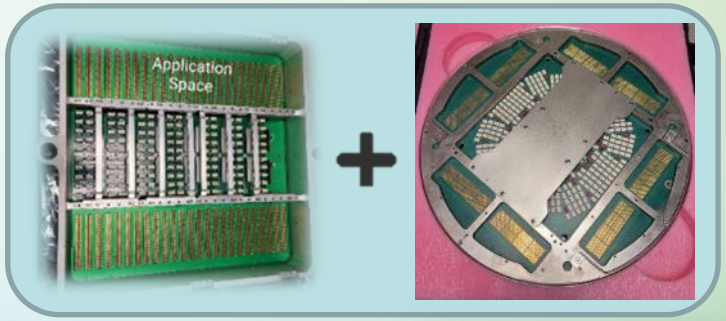


Towered Test Cell Advantages

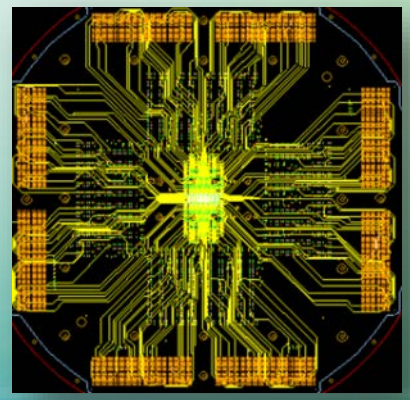
- **Planarity**
  - Pogo tower isolate tester instruments loading on probe head.
  - Docking, instrument and manipulator mechanical effects have less affect on the probe/die interface.



- **More apps space.**
  - Have the combined apps space of 2 PCBs.
  - Allows for higher parallel site count.

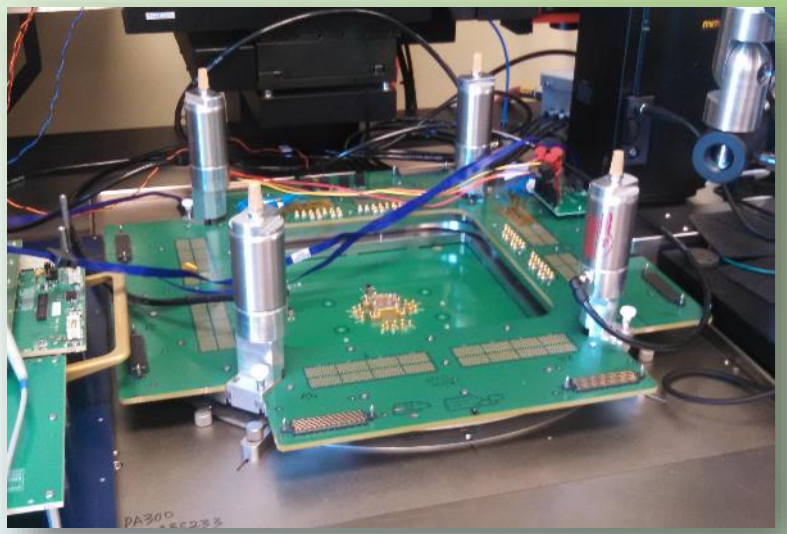


- **Towered solution allows symmetric signal routing to the probe area.**



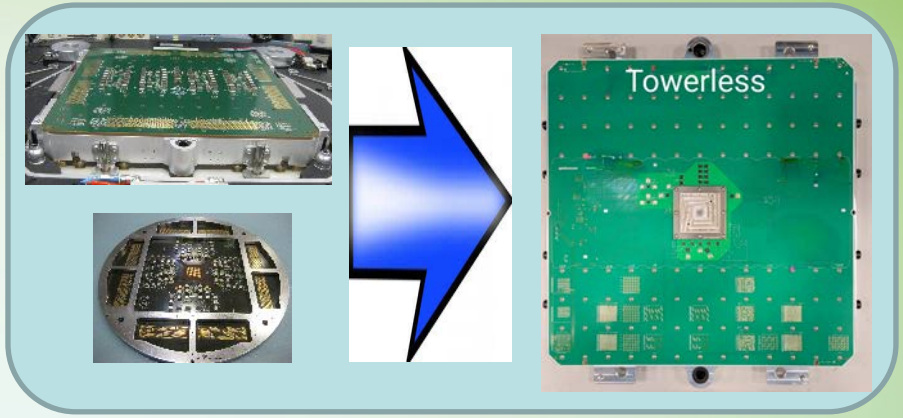
Towered Test Cell Advantages

- **Can use the same probe card on different ATE platforms.**
  - Including Bench equipment,
  - Would require planning in developing the PIB.



Towered Test Cell Disadvantages

- **For a new tester/config, now need to design 2 PCBs (PIB and Probe Card).**
  - When starting a new product line or tester config both the PIB and probe card need to be designed.



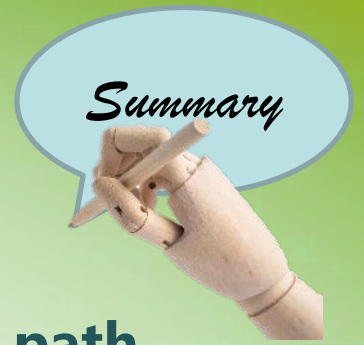
- **As port and site counts grow, RF cabling becomes complex and challenging.**
  - Cabling needs to route through the PIB creating less vertical space for dressing cables neatly.

Towered Test Cell Disadvantages

- **Damage to Pogo Towers possible**
  - No different than ATE instruments and probe head interfaces.
  - Standard care and maintenance required.

- **Will need separate debug hardware to debug off the prober.**

Conclusion



- **There is no perfect "one size fits all"**
- **Your specific parameters/requirements will influence the most efficient path.**
- **Once you venture down a path, redirection will cost you significant time, money and risk.**
- **This paper is not intended to chose your path.**
  - Just provide you with the background to chose the path best for your test solution.
- **At first look, the Towerless Probe card sounds like a less costly higher performing option, but when taking into consideration the overall potential use case for an individual product line it could be more cost effective and less time consuming to use the towered solution.**
- **Hopefully, this helps some of you work through the advantages/disadvantages of each, to assist in choosing most optimal solution for you.**

Thank You!