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30TH ANNIVERSARY

Probe to pad alignment improvement over wide temperature range for automotive applications with large probe array size, high parallelism and small pads size

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Summary

- **Introduction**
  - Probe card thermal expansion behavior: theory and experiments
- **HCTE probe card solution development**
- **Trials on the field**
  - Probe card configuration
  - Probing setup & Trials description
  - Data collected
    - Probe marks optical inspection
    - Probe marks position analysis (Automatic Visual Inspection)
- **Conclusions**
- **References & Acknowledgements**

Probe card thermal expansion behavior

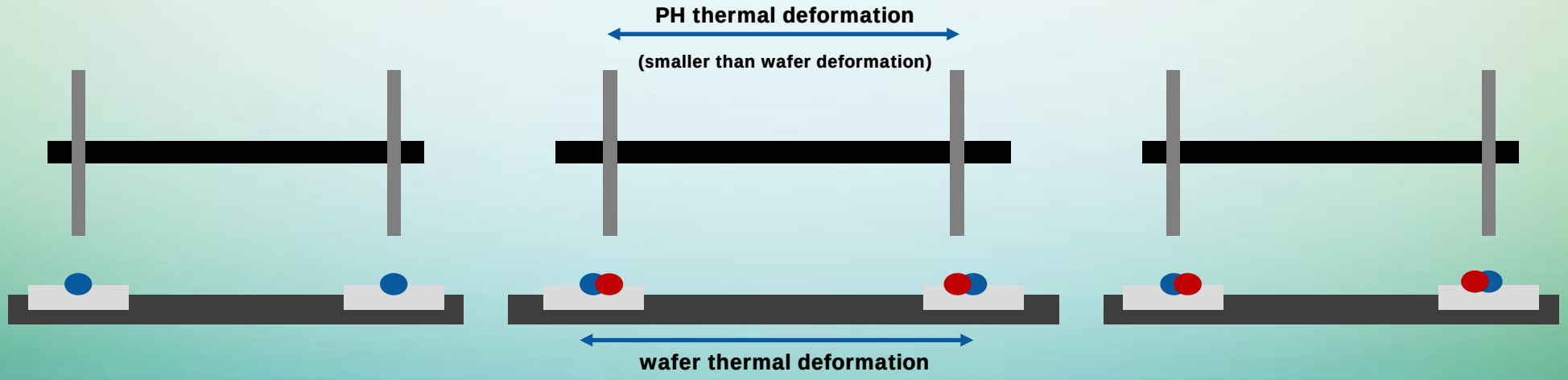
- **As widely known and broadly discussed in literature (examples are refs [1] and [2]), probe to pad alignment is *a challenge* for wide temperature range & large arrays**

- **Wafer**
  - After loading on chuck, it reaches chuck temperature rapidly (~ seconds) and uniformly (low mass & low thickness compared with wafer chuck)
  - Wafer size immediately changes according to the coefficient of thermal expansion (CTE) of Silicon

- **Probe card**
  - Adapts over much longer time scale (~ minutes/hours)
  - Probe head "size" (= distance between probe tips ad the edge of array) change according to
    1) **Temperature field & stabilization** of probe card→ Full soak time needed to work *near equilibrium*
    2) **Equivalent CTE of probe card system**

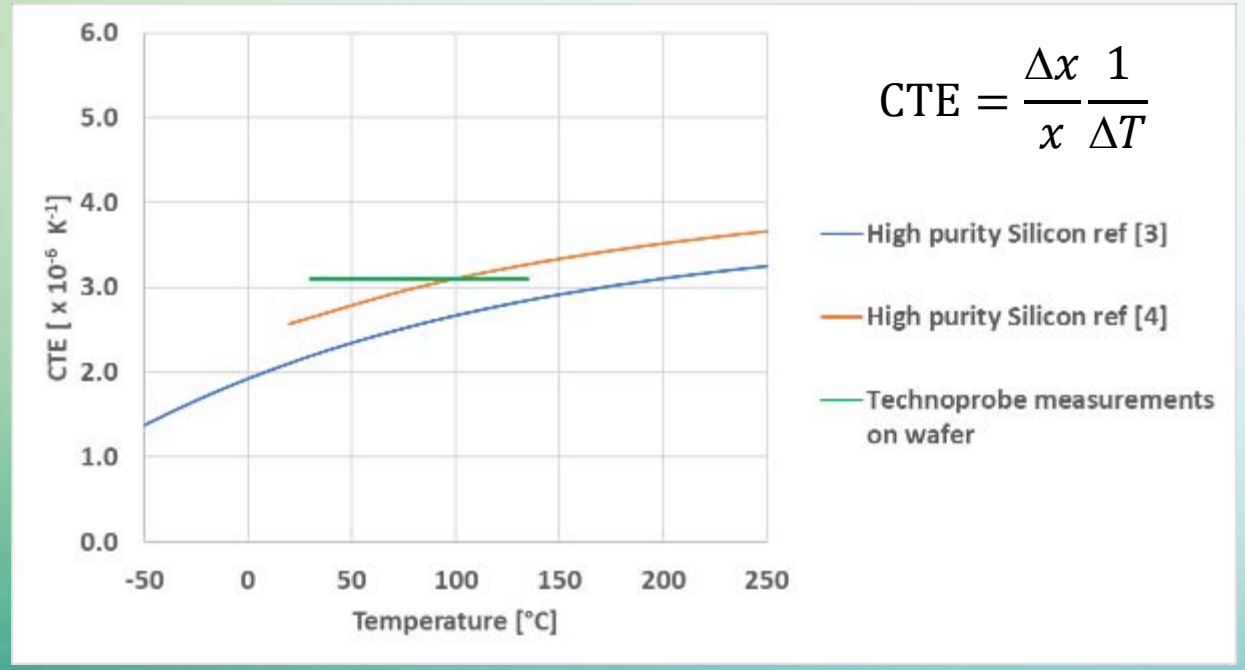
Probe card thermal expansion behavior

- **The resulting phenomenon is a probe mark shift**
  - It is due to different planar thermal deformation of test structure array located on wafer (pads, bumps, …) compared to probe array located on the probe head
  - Wafer is expanding more than probe array due to different CTE and different Temperature of parts
  - Considering a correctly aligned PC, the error is zero at array center and proportional to the distance from center → Error is relevant for large PHs and/or small probing area and/or extended temperature range



Probe card thermal expansion behavior

- **Wafer behavior**
  - Average CTE in the interval from 30 °C to 135 °C is measured on wafer
  - Distance measurement of reference marks on wafer surface is executed after 15 min of stabilization time on chuck, with UF3000ex prober using prober camera

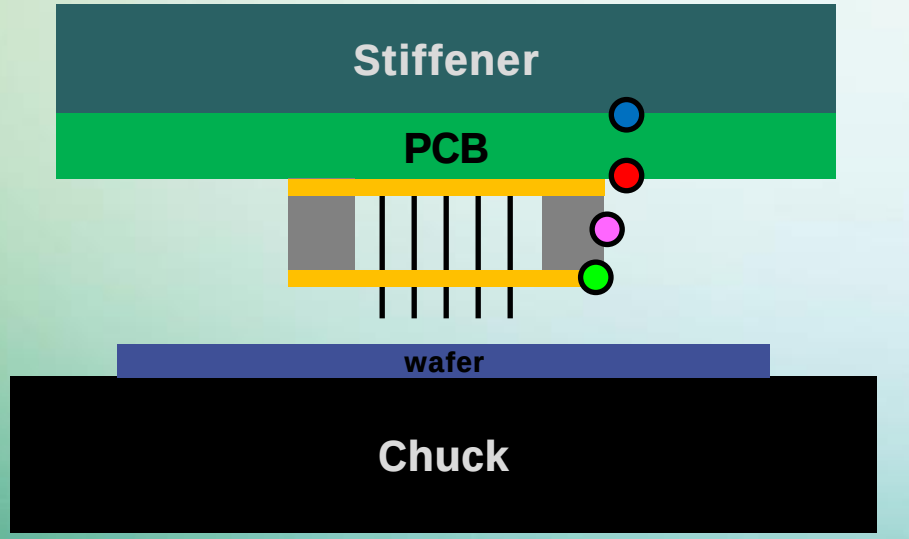


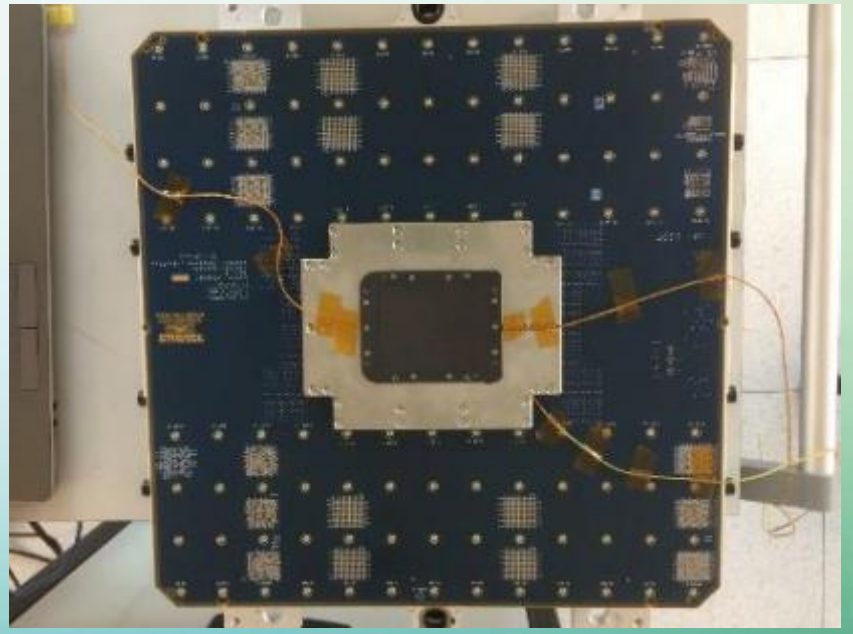
$$\mathrm{CTE} = \frac{\Delta x}{x}\frac{1}{\Delta T}$$

	$x_{30°C}$	$\Delta x_{30\rightarrow135°C}$	CTE
Ref. distance 1	190171 µm	61 µm	$3.05 \cdot 10^{-6}$ K^{-1}
Ref. distance 2	191765 µm	65 µm	$3.23 \cdot 10^{-6}$ K^{-1}
Ref. distance 3	190160 µm	63 µm	$3.16 \cdot 10^{-6}$ K^{-1}
Ref. distance 4	191850 µm	66 µm	$3.28 \cdot 10^{-6}$ K^{-1}
AVERAGE	-	-	**$3.18 \cdot 10^{-6}$ K^{-1}**

Probe card thermal expansion behavior

- **Probe card behavior**
  - Measurements of temperature in selected probe card locations on internal test vehicle based on Ultraflex DD platform, on prober without test head docked
  - Different probe to wafer clearance applied during soak time

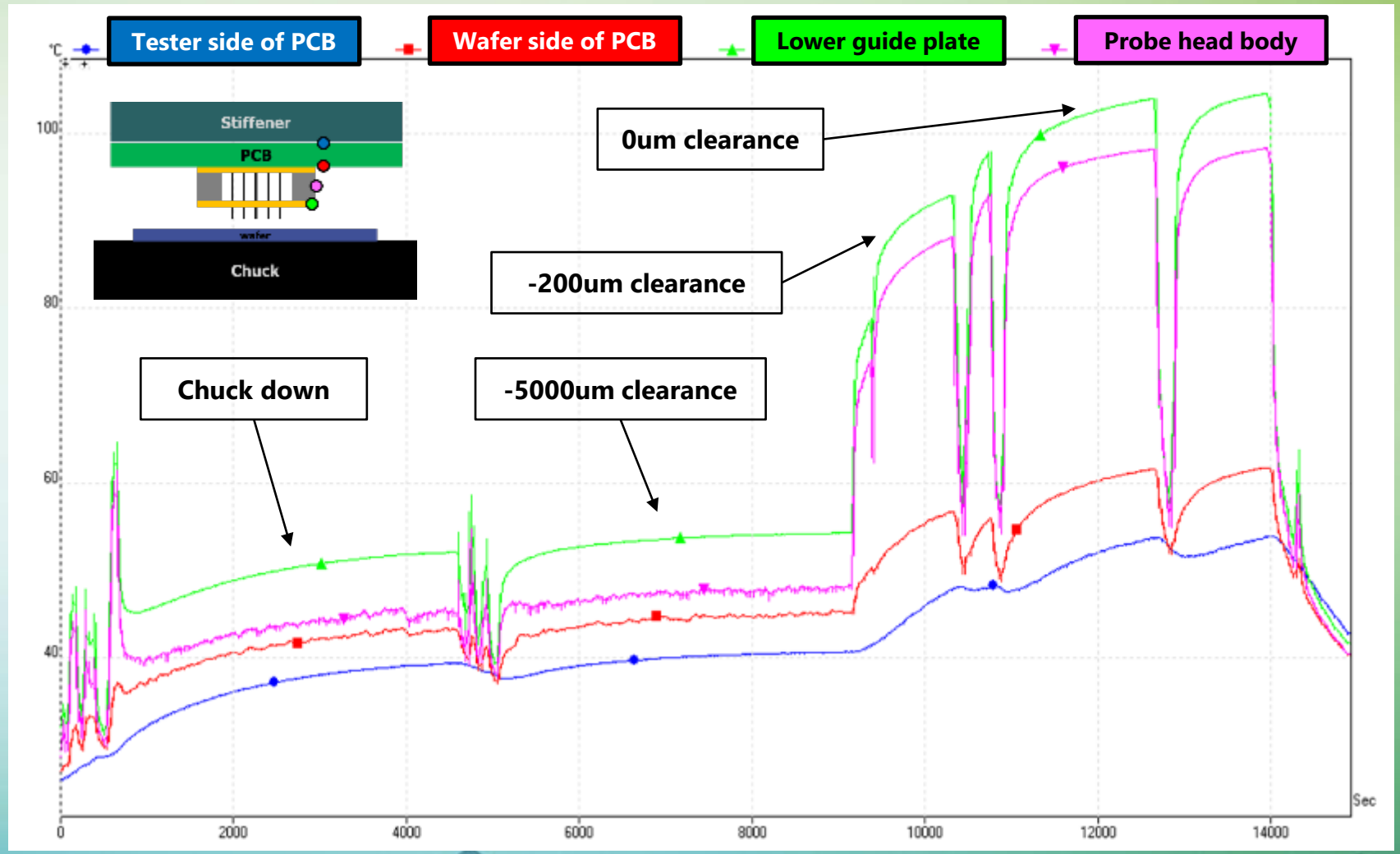




Probe card thermal expansion behavior

- **Probe card behavior**
  - Chuck temp = 135 °C
  - Measurement sites
    - Lower guide plate
    - Probe head body
    - Wafer side of PCB
    - Tester side of PCB

1) Temperature gradient is present inside the whole probe card
2) Also assuming a full soak time is executed, probe guide plates do not reach chuck temperature



HCTE probe card solution development

- **In vertical probe cards, guide plate material is playing a major role controlling probe tip position at different temperatures**

→ **Guide plate material selection is key**

- **But** considering that
  1. Temperature gradient is present inside the whole probe card when probing at T ≠ T_room
  2. Several different materials are used to build the probe card system and interact, each one with its set of thermomechanical properties including a specific CTE
  3. Probe guide plates do not reach chuck temperature (T_GP < T_chuck)

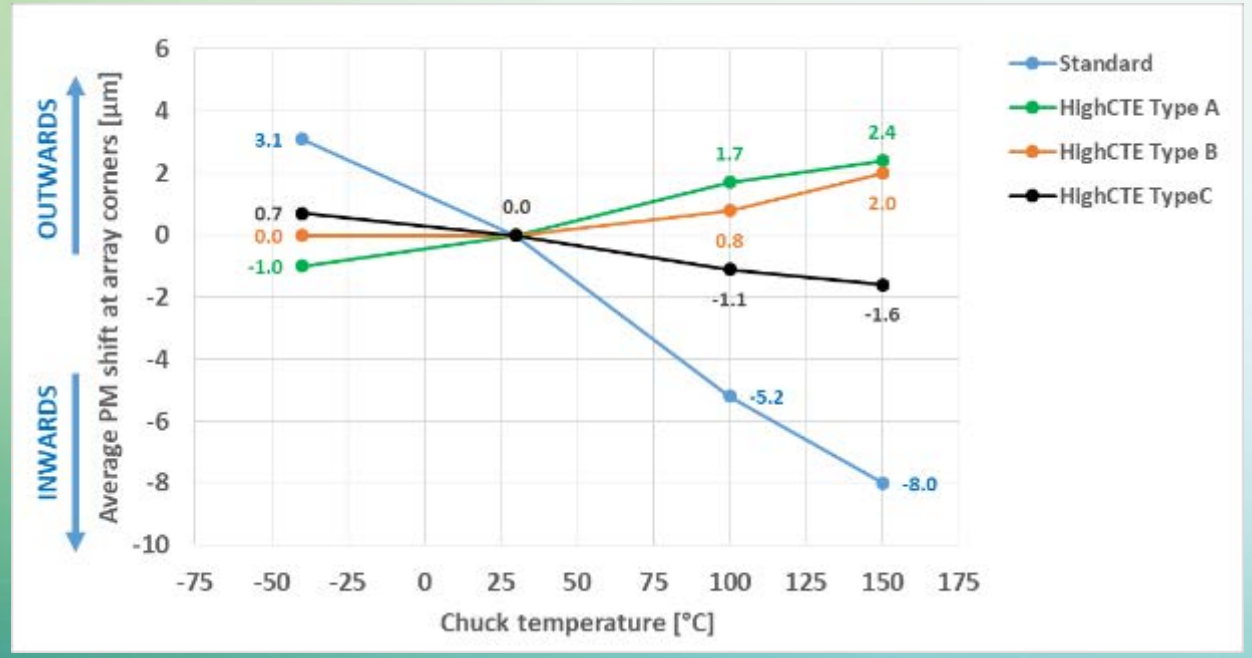
→ **A wide temperature range probe card architecture capable to match wafer thermal dilatation is required**

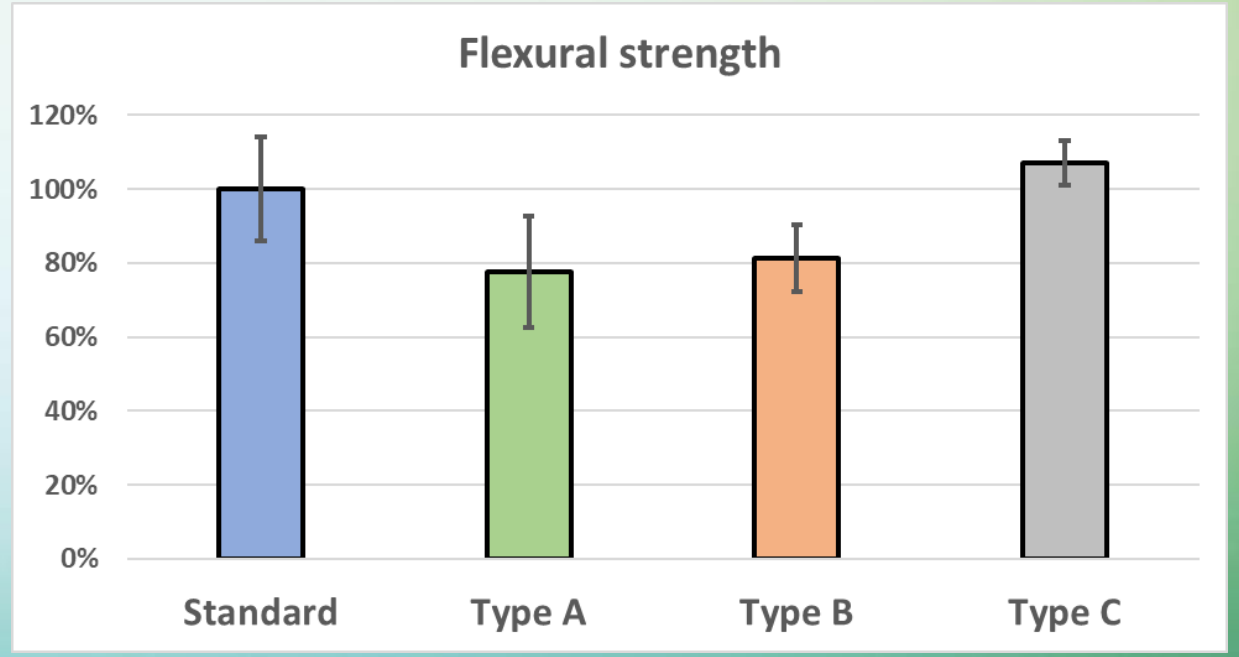
HCTE probe card solution development

- **Guide plate material selection: Technoprobe solution**
  - A new ceramic material with CTE higher than the wafer under test ("**HCTE**") has been implemented to achieve probe mark shift compensation
  - To this aim, different material formulations are considered and characterized in terms of
    - Physical properties (density and porosity)
    - Mechanical properties (mechanical strength, stiffness)
    - Electrical properties (resistivity)
    - Thermal and thermo-mechanical properties (thermal conductivity, CTE)
    - Laser machinability (holes quality, walls quality, drilling process time)
    - Surface finishing and appearance (surface roughness, color and reflectivity)

HCTE probe card solution development

- **Guide plate material selection: Technoprobe solution**
  - PM shift in the range -45 °C to +150 °C is assessed
  - Internal test vehicle: ~4k probes, ~90 mm array diagonal
  - Method: PM executed on Accretech UF3000ex on blank wafer after full soak time



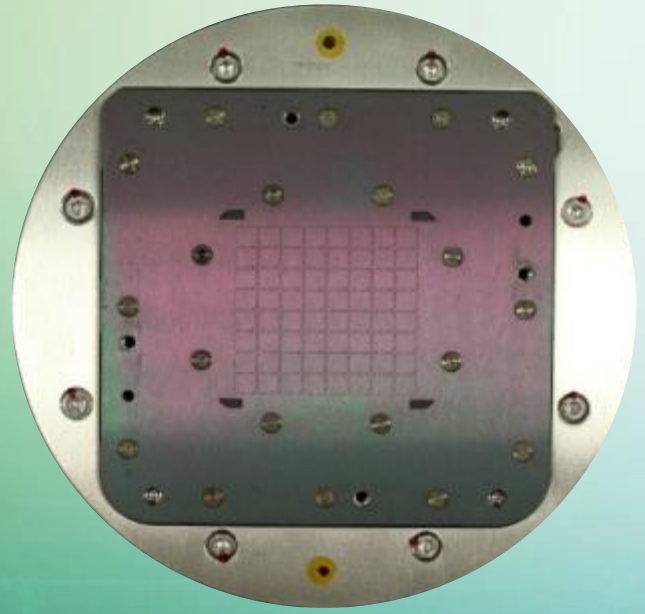


HCTE probe card solution development

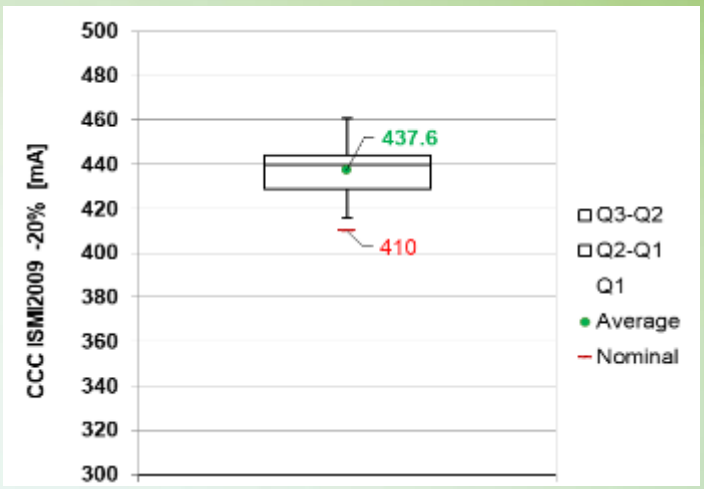
- **Guide plate material selection: Technoprobe solution**
  - Type C HCTE material has been finally qualified
    - Physical, electrical and mechanical properties are aligned with Standard material
    - Thermo-mechanical properties are matching improvement targets
    - Laser machinability with high quality is verified
    - Surface finishing and appearance are matching requirements
  - Probe head architecture is optimized to accommodate it
- **HCTE architecture can be applied to all vertical probe technologies in Technoprobe portfolio**

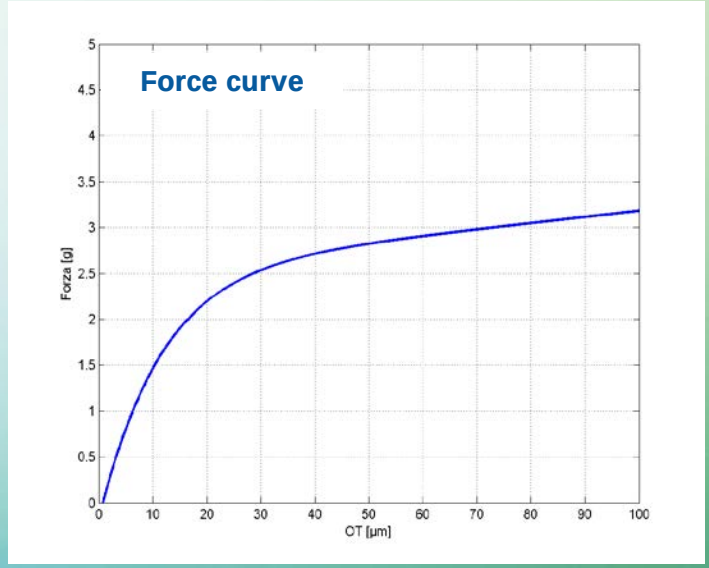
Probe card configuration

- **Technology : TPEG™ T1 TA**
- **Parallelism : // 64**
- **Array size : 35x36.6 mm**
- **Pad Size : 41x49 µm**



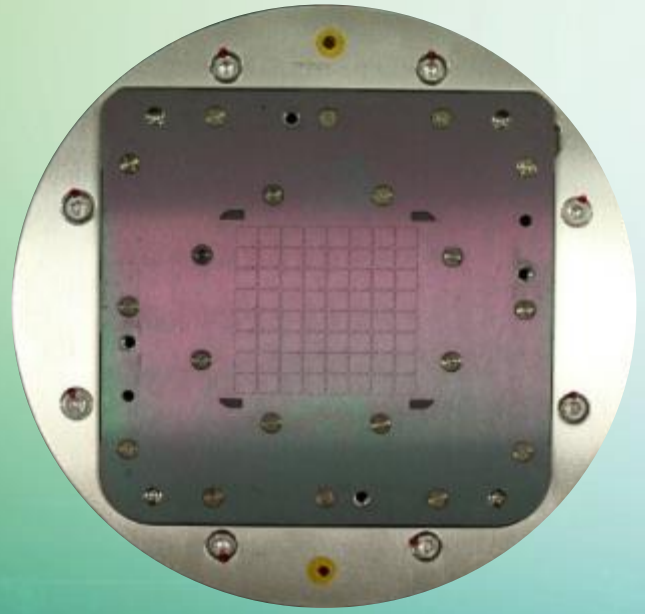
TPEG™ T1 TA specifications	
Radial alignment capability	6 µm
Z planarity capability	Δ = 20 µm
Min pitch	60 µm linear 80 µm full array
Pin Current (CCC)	410 mA
Force (at 75 um OT)	3.0 g
Temperature range	-45 °C / +175 °C
Probe alloy	LCR2
Tip diameter (typical)	9 ± 3 µm

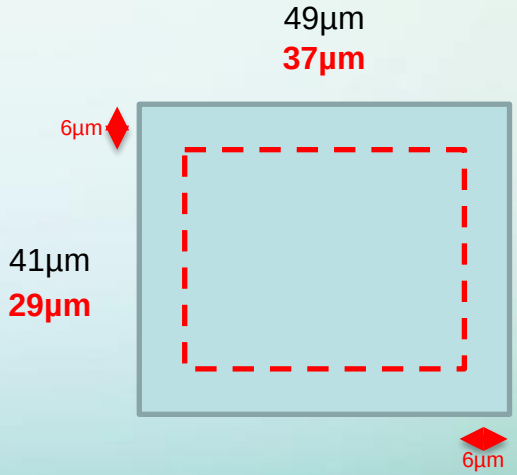




Probe card configuration

- **Technology : TPEG™ T1 TA**
- **Parallelism : // 64**
- **Array size : 35x36.6 mm**
- **Pad Size : 41x49 µm → Band guard = 6 µm → Allowed probing area reduced to 29x37 µm**



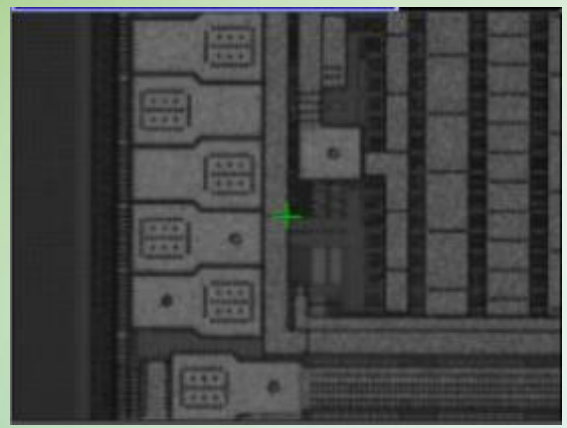


Probing setup & Trials description

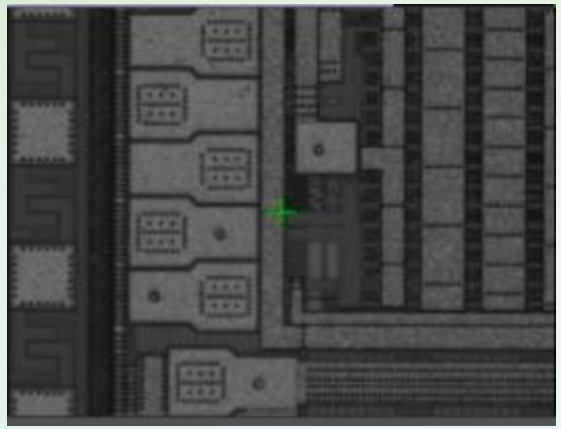
- **Prober: TEL PRECIO**
- **Comparison of probe Standard & HCTE probe heads, swap on same board**
- **Testing temperatures:**
  - Trial 1: +150 °C
  - Trial 2: +90 °C
  - Trial 3: +30 °C
  - Trial 4: – 45 °C
- **Soak time procedure:**
  1. 2h stabilization (probe card loaded, wafer on chuck)
  2. 45min probe card preheat
- **Data collection:**
  - Single TDs for each temperature is executed after automatic PTPA
  - Probe mark pictures captured from corned DUT
  - AVI : All probe marks positions measured for all sites for each test and analyzed

Trial 1 : 150° STD vs HCTE

S1

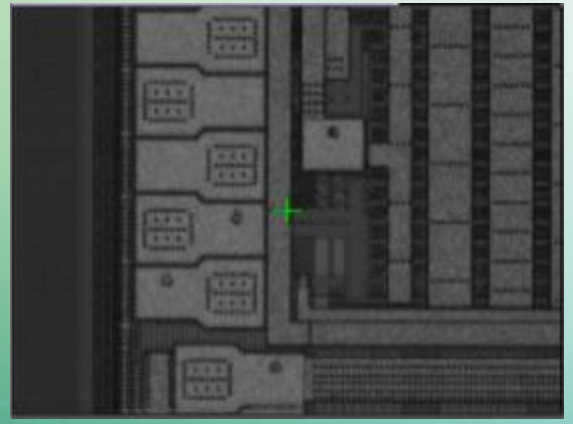


S8



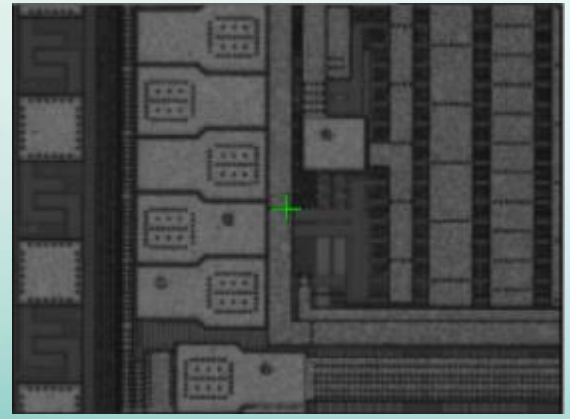
S64

STD

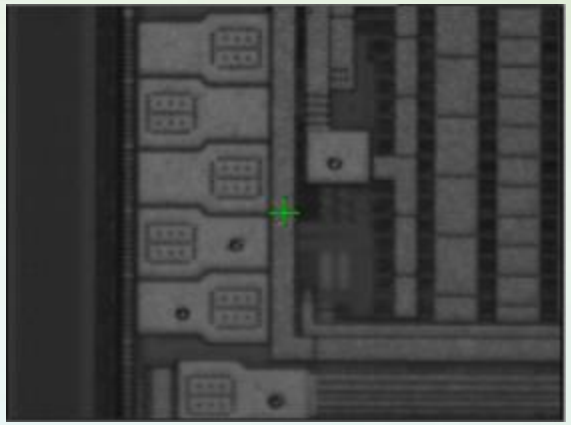


S57

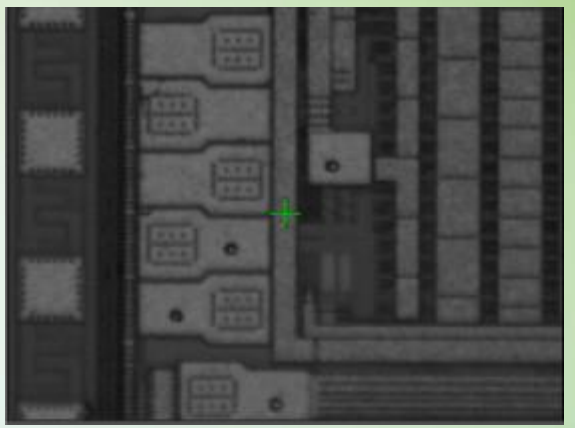
STD



S1

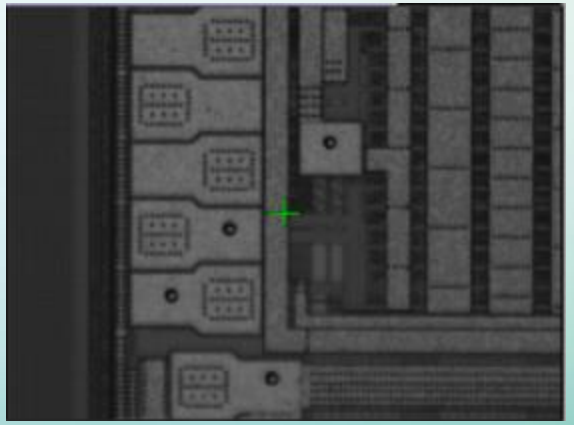


S8



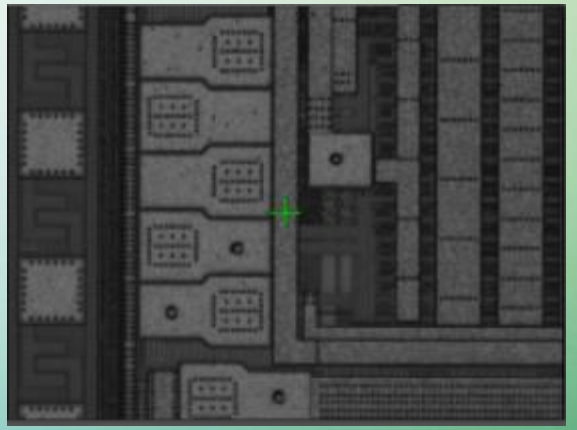
S64

HCTE



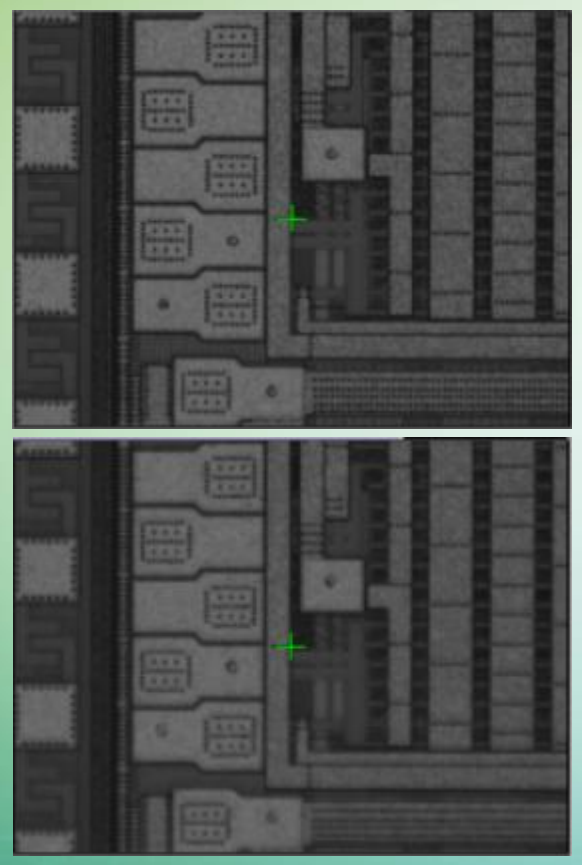
S57

HCTE



Trial 2 : 90° STD vs HCTE

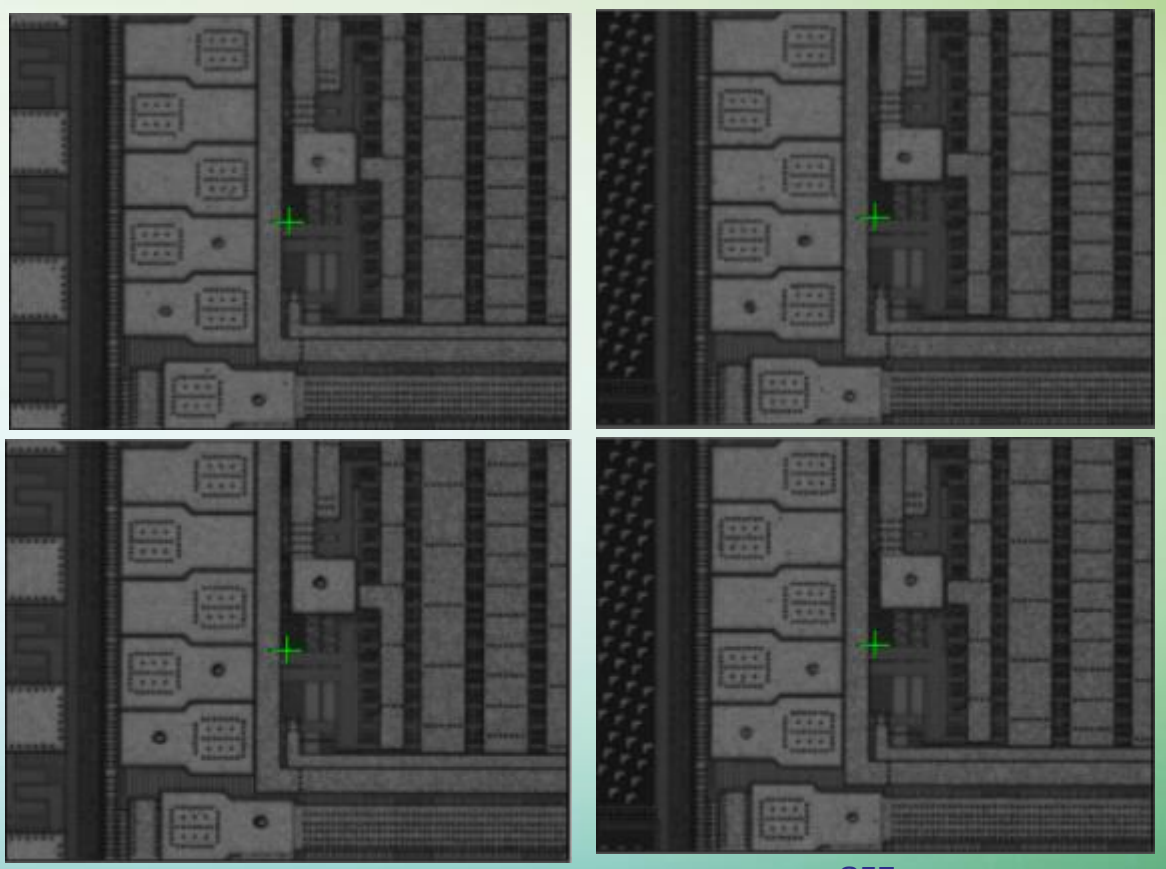
S1 S8



S64 STD

S57 STD

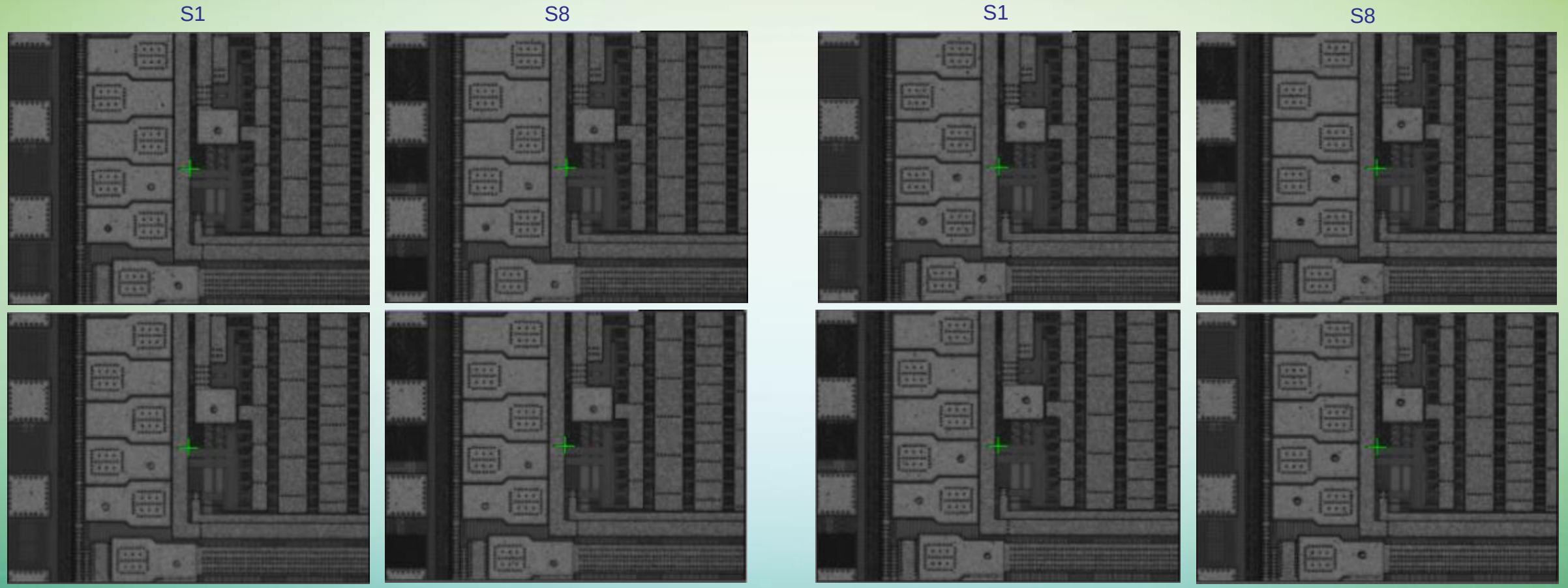
S1 S8



S64 HCTE

S57 HCTE

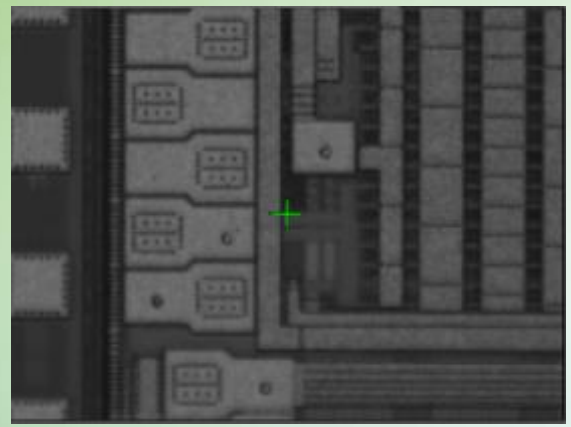
Trial 3 : Test @ 30° STD vs HCTE

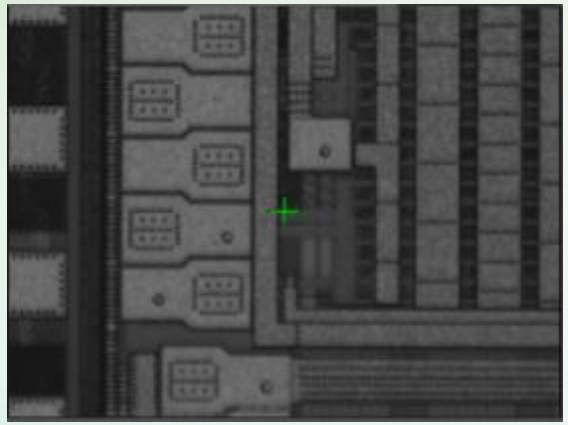


Trial 4 :Test @ -45° STD vs HCTE

S1

S8





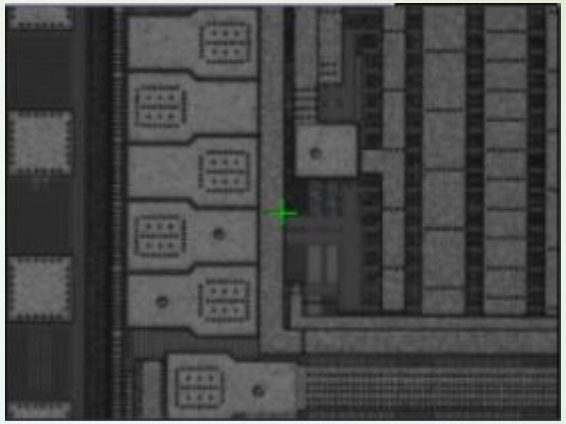
S64

STD

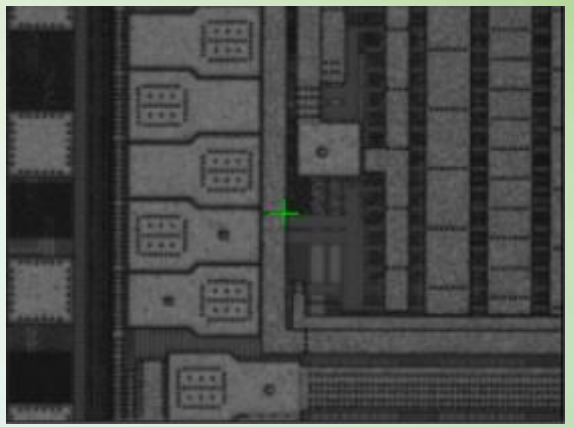
S57

STD

S1

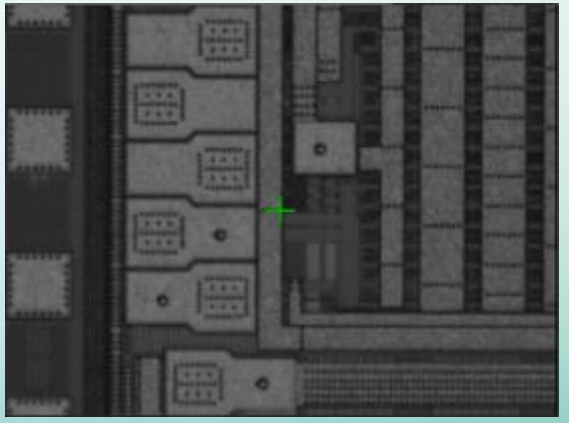


S8



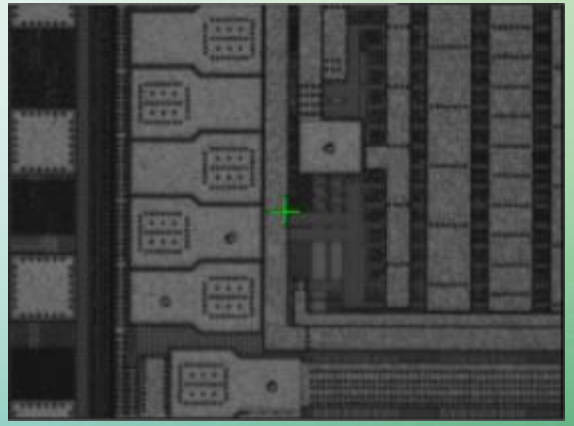
S64

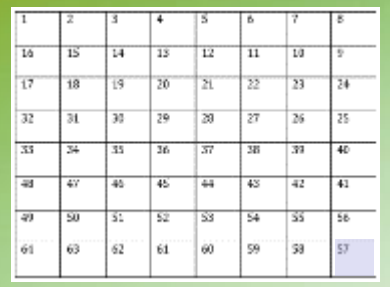
HCTE



S57

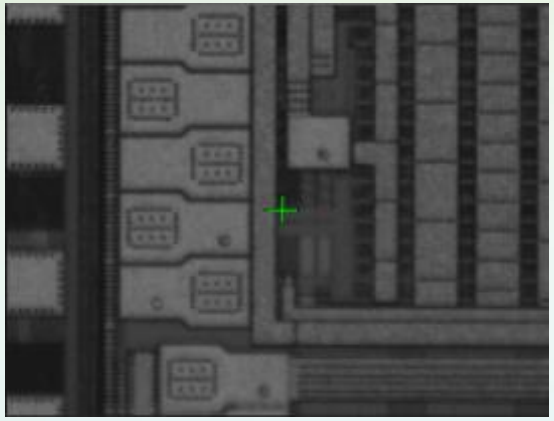
HCTE



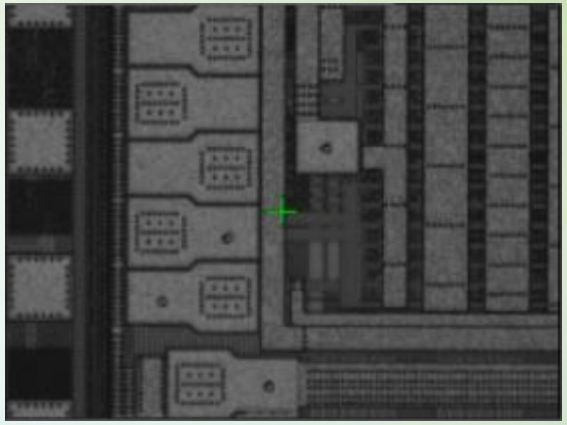


Analysis : Focus on site 57

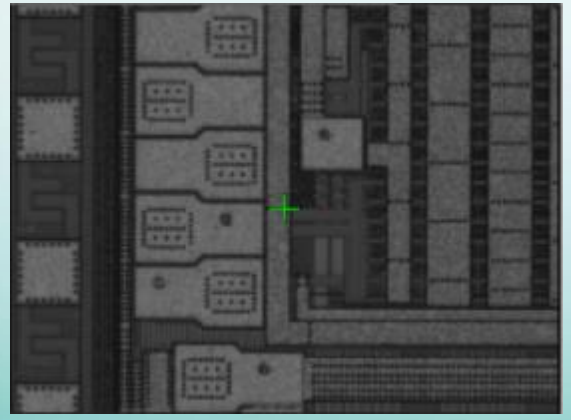
At -45°c probehead STD does not retract enough



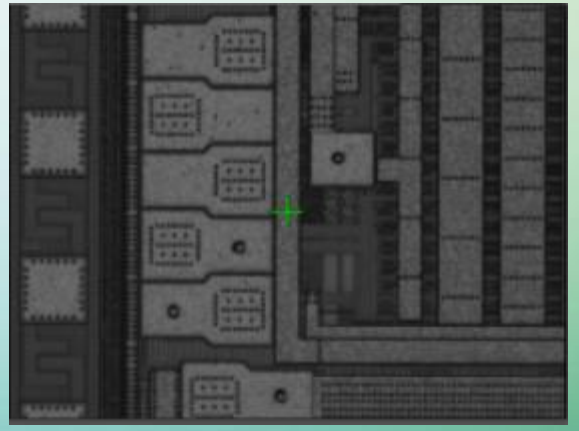
-45°



At 150°c probehead STD does not expand enough

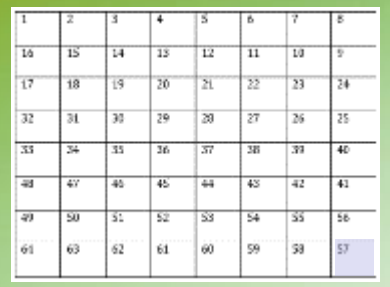


150°



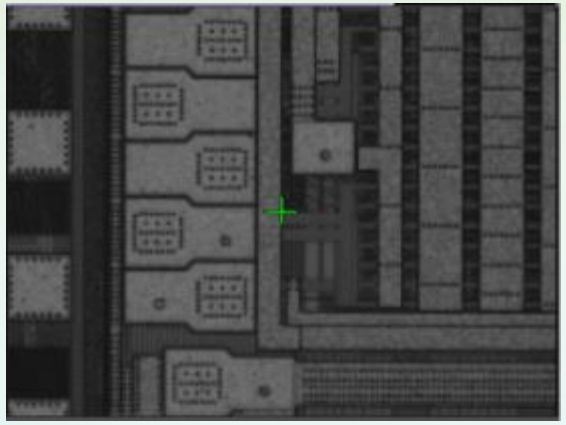
STD

HCTE

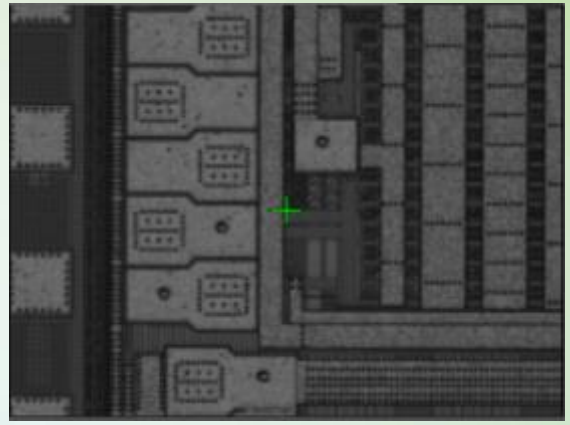


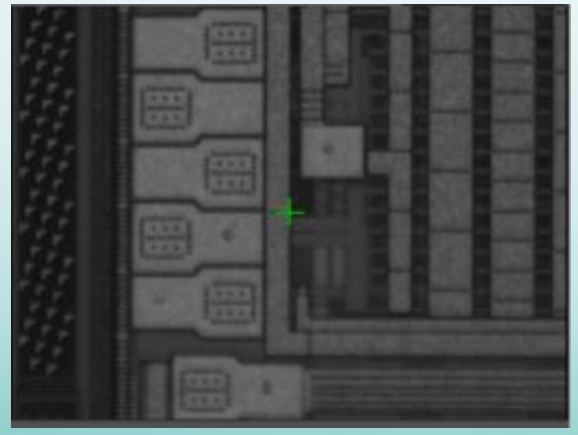
Analysis : Focus on site 57

Almost same behaviour

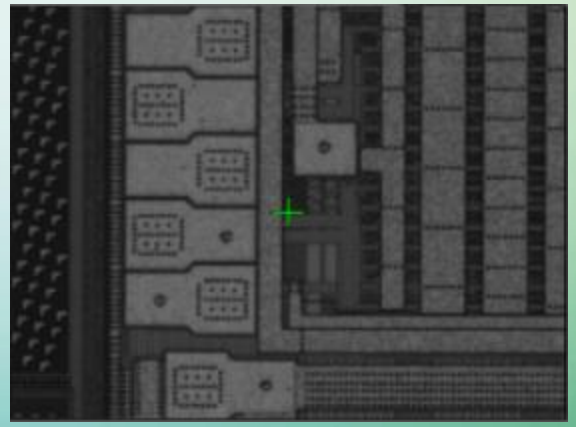


30°





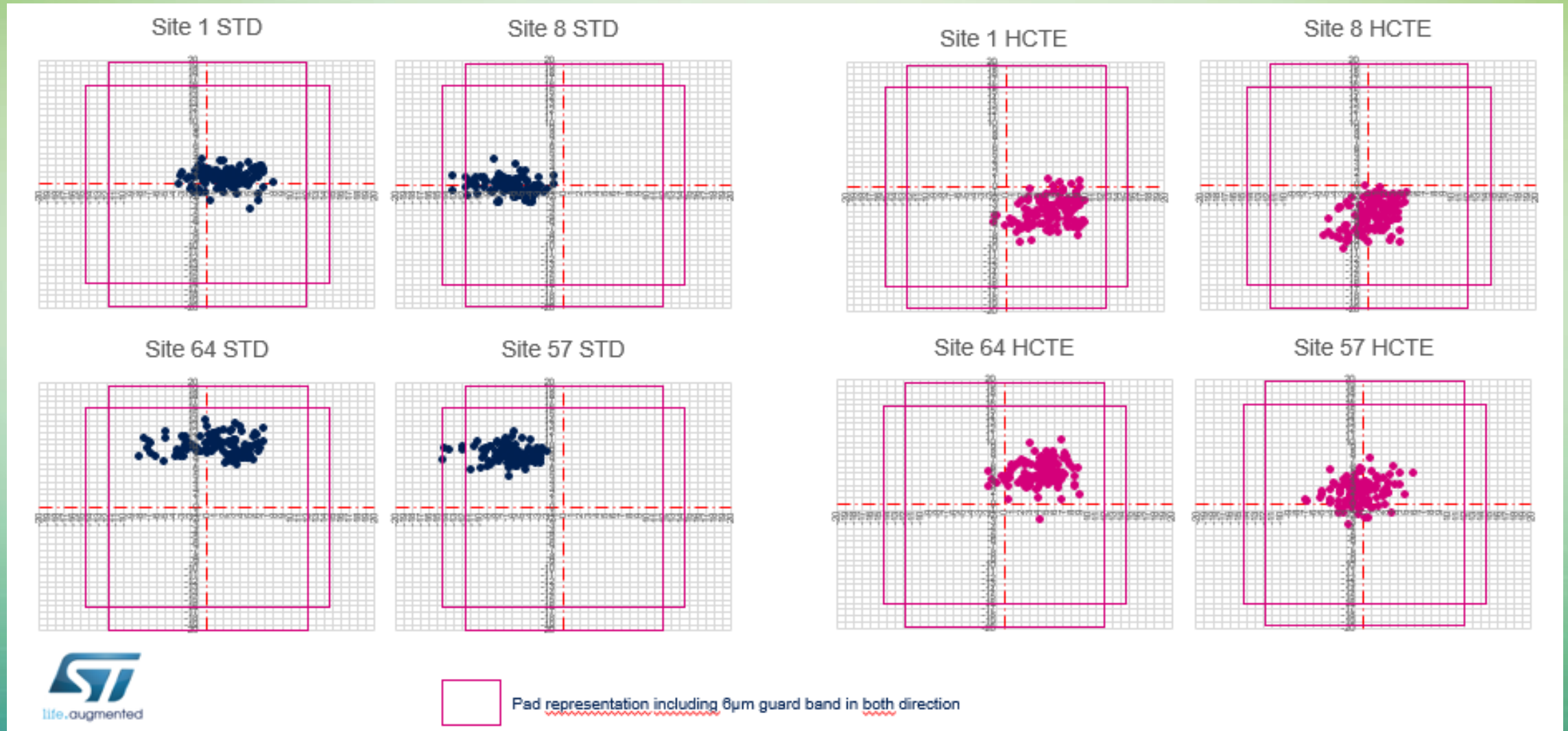
90°



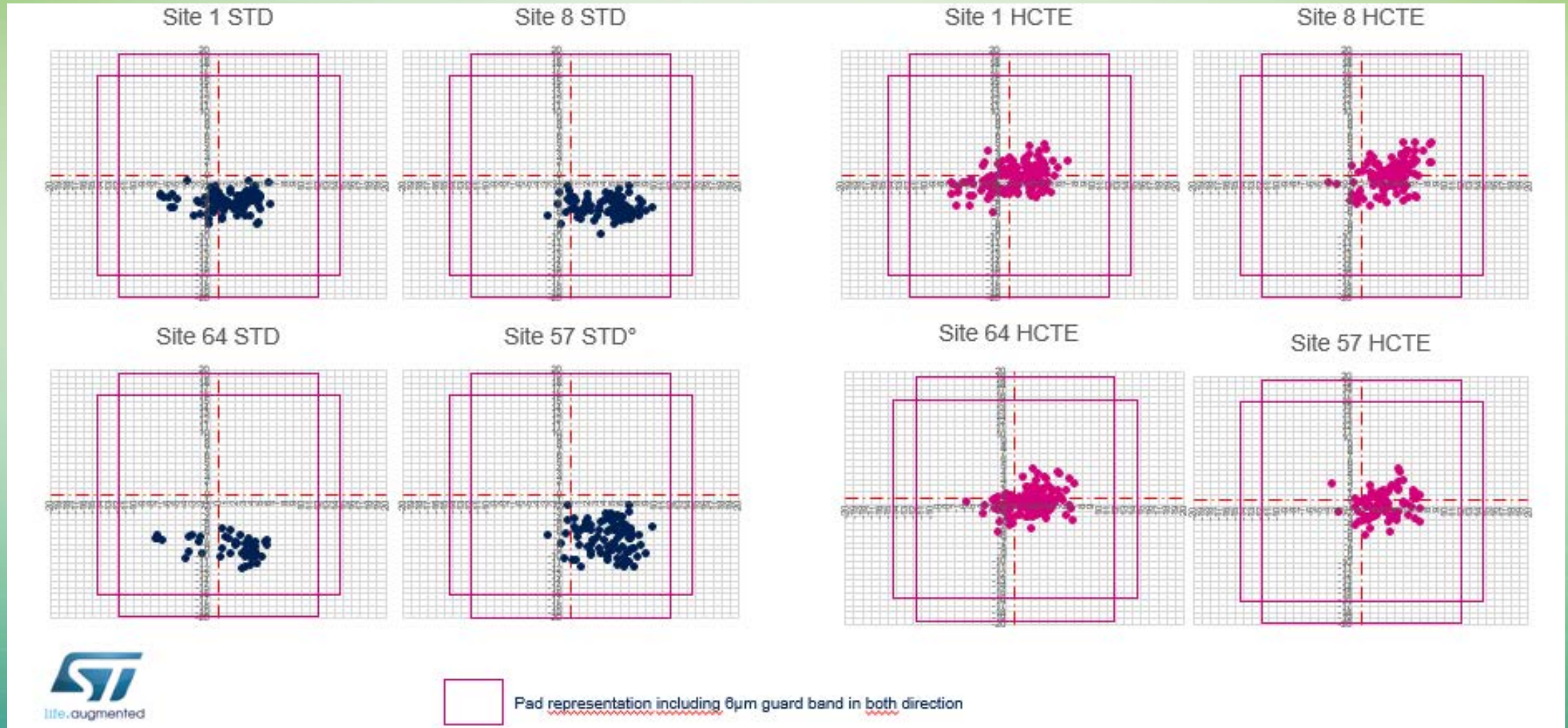
STD

HCTE

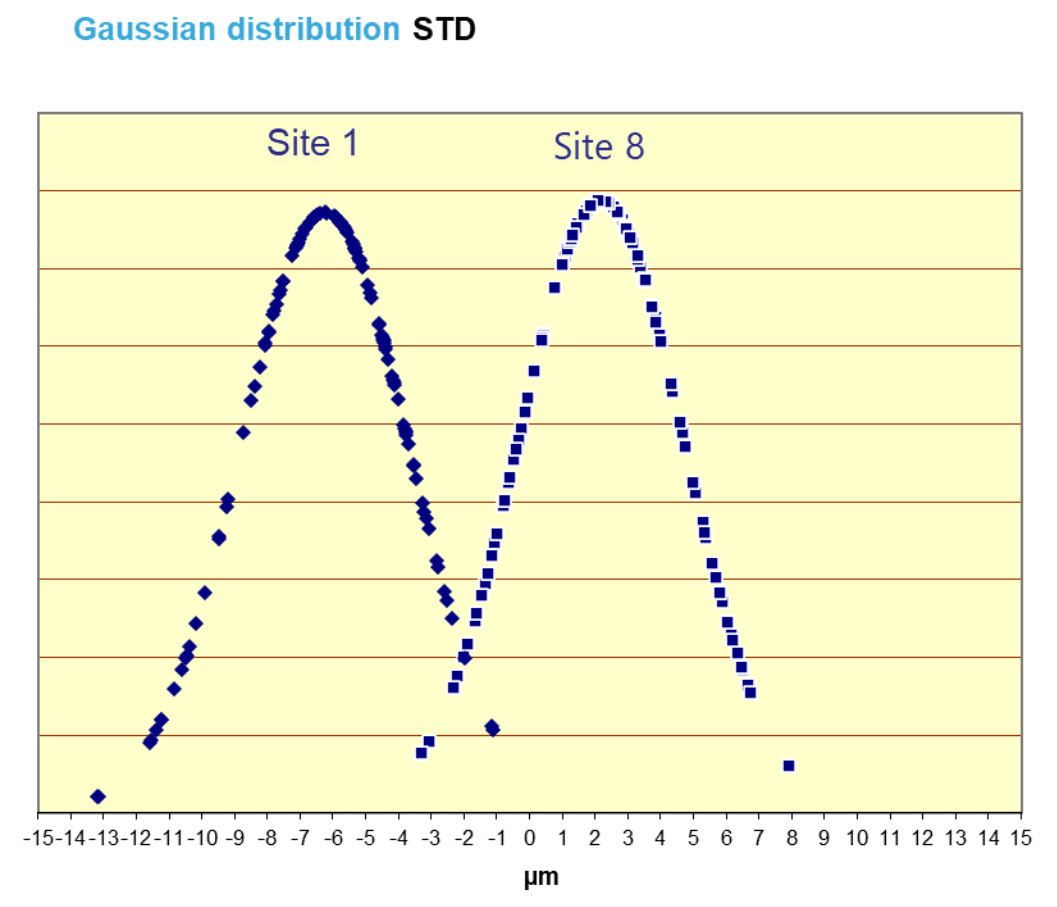
AVI Results: testing at 150 °C



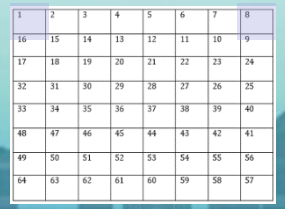
AVI Results: testing at -45 °C

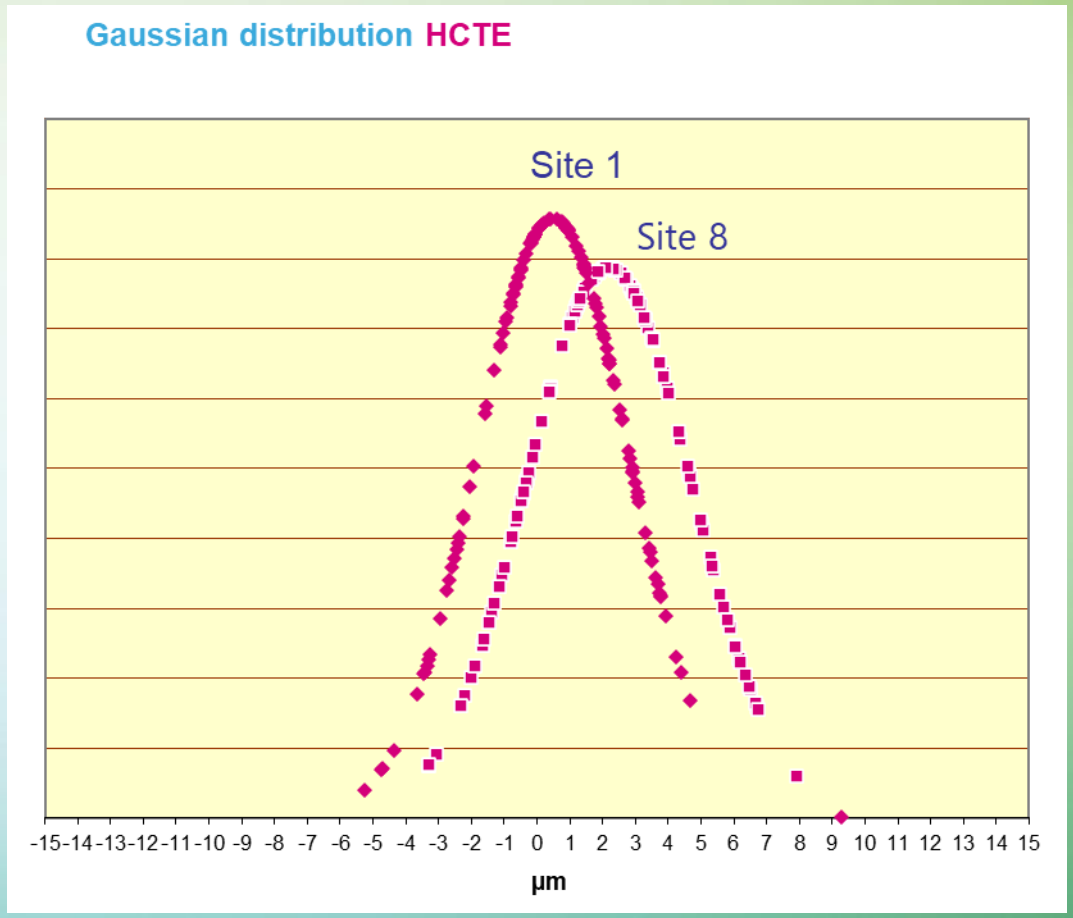


150°C Align X STD/ HCTE Site 1 / Site 8

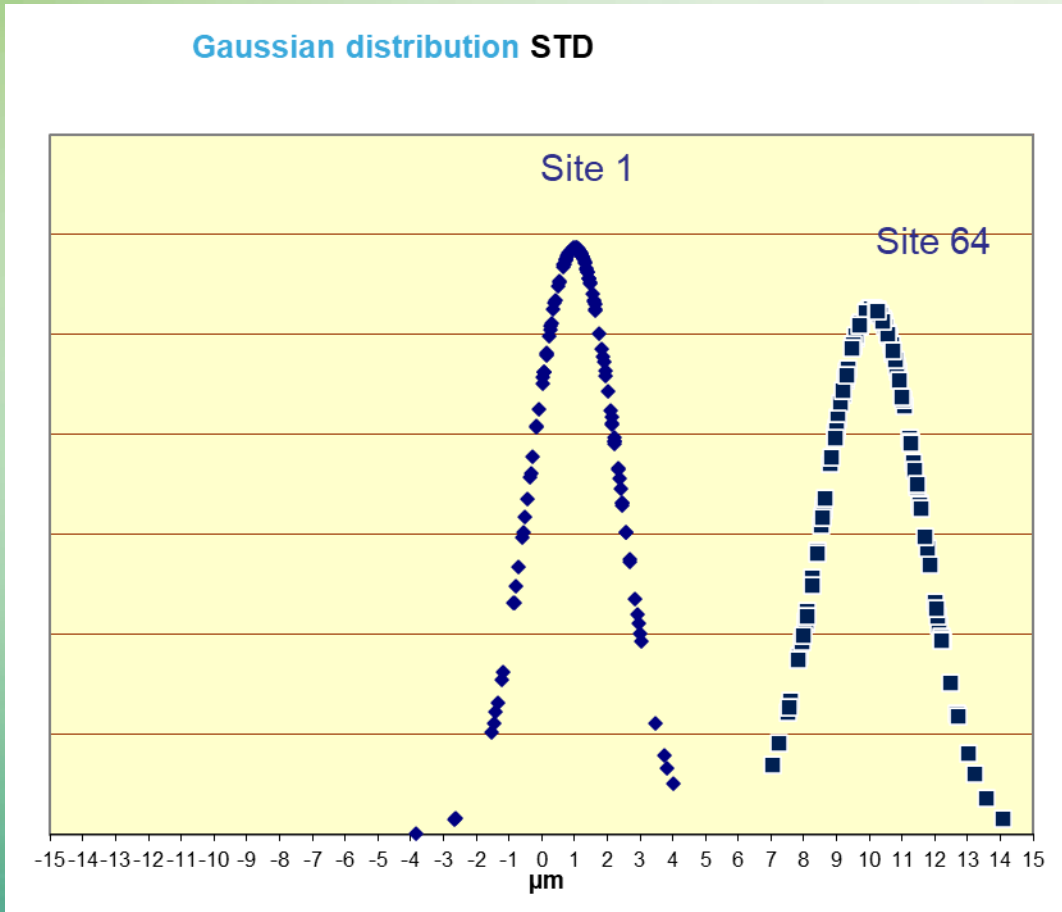


PM Xerr gap:
STD = 10µm
HCTE = 1.3µm

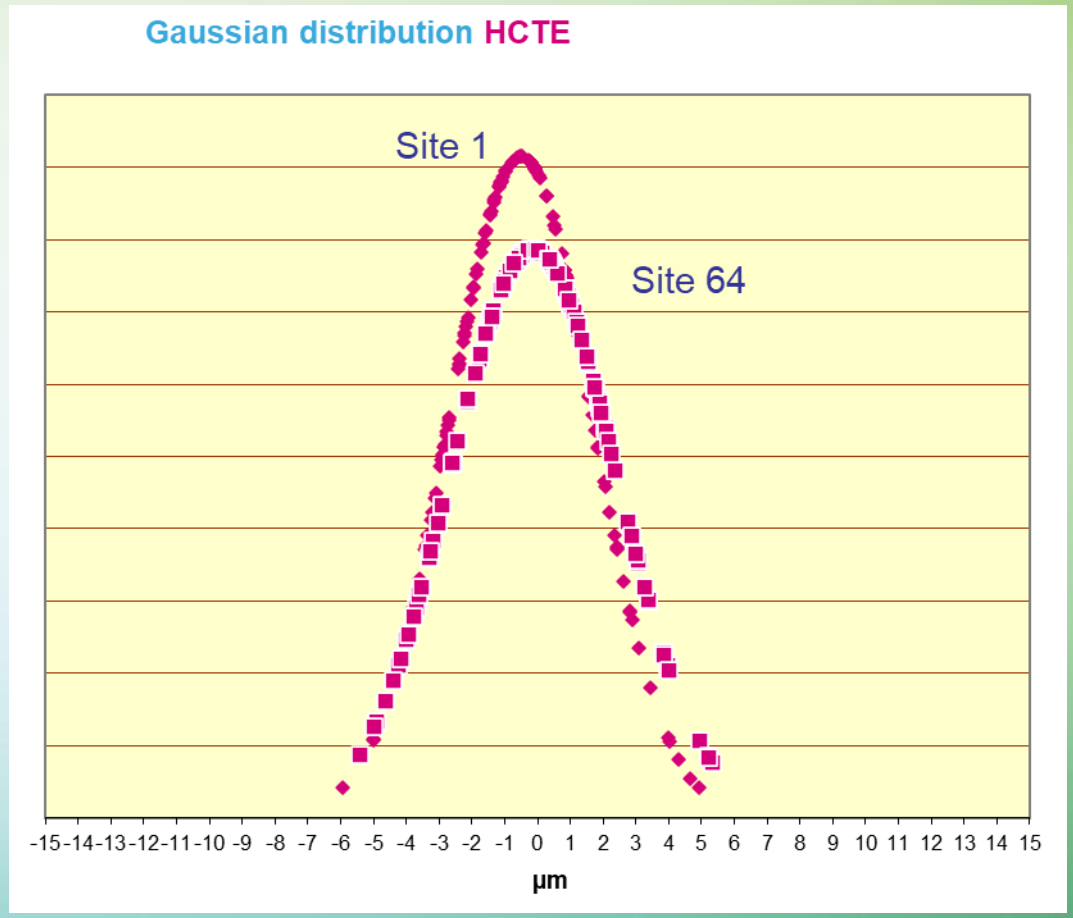


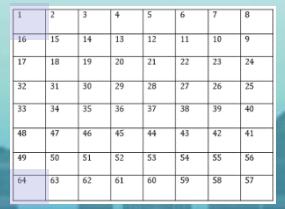


150°C Align Y STD/ HCTE Site 1 / Site 64

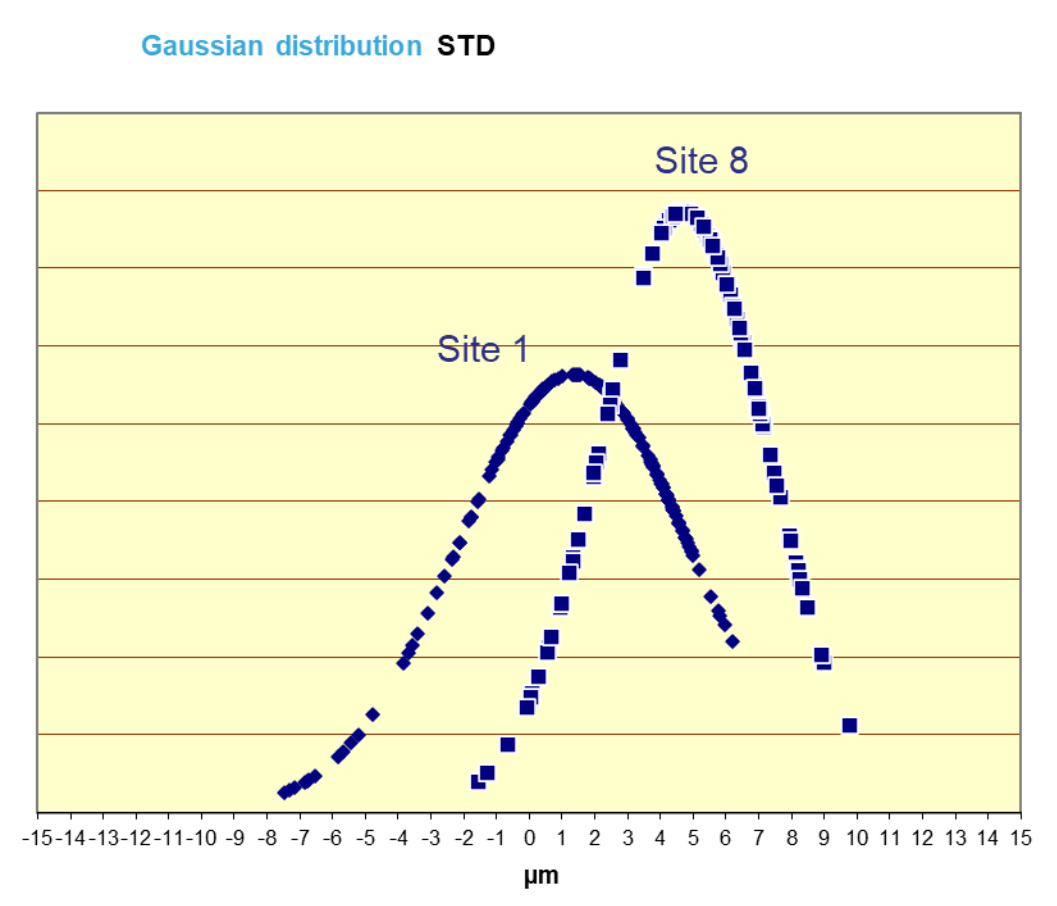


PM Yerr gap:
STD =8.8 µm
HCTE = 0.2µm

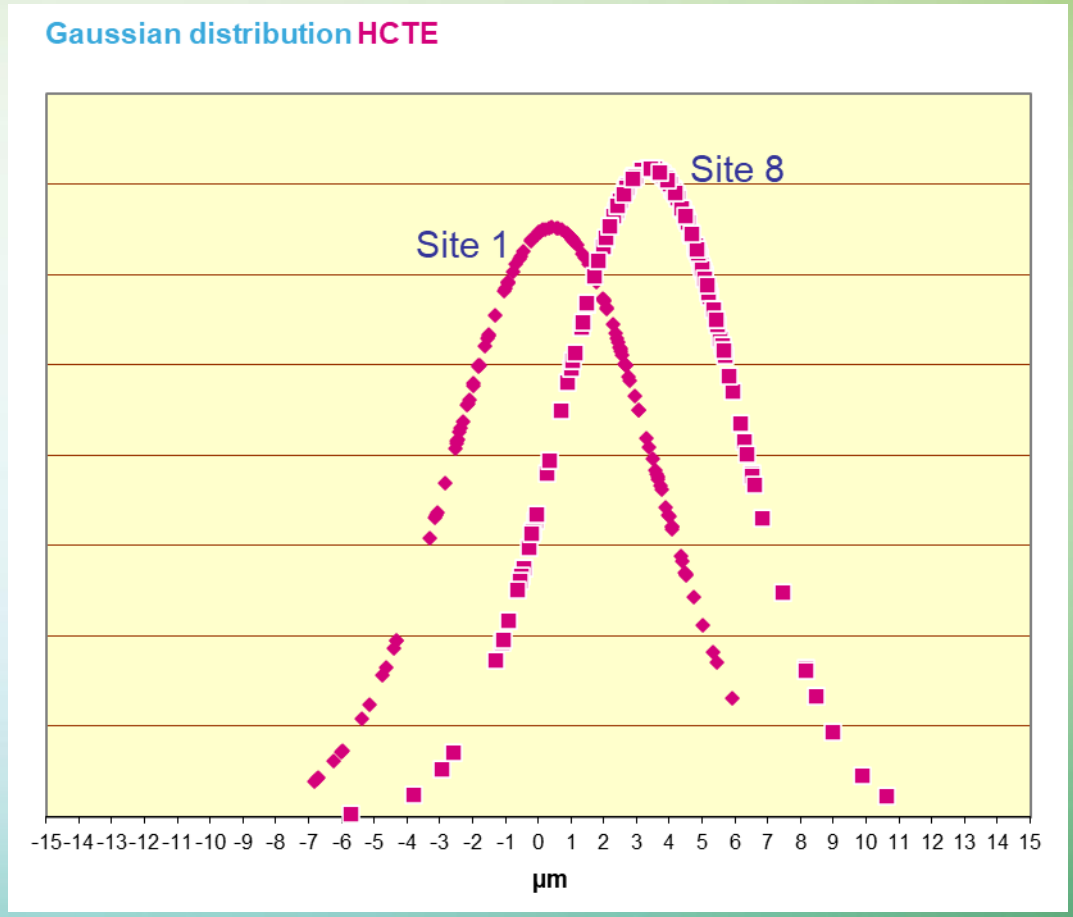


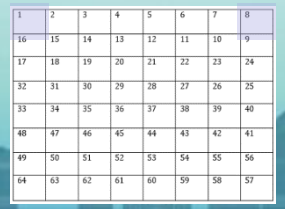


-45°C Align X STD/ HCTE Site 1 / Site 8

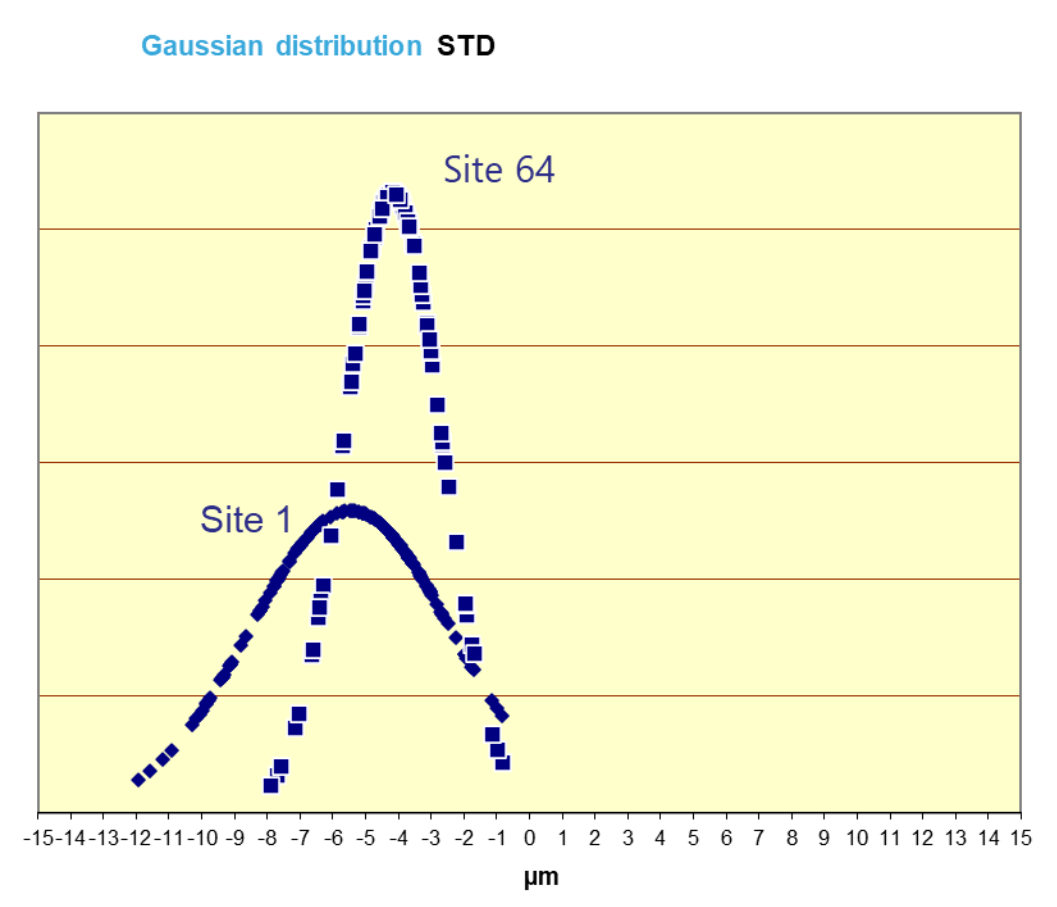


PM Xerr gap:
STD = 4.3µm
HCTE = 2.5µm

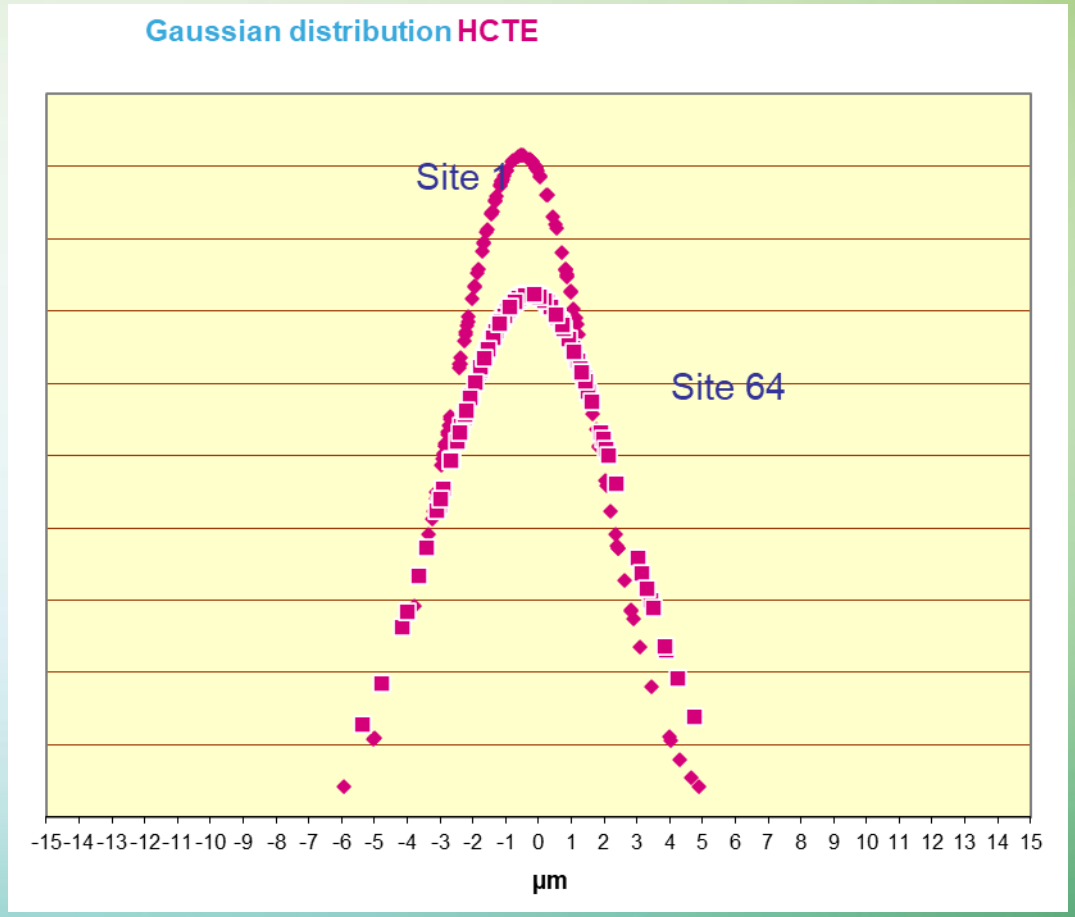


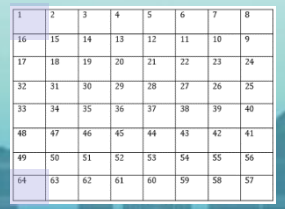


-45°C Align Y STD/ HCTE Site 1 / Site 64



PM Yerr gap:
STD = 2µm
HCTE = 0µm





Probe mark position error comparison

- **HCTE architecture compared with Standard architecture demonstrates significant improvement of PTPA alignment error due to thermal shift**

Dimension	STD PH	HCTE PH	Absolute improvement	Alignment Error reduction
X direction @ 150 °C	-10 um	-1.3 um	Δ = 8.7 um	-87%
Y direction @ 150 °C	-8.8 um	-0.2 um	Δ = 8.6 um	-98%
Diagonal @ 150 °C	-11.1 um	-2.2 um	Δ = 8.9 um	-80%
X direction @ -45 °C	4.3 um	2.5 um	Δ = 1.8 um	-42%
Y direction @ -45 °C	2.0 um	0.0 um	Δ = 2.0 um	-100%
Diagonal @ -45 °C	8.5 um	3.0 um	Δ = 5.5 um	-65%

Conclusions

- **A wide temperature range probe card architecture capable to match wafer thermal dilatation has been developed by Technoprobe**
- **This solution has been characterized and validated on the field in collaboration with ST Microelectronics**
  - In terms of probe marks positioning, **HCTE architecture** compared with Standard architecture demontrates for the specific application
    - Improvement of 8 - 9 um at +150 °C, where average probe mark shift at corner DUT is reduced by 88%
    - Improvement of 2 - 5 um at – 45 °C, where average probe mark shift at corner DUT is reduced by 70%
  - Combined with TPEG™ needle technology, HCTE architecture provides a high performing solution to control probe marks alignment for large array size, high parallelism and small pads size, over a wide temperature range

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[3] Y. Okada and Y. Tokumaru, *Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K* – Journal of Applied Physics 56 (1984)

[4] H. Watanabe et al., *Linear Thermal Expansion Coefficient of Silicon from 293 to 1000 K* – International Journal of Thermophysics 25 (2004)