ARCHITECTING TEST SOLUTIONS FOR THE NEXT GENERATION OF COMPUTE

SWTEST 2022 KEYNOTE

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Product Engineering

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AGENDA

- INTRODUCTION : AMD & COMPUTE INDUSTRY
- TEST CHALLENGES
- PROBE CHALLENGES & NEEDS
- CLOSING

EVOLVING INDUSTRY

Founder: Jerry Sanders

[Fairchild Semiconductor]

1969 AMD

2003 SPANSION™

2006 ATI™

2009 GLOBAL FOUNDRIES

2016 TF · AMD

2022 XILINX®

SOURCE: en.wikipedia.org/wiki/Advanced_Micro_Devices
SOURCE: https://wccftech.com/8-facts-intel-amd-nvidia/

SEMICONDUCTOR MARKET IS MASSIVE & GROWING

COMPUTE

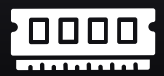
Microprocessor and Controller

ASIC/ASSP

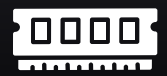
FPGA/Others

$239B

MEMORY



DRAM



NAND/Others

$123B

OTHERS

Analog

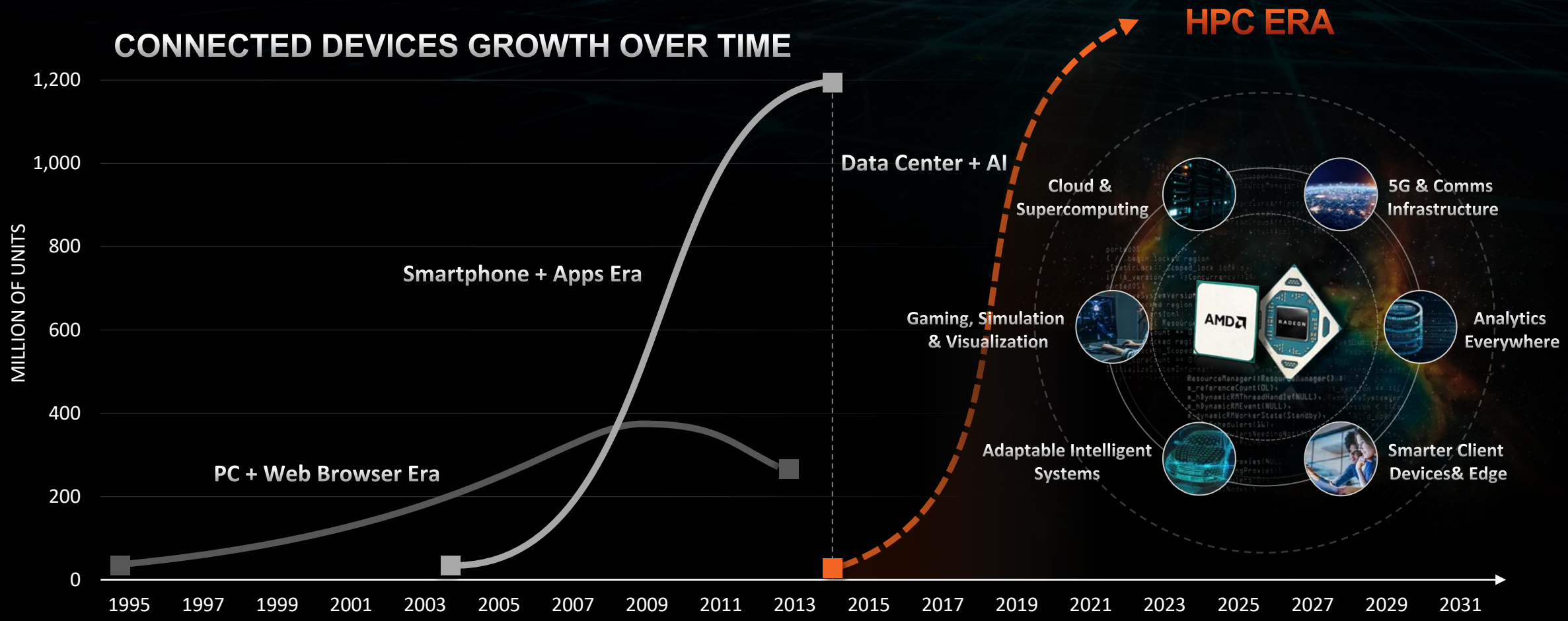
Discrete, Optoelectronics, Sensors, etc.

$88B

$450B MARKET

SOURCE: GARTNER SEMICONDUCTOR FORECAST Q4 2020, 2019 SIZE WAS $419B.

EXPLOSION OF CONNECTED DEVICES



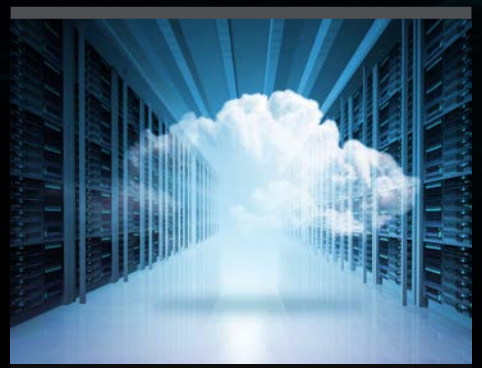
SOURCE: AMD

AMD Data Center Focus

Delivering CPU, GPU, and Adaptive Compute Solutions

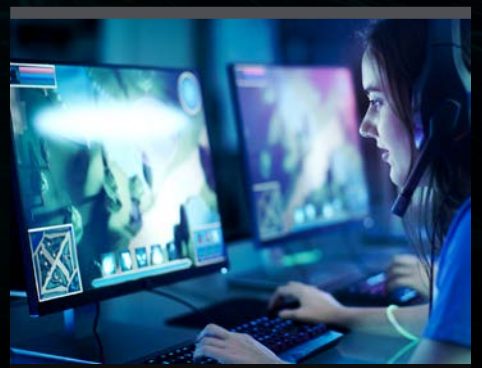
HPC

Enterprise/IT



Cloud

Machine Intelligence



Virtualization & Cloud Gaming

AMD EPYC

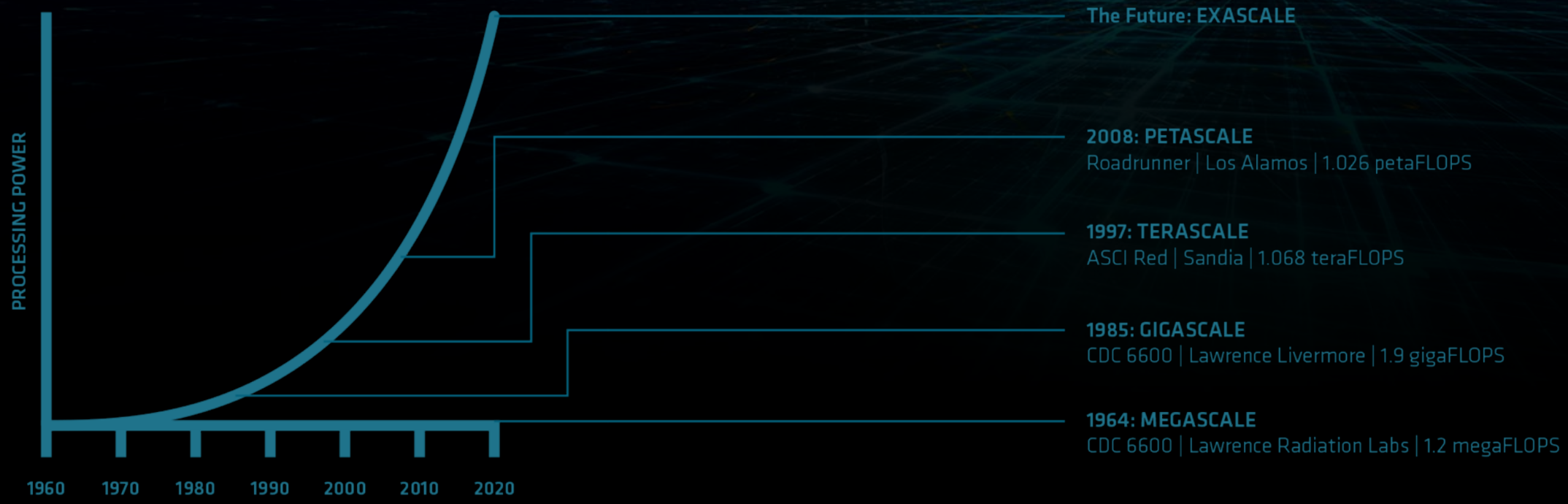
AMD INSTINCT

XILINX ALVEO™

XILINX VERSAL™

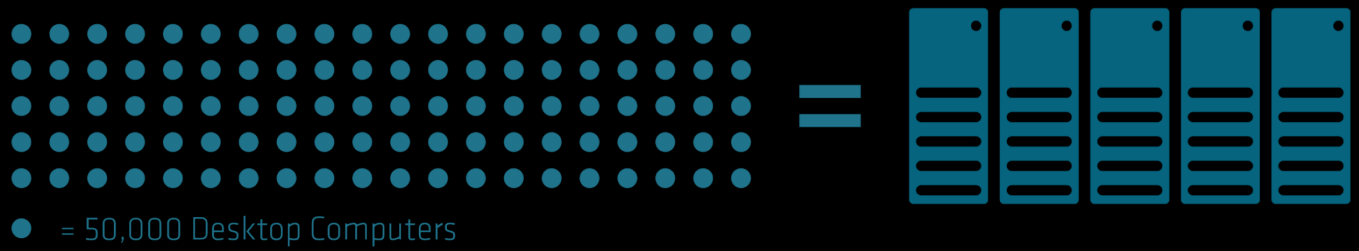
AMD

SUPERCOMPUTING



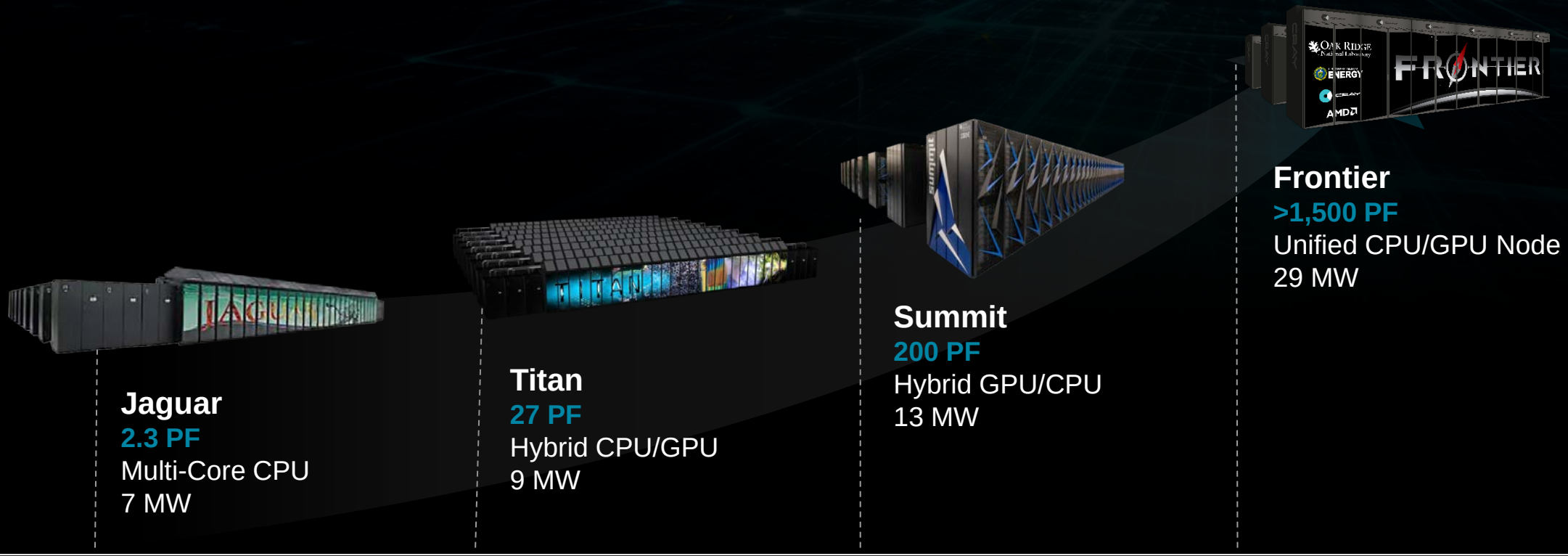
It would take 5,000,000 desktop computers to achieve the next level of supercomputer processing performance of 1 exaFLOP.*

*Assuming each desktop is capable of 200 gigaFLOPS



SOURCE: www.amd.com/en/technologies/hpc-explained

Oak Ridge National Laboratory's Journey from Petascale to Exascale



Jaguar
2.3 PF
Multi-Core CPU
7 MW

Titan
27 PF
Hybrid CPU/GPU
9 MW

Summit
200 PF
Hybrid GPU/CPU
13 MW

Frontier
>1,500 PF
Unified CPU/GPU Node
29 MW

2009 2012 2017 2022

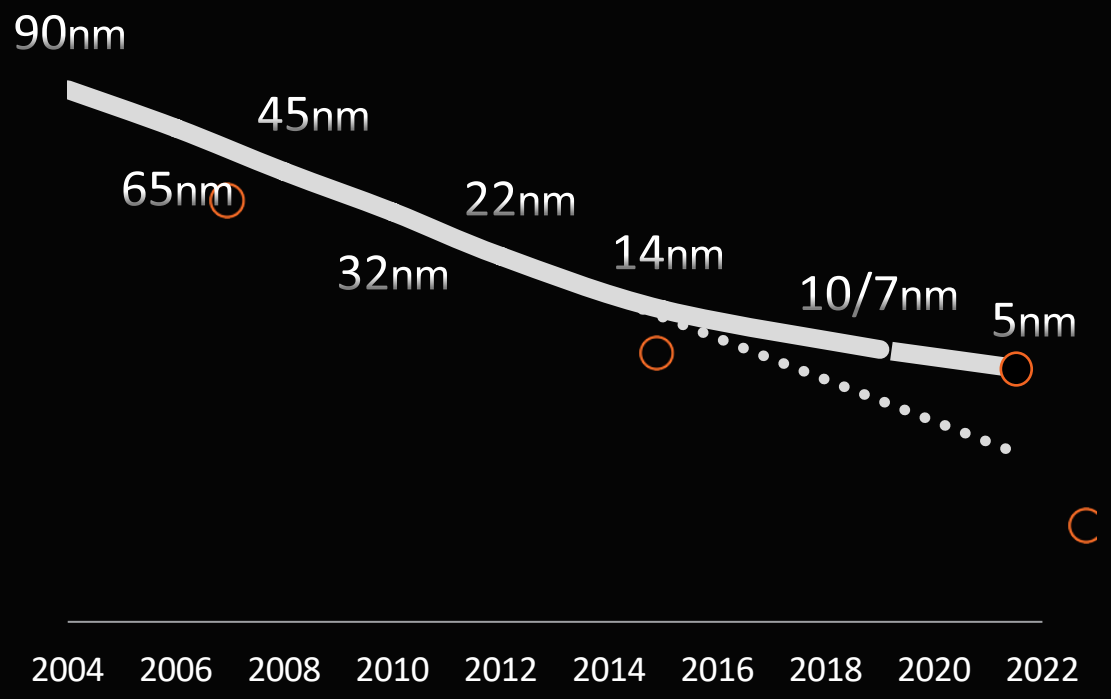
Petascale

Exascale

SOURCE: Oak Ridge National Laboratory

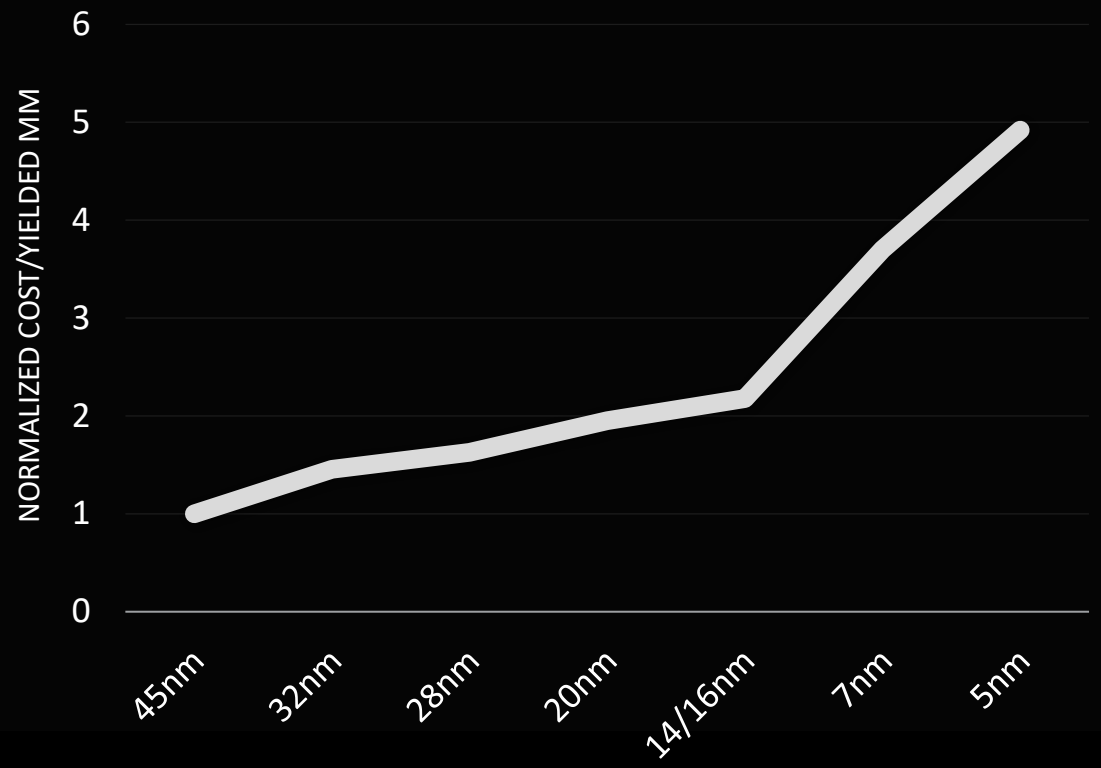
COST/MM2 BECOMING PROHIBITIVE

NEW NODE INTRODUCTION RATE IS SLOWING



WHILE COSTS CONTINUE TO INCREASE

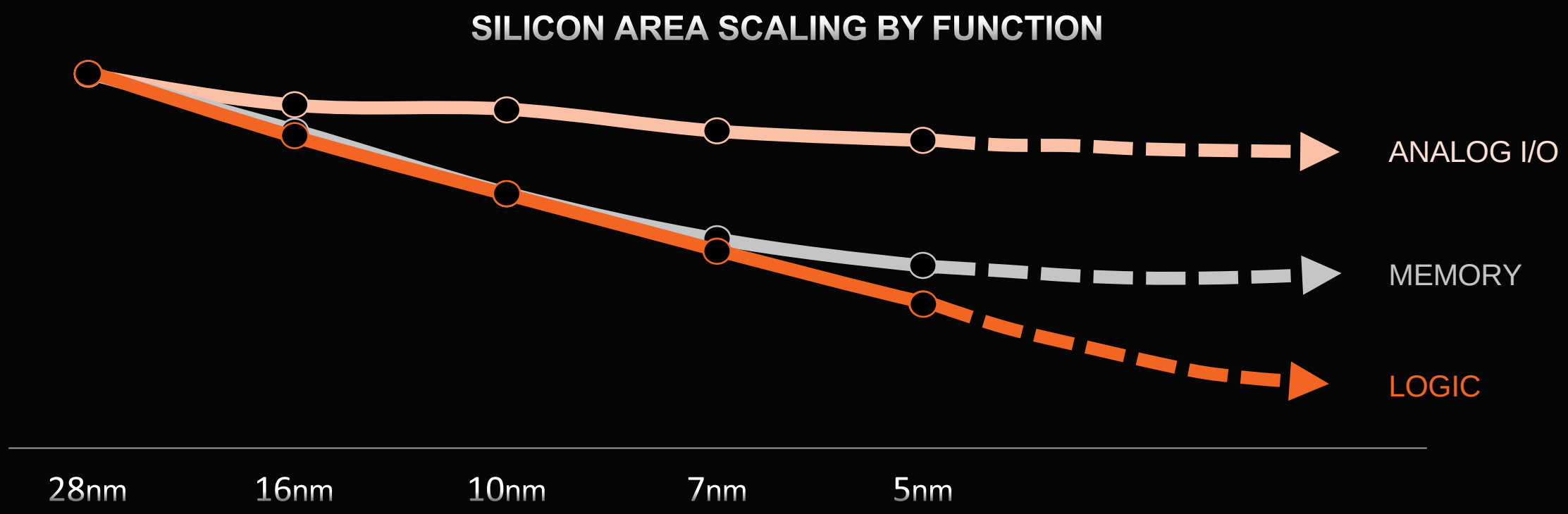
(Cost Per Yielded mm2 for a 250mm2 Die)



SOURCE: AMD

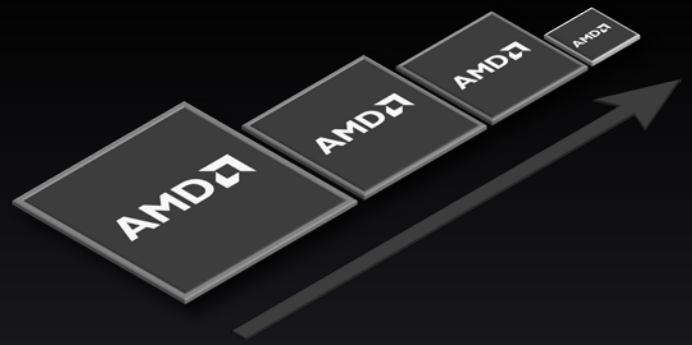
SILICON SCALING CHALLENGES

AREA SCALING BY CIRCUIT IP



REQUIRES NEW SOLUTIONS

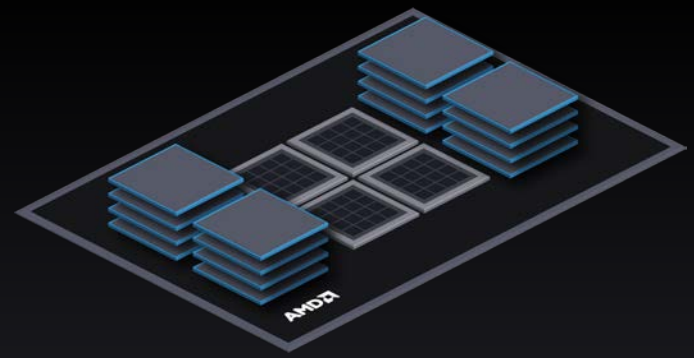
ADVANCED TECHNOLOGY
DEVICE INNOVATIONS



PROCESS

Continued Logic Scaling for Key Performance IP

Optimize Technology & IP Choice to Minimize Cost & Power



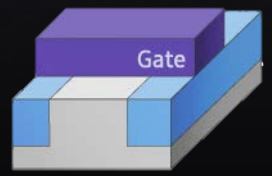
PACKAGING

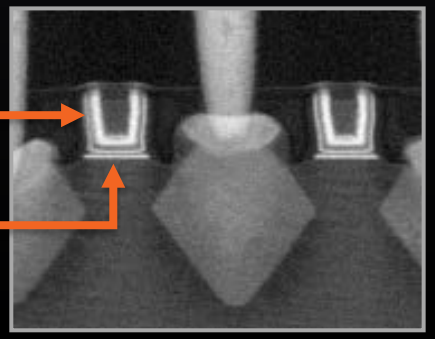
Leverage Advanced Packaging to Build Future SoC

Advanced 3-Dimensional Chiplets
Will Enable Heterogenous Designs

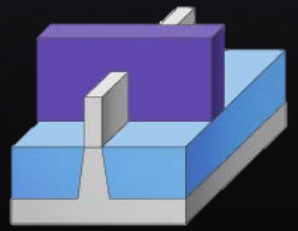
DEVICE FAB PROCESS ARCHITECTURES

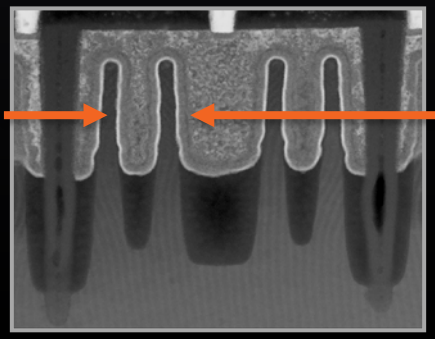
PLANAR



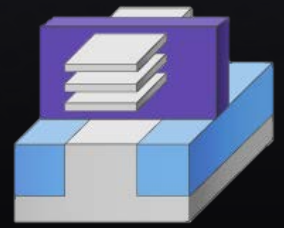


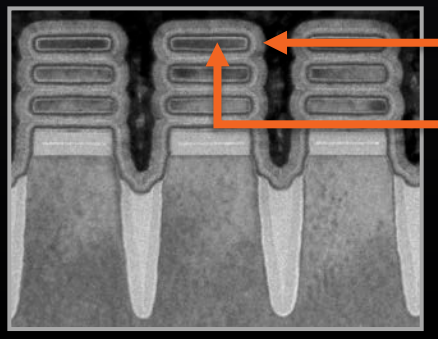
FinFET





GATE ALL AROUND





GOOD

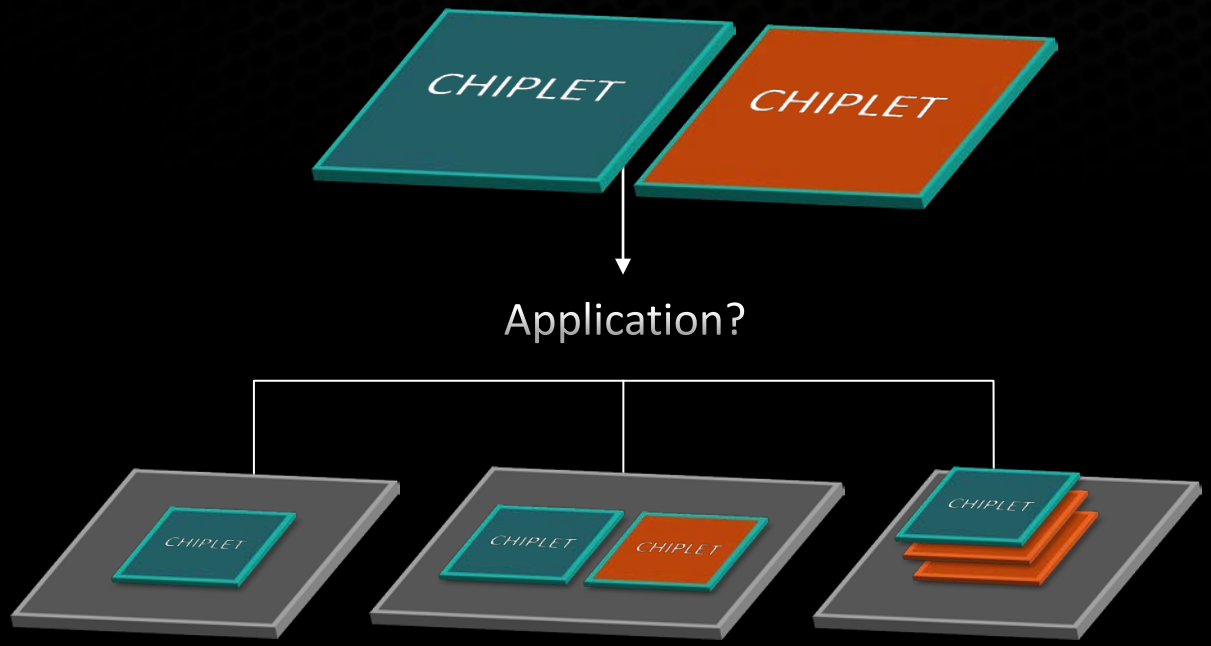
BETTER

BEST

ELECTROSTATICS

PACKAGE ARCHITECTURE GOALS

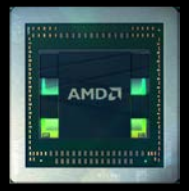
ENABLING A FLEXIBLE PACKAGING APPROACH



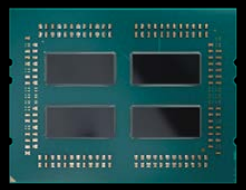
- Enable performance, power, area, cost (PPAC) for high-performance leadership products
- Heterogeneous architectures for configurable, segment-specific optimization
- Maximize product yield by enabling smaller, low-interconnect-overhead chiplets

AMD Leadership Packaging Innovation

2015 — 2.5D HBM

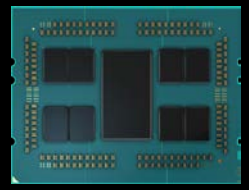


2017 — MULTICHIP MODULE



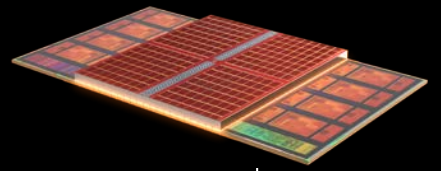
Led Industry in HBM, 2.5D & Chiplet Architecture

2019 — CHIPLETS

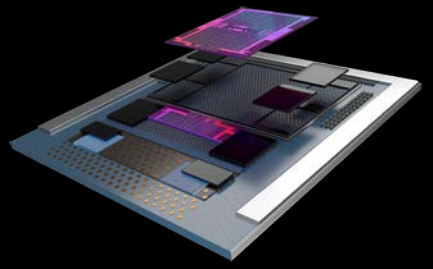


2021 — 3D CHIPLETS

(Chiplet + Advanced 3D Stacking)



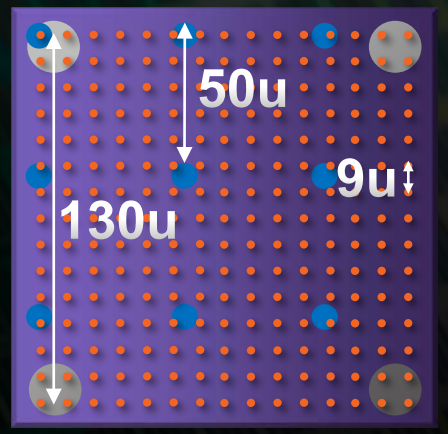
2021 — 2.5D CHIPLETS

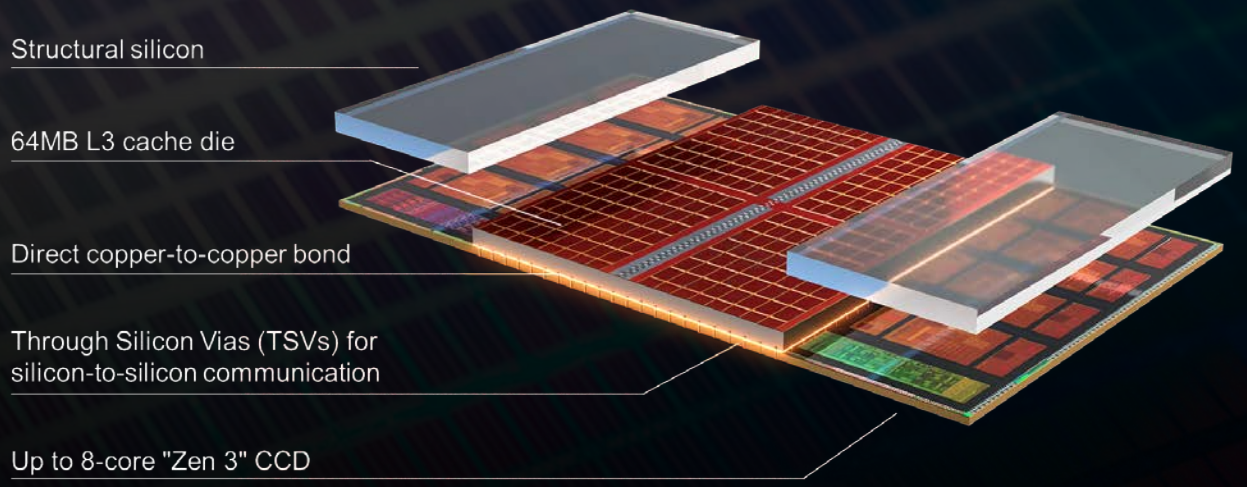


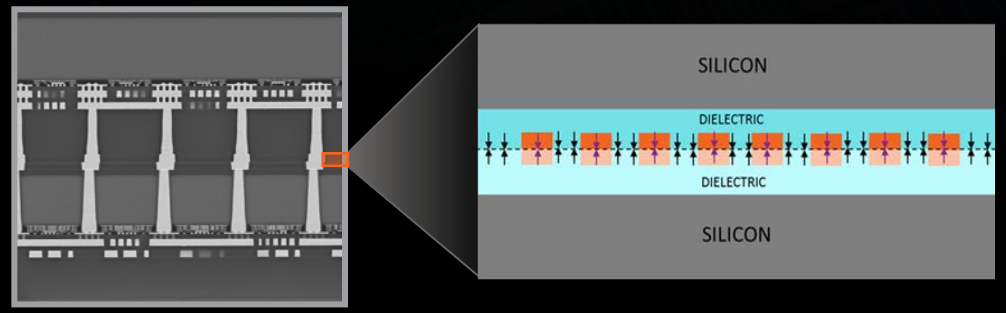
Aggressive Roadmap for Chiplet & 3D Integration

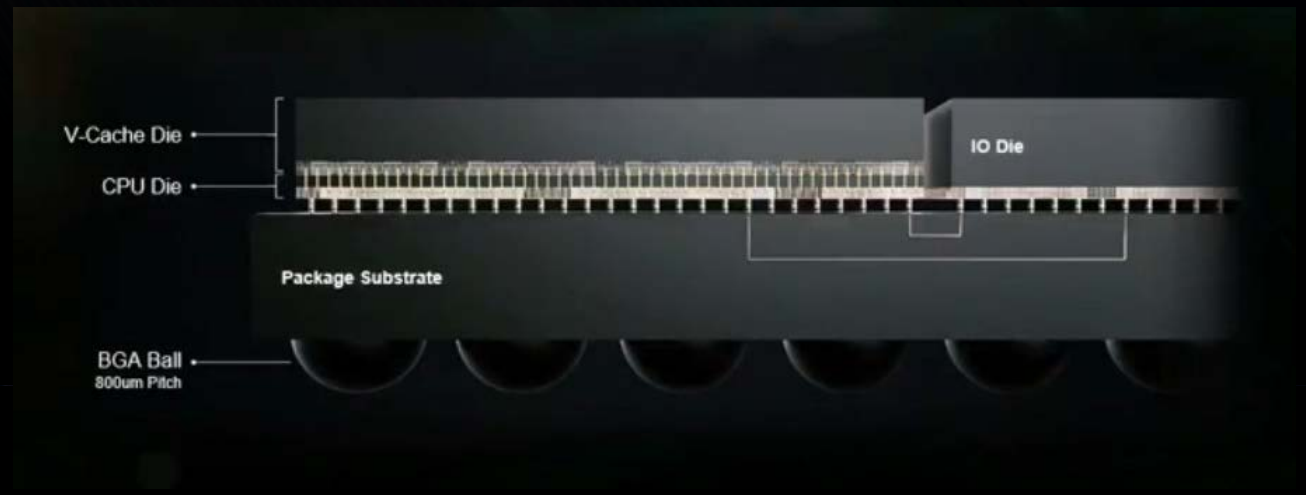
Manufacturing Friendly Elevated Fanout Bridge (EFB)

3D CHIPLET TECHNOLOGY







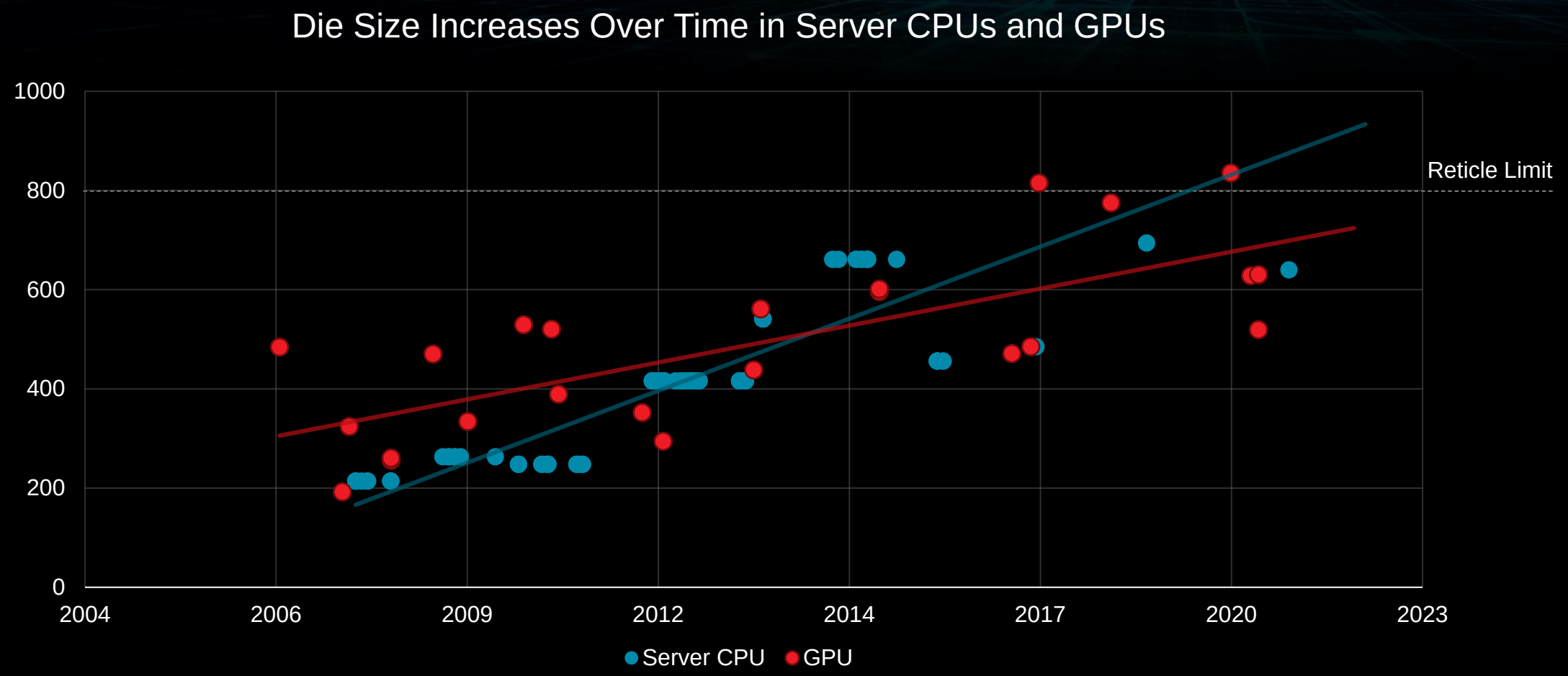


AMD

TEST CHALLENGES

Power & Performance
Quality & Reliability

Die Size Trend

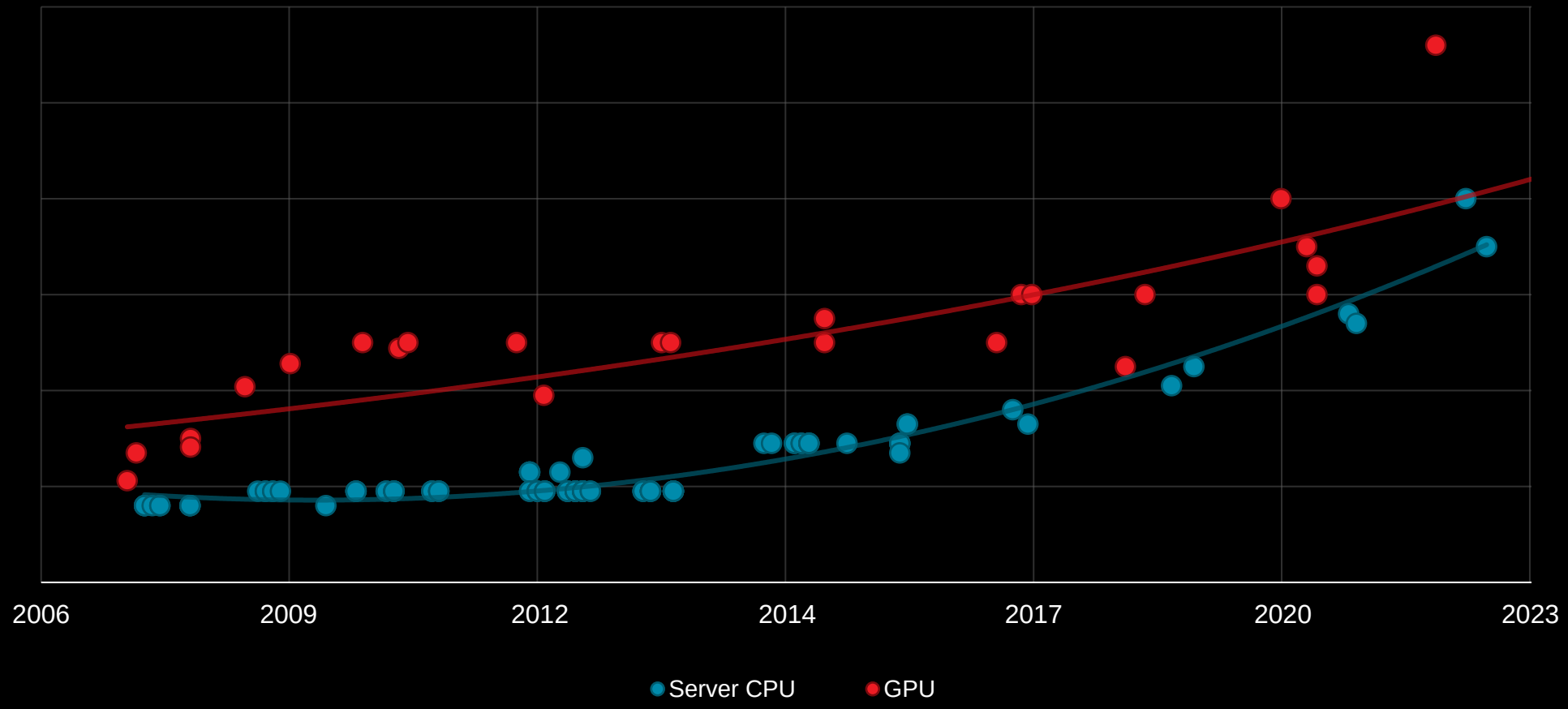


Die Sizes Increasing at an Unsustainable Rate

SOURCE: AMD

SOC Power Trend

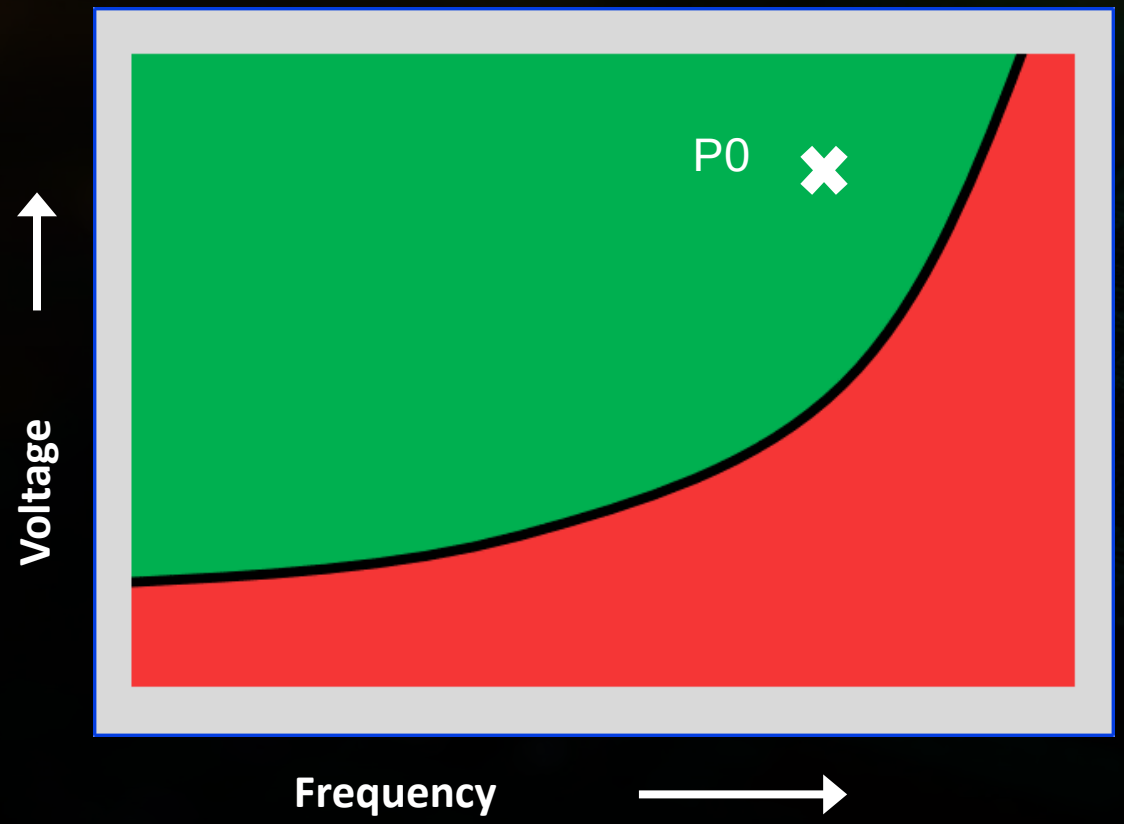
Thermal Design Power Over Time in Server CPUs and GPUs >2X



SOURCE: AMD

AMD

POWER & PERFORMANCE



Ex: P0 = Power/Freq/Voltage/Temp

Dependencies

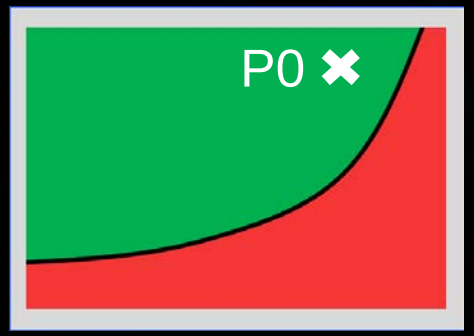
1. Test Content
2. Test Environment (ATE vs SLT vs Others)

POWER & PERFORMANCE EVOLUTION

Single P-State

Core 0

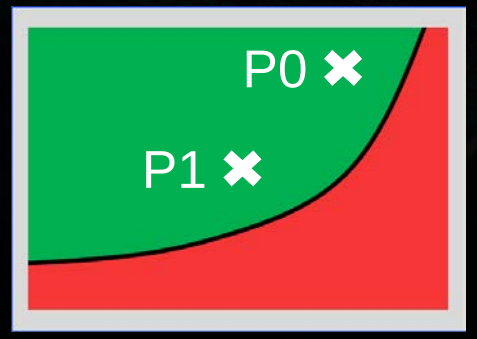
P0



Multiple P-States Single power plane

Core 0 | Core 1

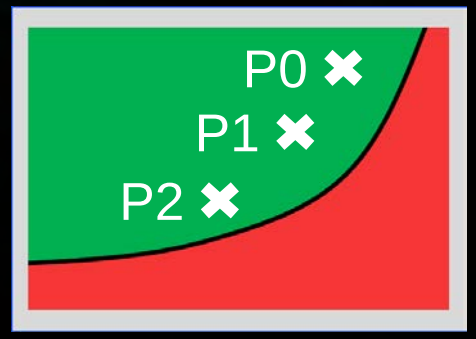
P0 P0



Multiple Finer P-States Independent power planes

Core 0 | Core 1 | Core 2 | Core 3

P0 P2 P1 P2



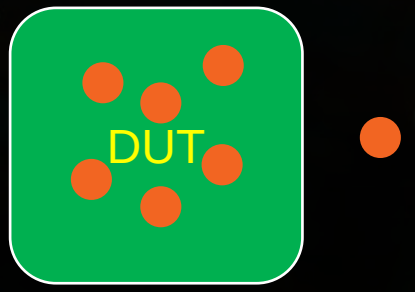
Px – Power State (Voltage, Frequency)

TEST TEMPERATURE : THERMAL SENSORS

Single Sensor
External

Internal Sensor
(Analog)
+
External Sensor

Multiple Internal Sensors
(Analog + Digital)
+
External Sensor



TEST TEMPERATURE : THERMAL DENSITY

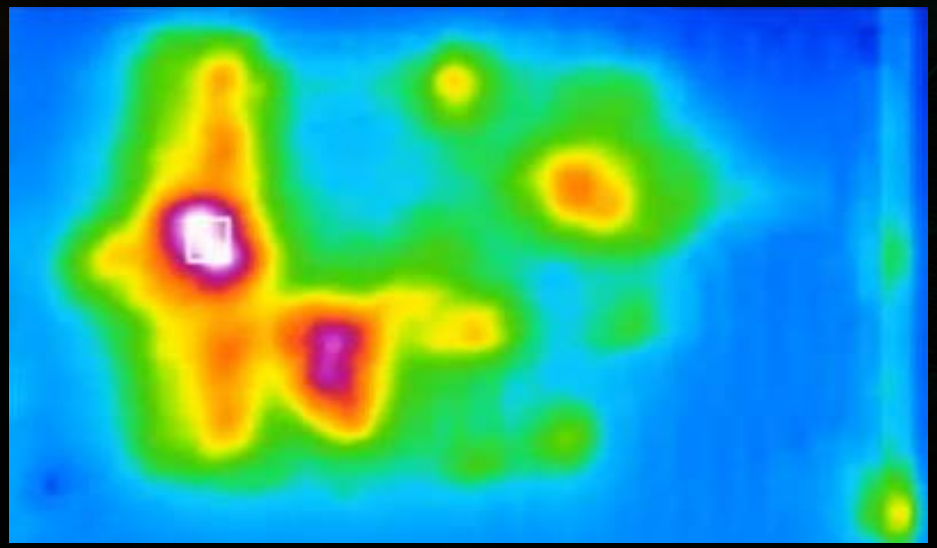


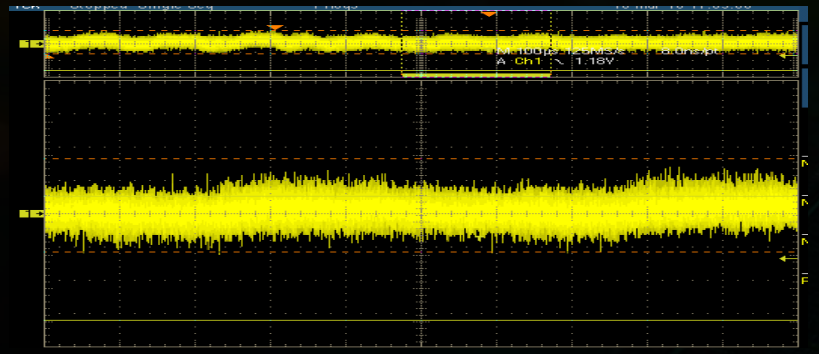
IMAGE SOURCE: AMD

CHALLENGES :

- Sense & Control at Hotspots
- Proper placement & calibration of in-silicon sensors (2D & 3D)
- Digital thermal sensors need to work in mission mode + DFT
- Reaction time for “Bigger” & “Faster” thermal capable systems

TEST VOLTAGE : VOLTAGE DROOP

Core Voltage [Diag# 1]



Core Voltage [Diag# 2]

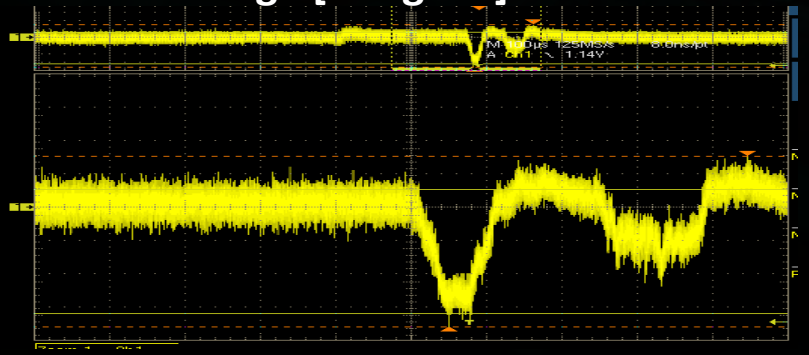
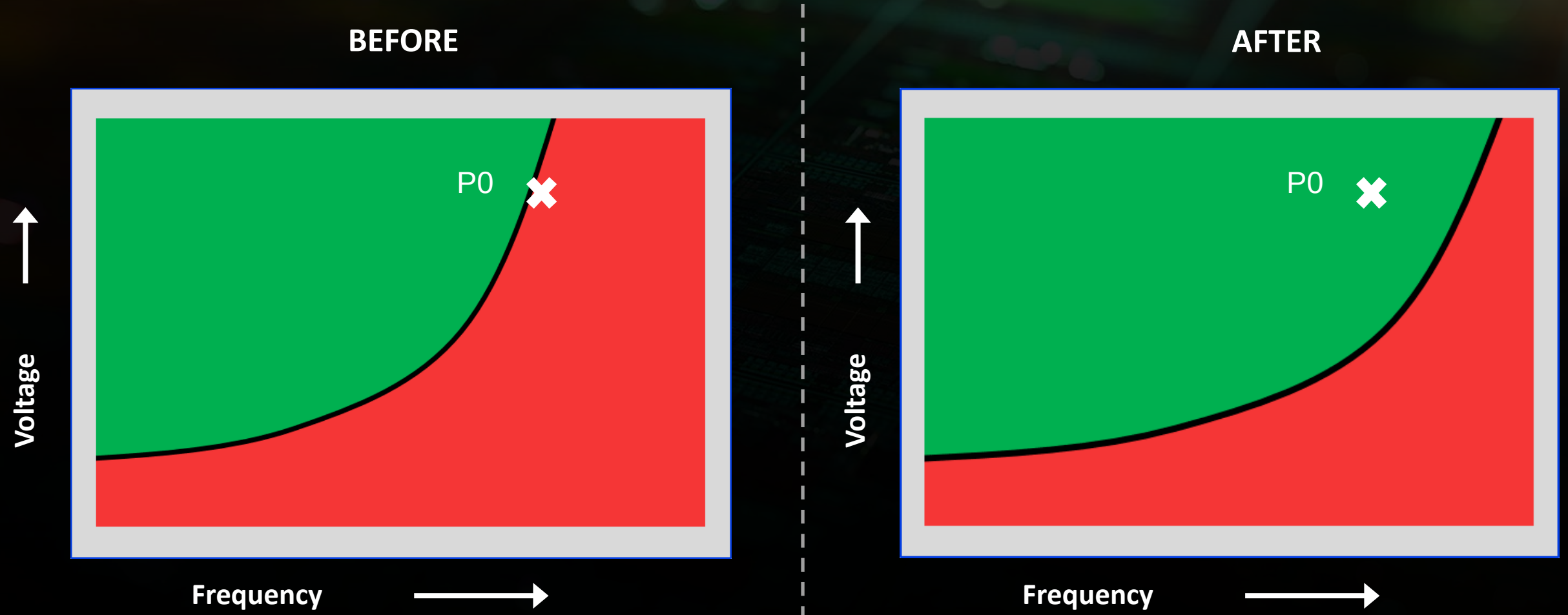


IMAGE SOURCE: AMD

CHALLENGES :

- DFT & diagnostics that mimic end-user behavior
- Balancing test margins

POWER & PERFORMANCE : NET IMPACT



BASELINE TEST INSERTIONS

ATE Wafer Sort

- Coarse Performance Bucketing
- Defect Coverage

Burn-in Wafer/Package

- Accelerate Reliability Coverage

ATE Package Test

- Finer Performance Binning
- Assembly Coverage
- Additional Coverage (temp or voltage related)

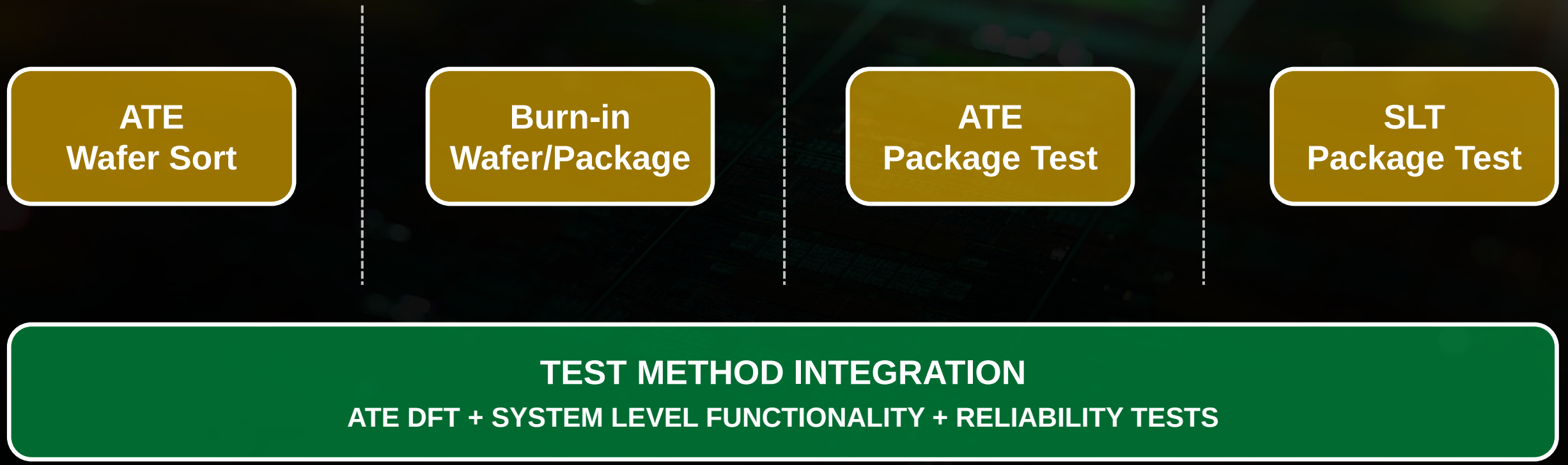
SLT Package Test

- Verify Performance Bin
- dPPM Coverage

IMPROVING TEST COVERAGE

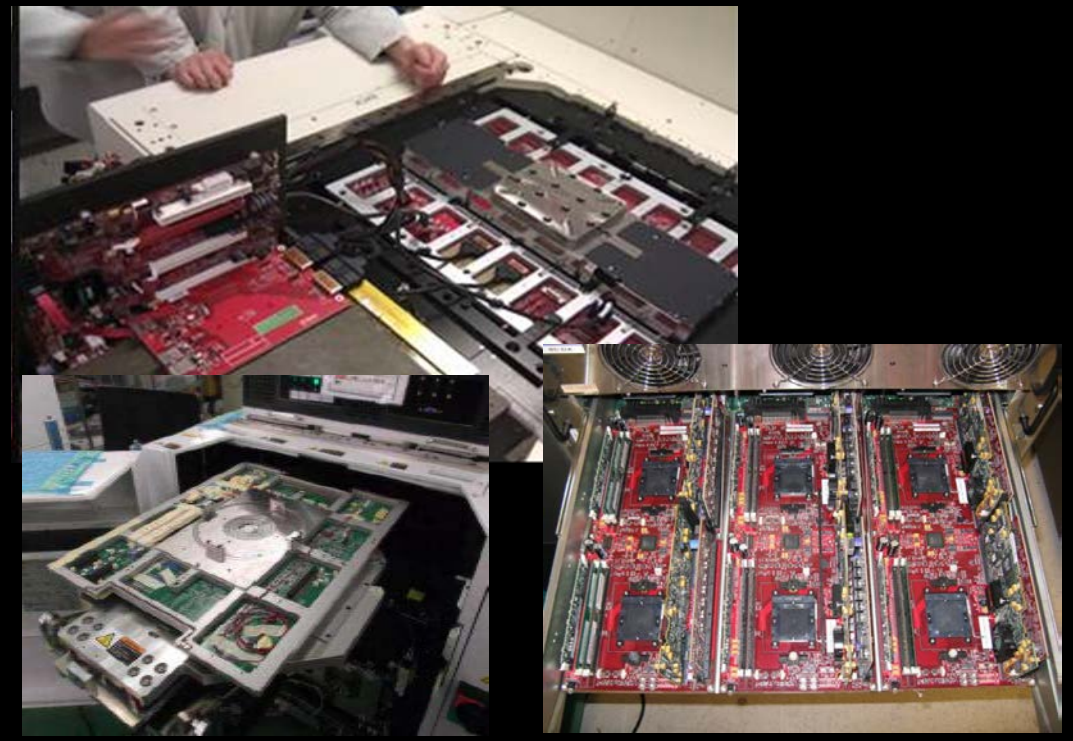
@ some point, the ‘cost’ of ATE test addition makes SLT more attractive

TEST “INTEGRATION”



TEST “INTEGRATION”

REDUCE TEST HW OVERHEAD : DFT INNOVATIONS



AMD Test R&D circa 2010 & 2012

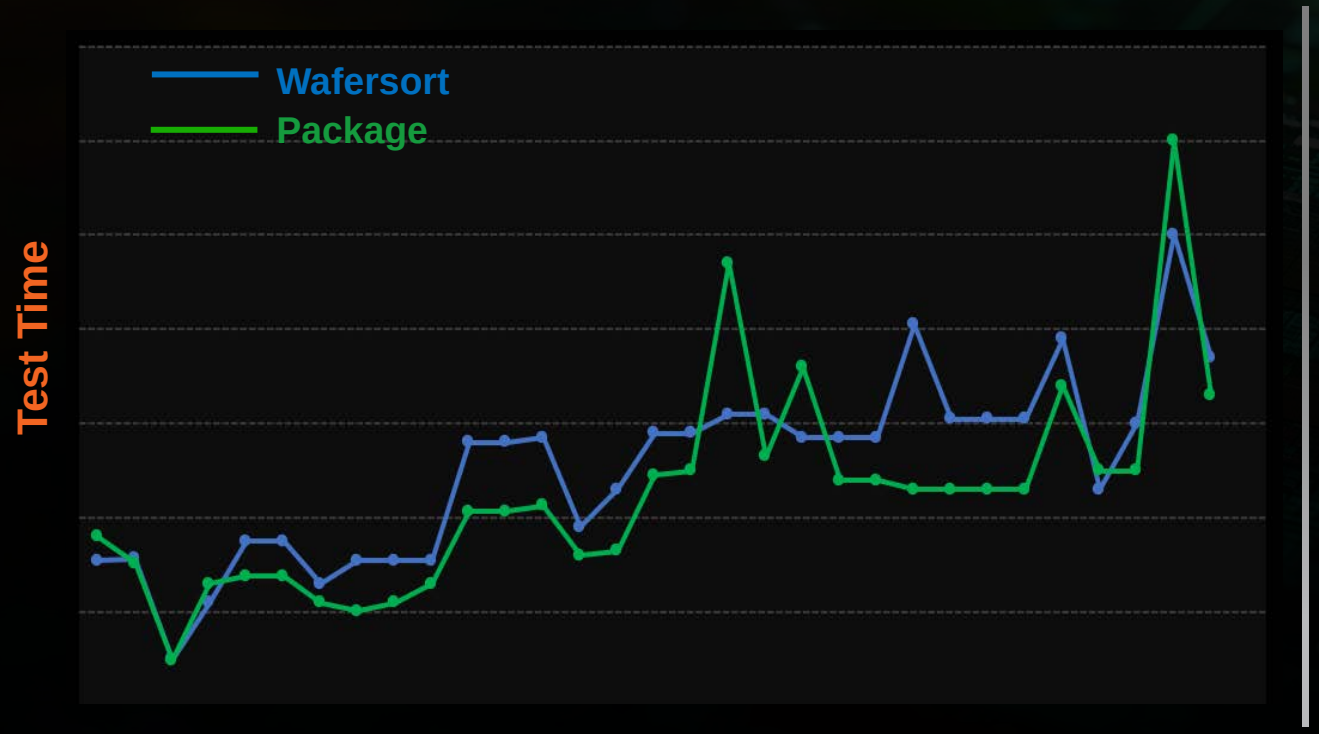
IMAGE SOURCE: AMD

3rd Party Test Platforms

IMAGE SOURCE: Advantest & Teradyne public web

GROWING TEST TIMES

ATE Test Time has increased >2X



SOURCE: AMD

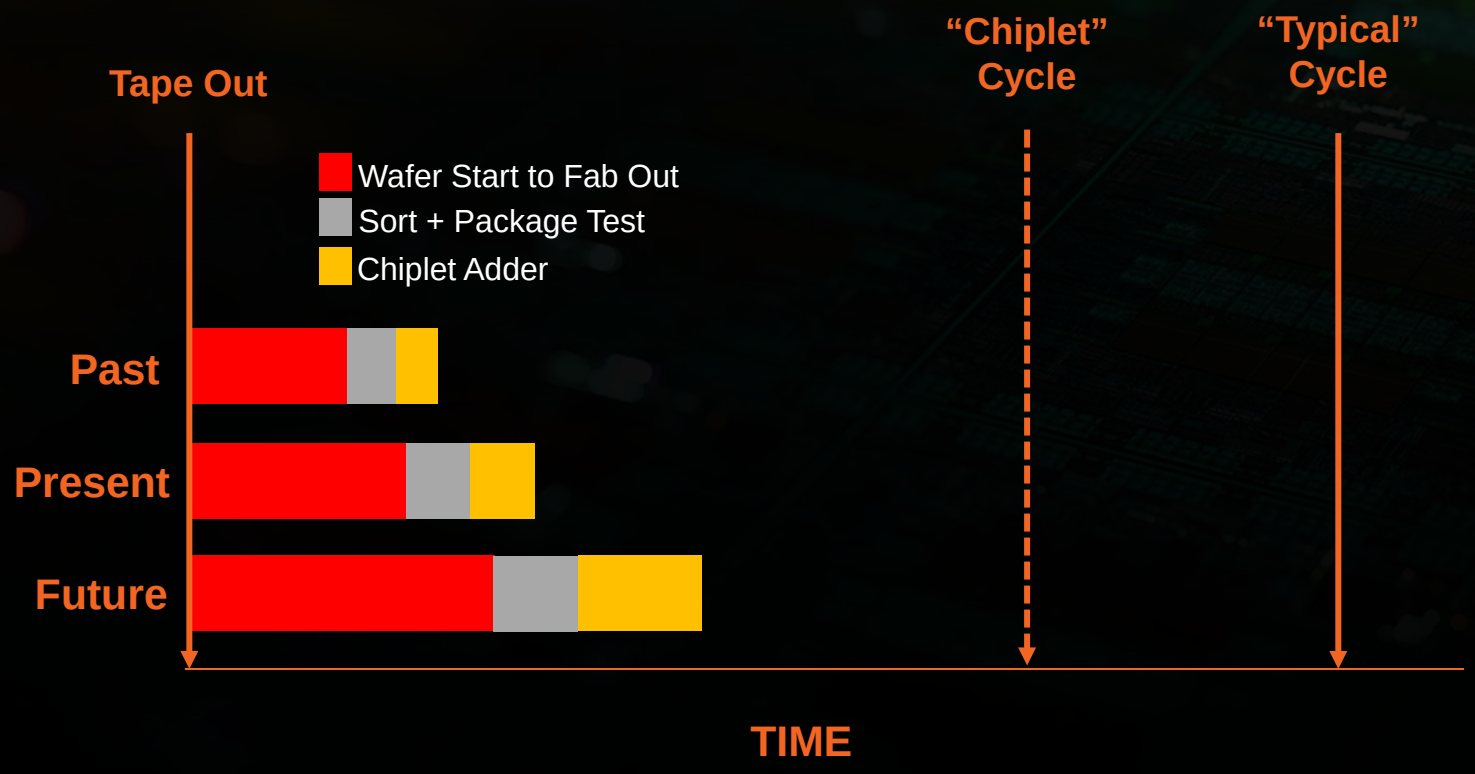
CAUSES

- IP Variations (SoC integration)
- More Cores
- Reliability Tests
- More Test Points
- More Characterization

MITIGATIONS

- DFT Innovations
  - Self-Test vs Tester Driven
  - Test architecture
- Parallelism
  - Increase multi-site

ACCELERATE TIME-TO-LEARN



SOURCE: AMD. Time scale not absolute.

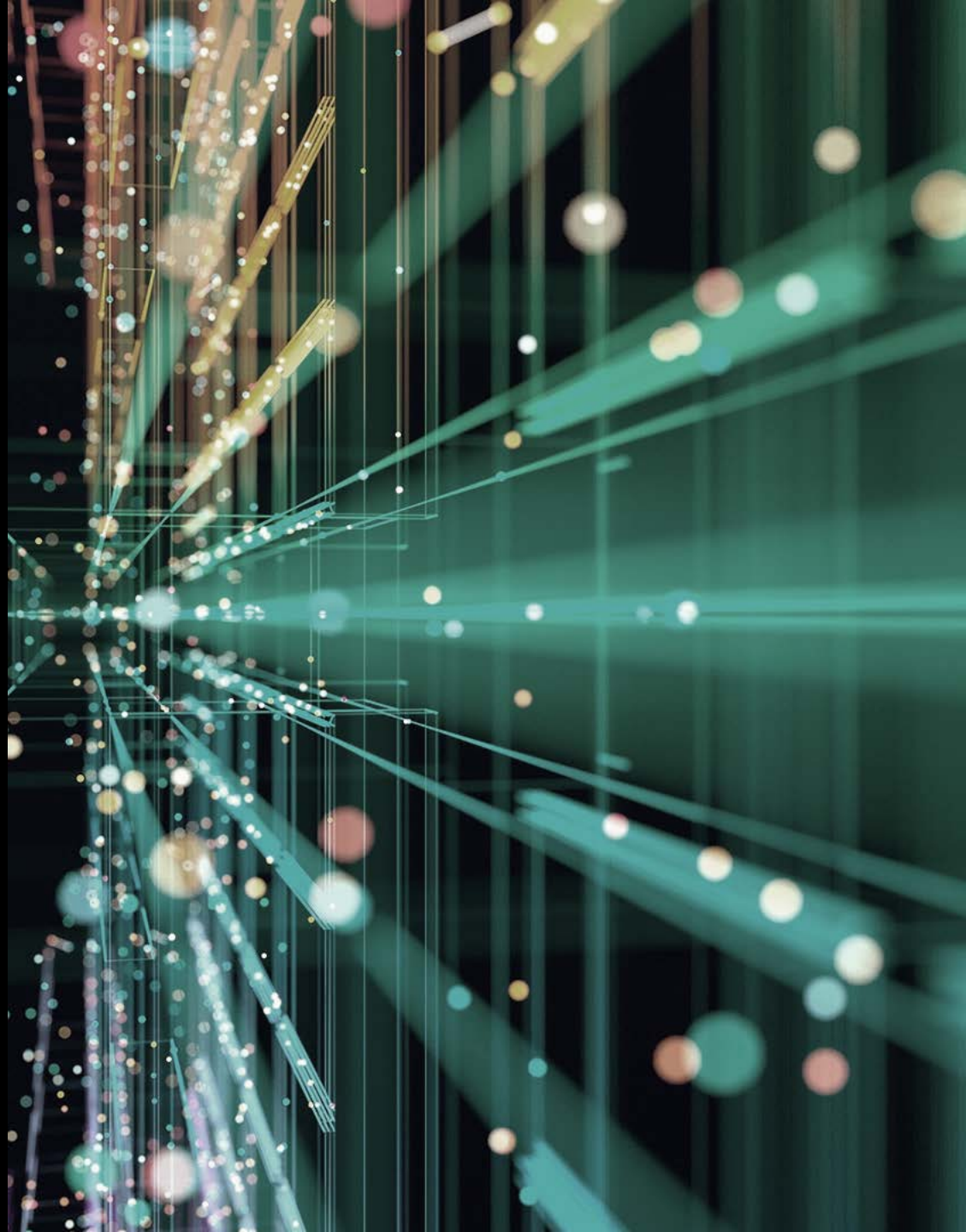
- Manufacturing cycle-times are increasing
- Chiplet strategy reduces design-to-production window
- Need to accelerate learning (Yield, Cost, Quality)
  - Time-to-find
  - Time-to-debug
  - Time-to-deploy

FUTURE OF TEST

- Continue to enhance DFT
  - Die-to-Die Interconnects (2.5D & 3D)
  - Power & Performance
  - Quality & Reliability
- Continue to integrate (“blend”) test methods across various test platforms
  - ATE vs SLT vs Burn-in
- Accelerate Time-to-Learn
  - First-Time-Right (FTR)

AMD

PROBE CHALLENGES



PROBE CHALLENGES

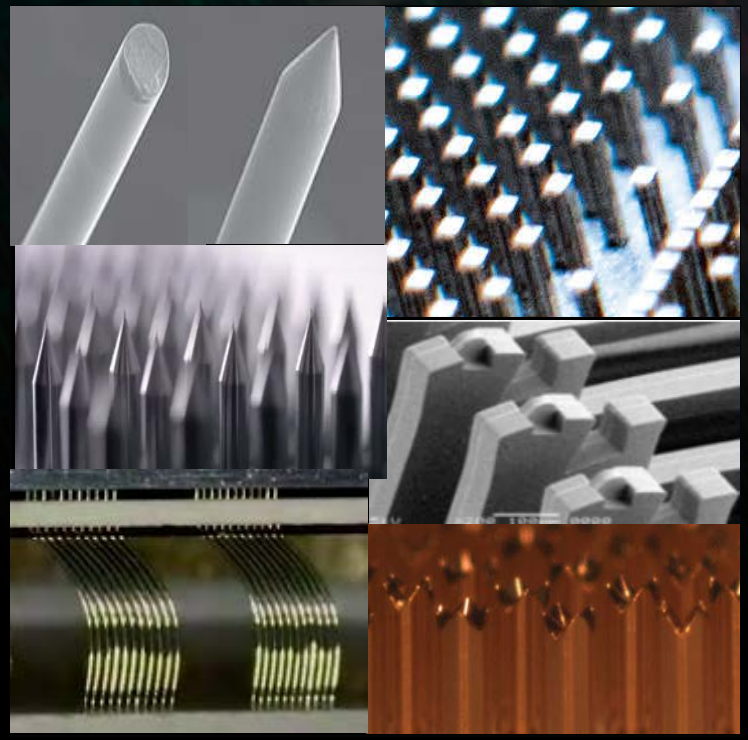
Mechanical : Smaller Pitches & sizes - Bump vs Pad | Multi-site

Thermal & Power : Burned Probes – CCC/MAC | CRES

Electrical : DC vs High-Speed | Signal Integrity

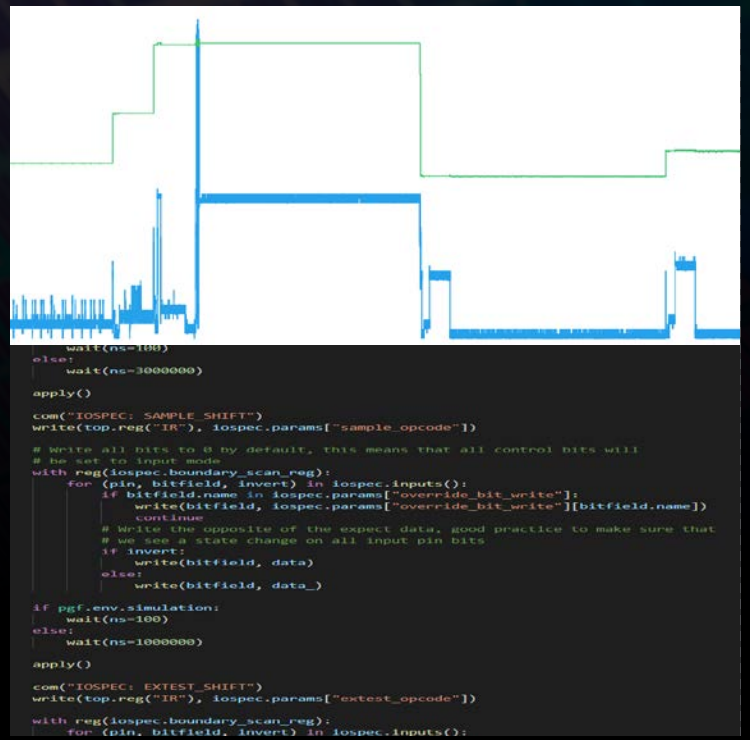
Reliability of Test : >1M Touchdowns | Contact Integrity (FTR)

PROBE SOLUTIONS



CONSTRUCTION

METALLURGY



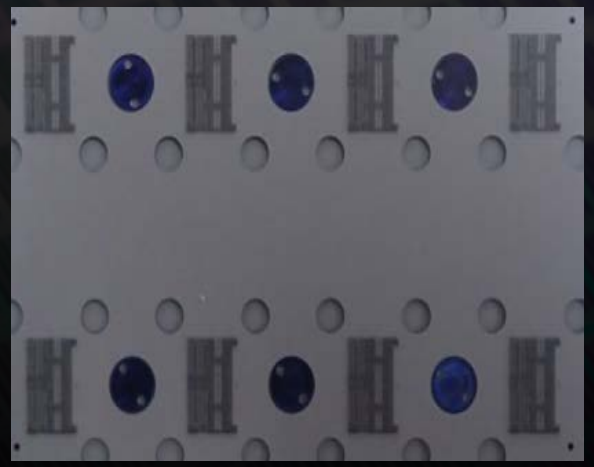
```
    wait(ns=100)
else:
    wait(ns=3000000)

apply()

com("IOSPEC: SAMPLE_SHIFT")
write(top.reg("IR"), iospec.params["sample_opcode"])

# Write all bits to 0 by default, this means that all control bits will
# be set to input mode
with reg(iospec.boundary_scan_reg):
    for (pin, bitfield, invert) in iospec.inputs():
        if bitfield.name in iospec.params["override_bit_write"]:
            write(bitfield, iospec.params["override_bit_write"][bitfield.name])
            continue
        # Write the opposite of the expect data, good practice to make sure that
        # we see a state change on all input pin bits
        if invert:
            write(bitfield, data)
        else:
            write(bitfield, data_)

if pgf.env.simulation:
    wait(ns=100)
else:
    wait(ns=1000000)

apply()

com("IOSPEC: EXTEST_SHIFT")
write(top.reg("IR"), iospec.params["extest_opcode"])

with reg(iospec.boundary_scan_reg):
    for (pin, bitfield, invert) in iospec.inputs():
```

TEST METHODS

IMAGE SOURCE: Probe vendors public web

IMAGE SOURCE: AMD

CHIPLETS : MORE MULTI-SITE OPPORTUNITES

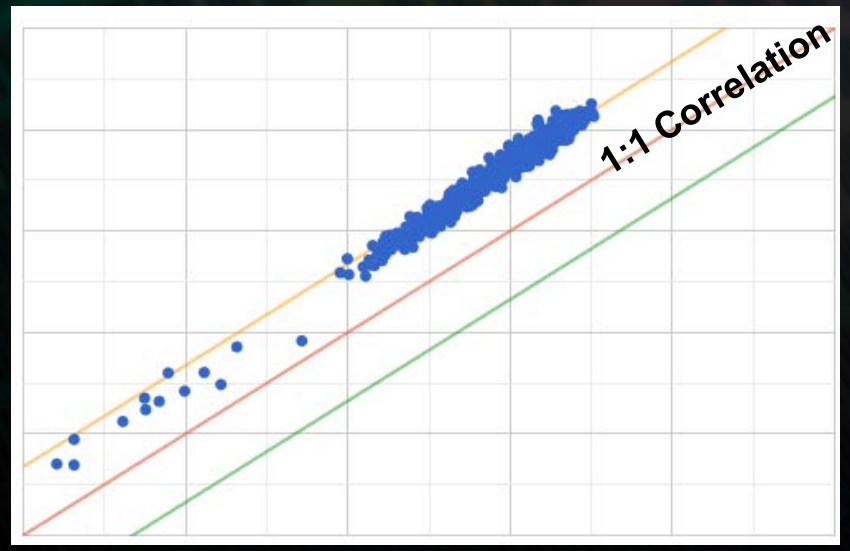


Smaller Die ➡ Less Power & Signals per Chiplet ➡ Increased Multi-Site

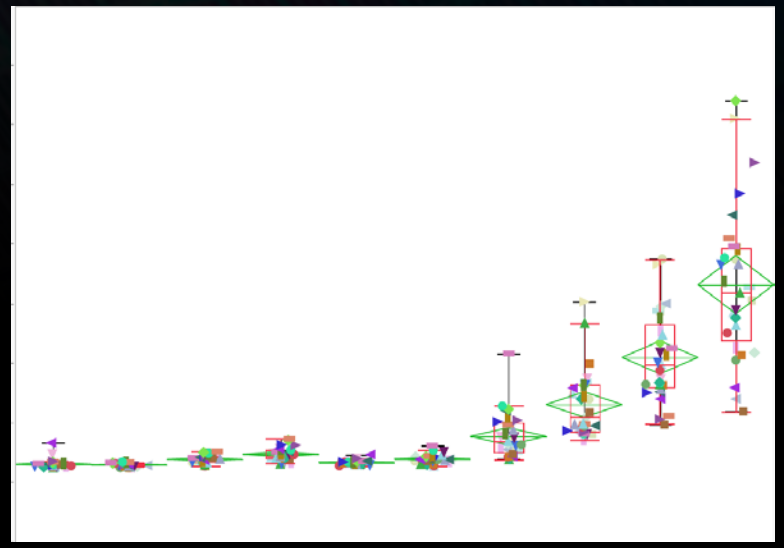
Limited by ATE Instrumentation , MLO size, Probe Count, Probe Force, Planarity, …

IMAGE SOURCE: AMD

TEST SENSITIVITY TO CRES

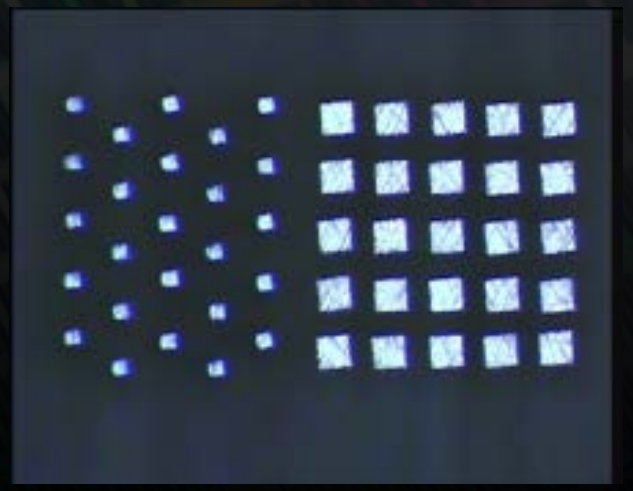


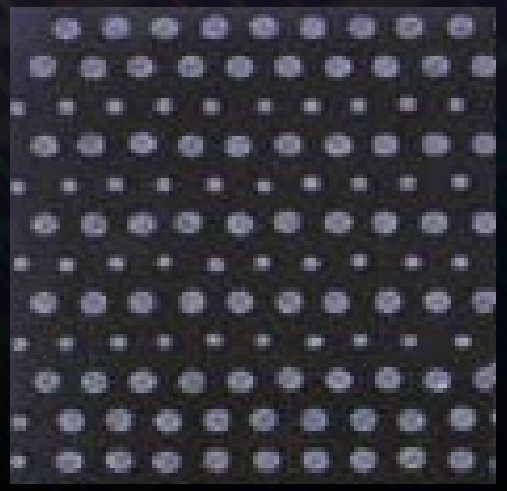
- **CRES** needs to be lower & consistent
- **Test Methods** need to be neutral to Probe effects



SOURCE: AMD

HYBRID : USING THE RIGHT PROBE PER APPLICATION





Mixing & Matching different Probe types into same Probe Head
Higher Power (CCC) vs Higher Speed (I/O)

SOURCE: AMD

FUTURE OF PROBE

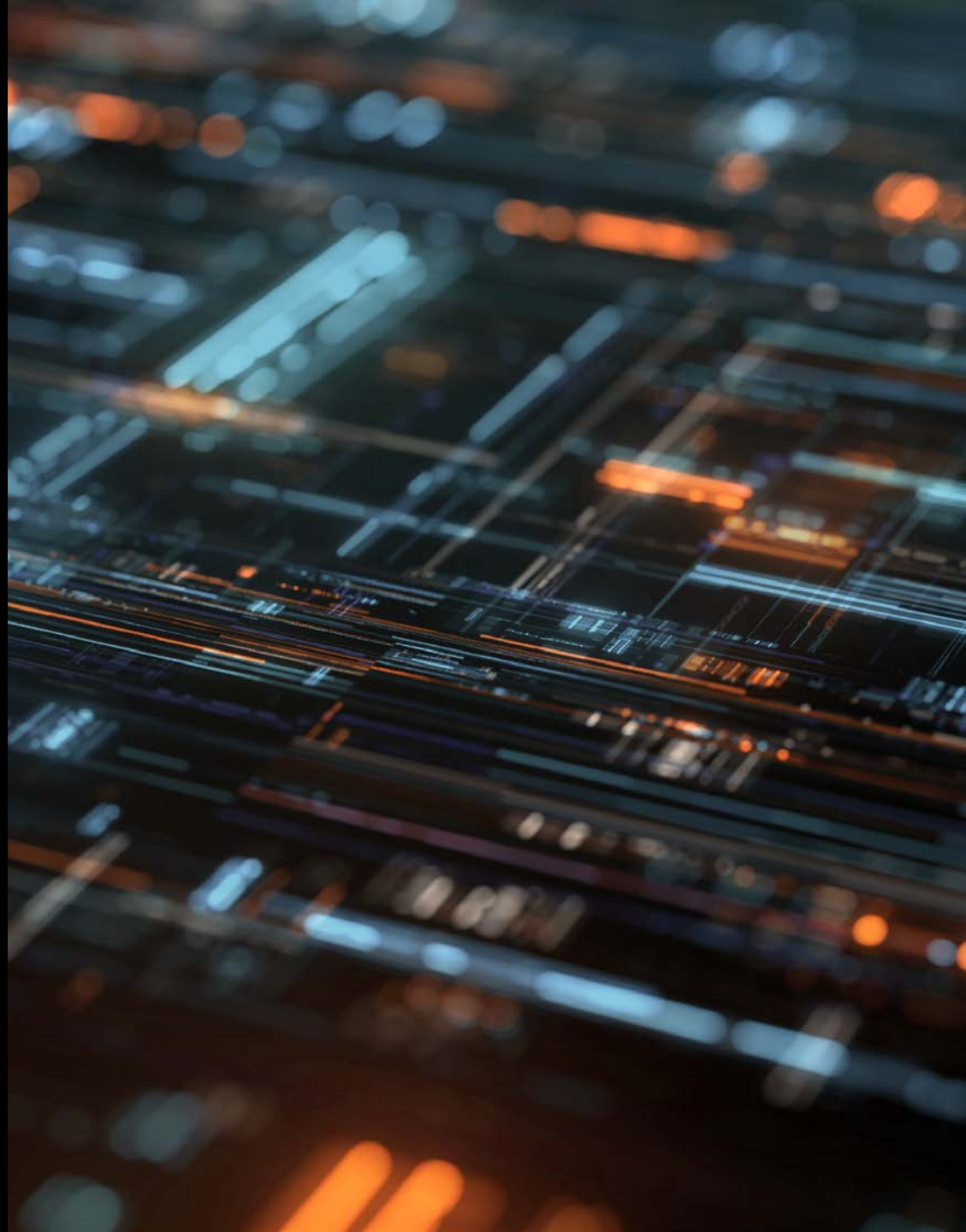
- **Adapt to Advanced Fab & Package Technologies**
  - Finer Pitch
  - Bump & Pad Geometry & Metallurgy
  - High Power Density
  - Increasing Parallelism

- **Adapt to changing Test Methods**
  - DFT
  - System-Level Test
  - Reliability Test

- **Maintain & Improve Past Performance**
  - First-Contact Integrity
  - Touchdown Lifetimes
  - Cost Neutral

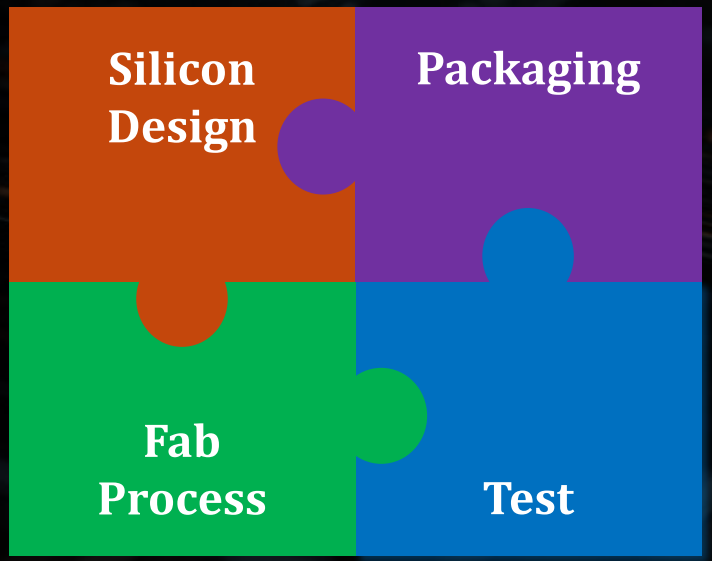
AMD

CONCLUSION



INNOVATION THROUGH COLLABORATION

Development of Key Technologies Require Early Engagement & Collaborations

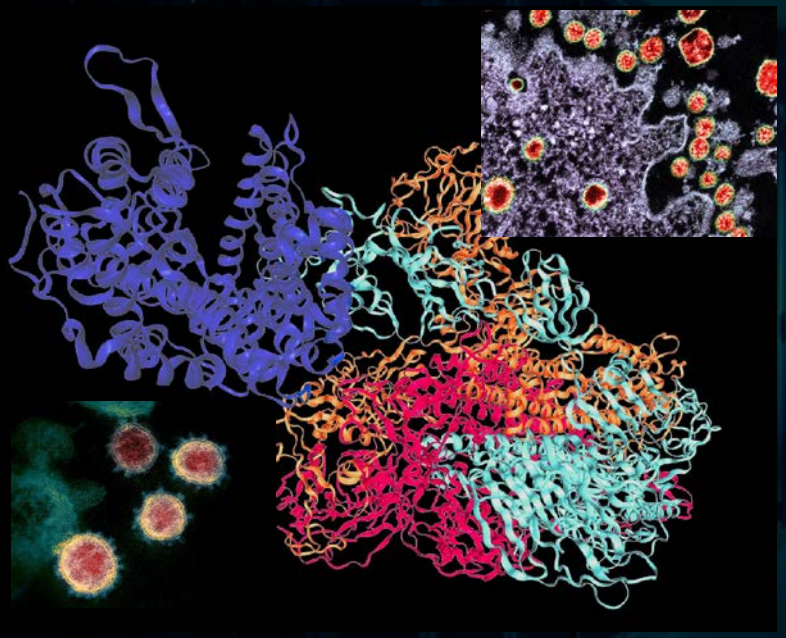


Vendor Co-Development

- EDA Tools
- OSATs
- Test Hardware Providers

…

ACCELERATING LIFE SCIENCES : THE HUMAN TOUCH

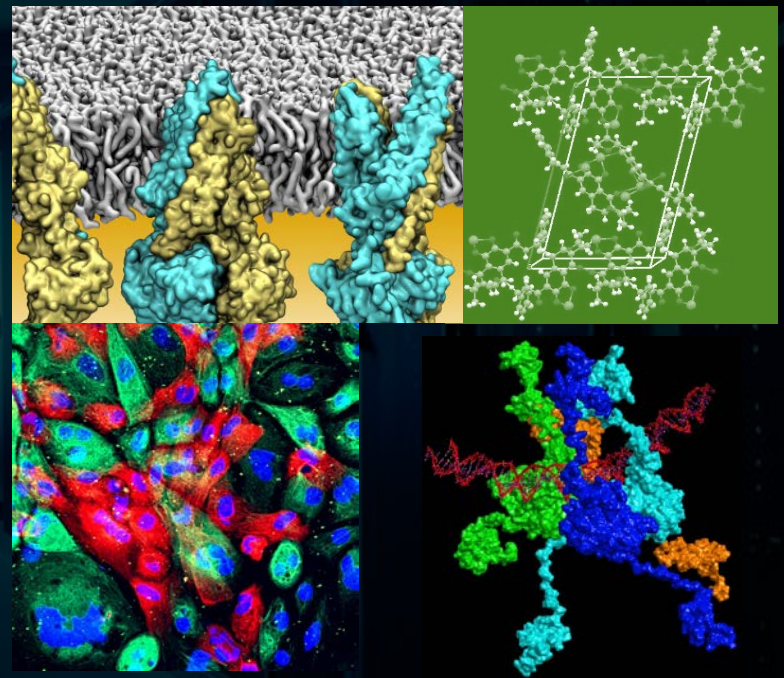


COVID-19 HPC Consortium

6.4M CPU Cores + 49K GPUs

Industry [10] + Academia [17] + National Labs

Source: covid-19-hpc-consortium.org



Cancer Research

Early Detection & Enhanced Treatments

"Supercomputers are key to the Cancer Moonshot"

As Vice President, in 2016, Joe Biden launched the Cancer Moonshot with the mission to accelerate the rate of progress against cancer

SOURCE:
www.amd.com/en/case-studies
Oak Ridge National Lab
https://www.hpcwire.com/2017/05/31/cancer-research-supercomputing-perspective/
https://www.cancer.gov/research/key-initiatives/moonshot-cancer-initiative

CONCLUDING REMARKS

- Evolving Market Needs
- Accelerating Compute Product Releases
- Innovating Test Solutions

- BE INSPIRED TO INNOVATE

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4. R. Swaminathan, “Enabling Moore’s Law’s Next Frontier Through Heterogeneous Integration,” 3DIC, Nov. 2021.

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