Introduction of New Ceramic Technology

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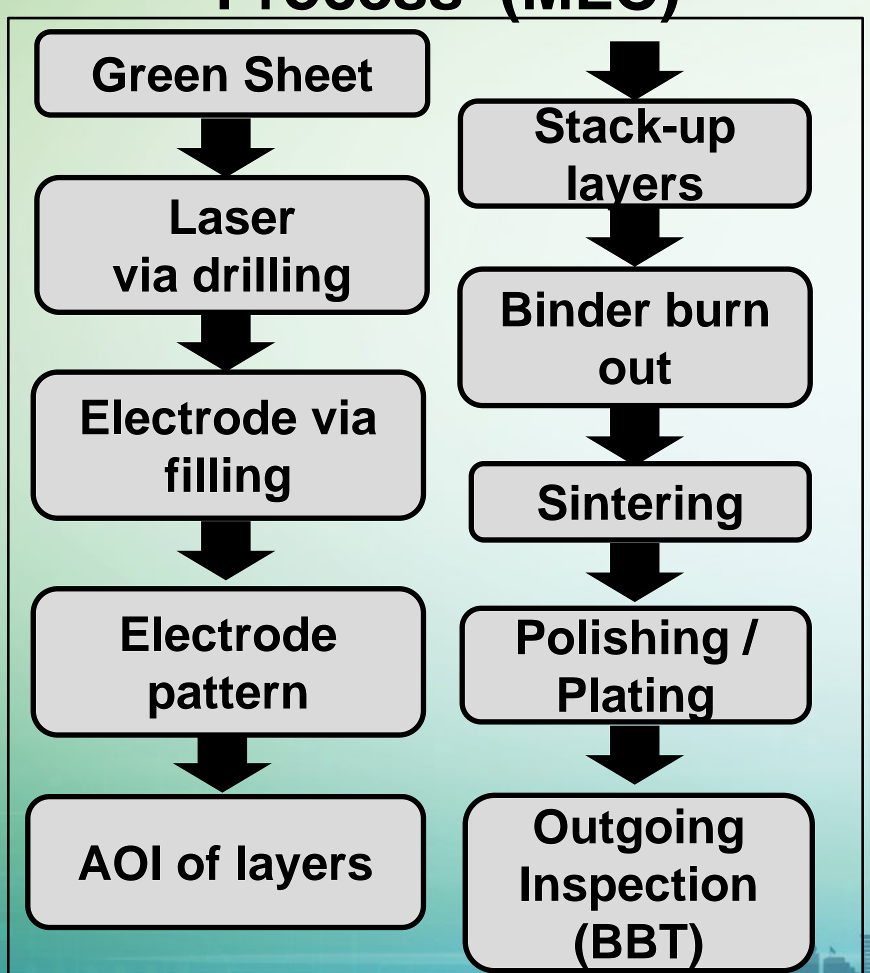
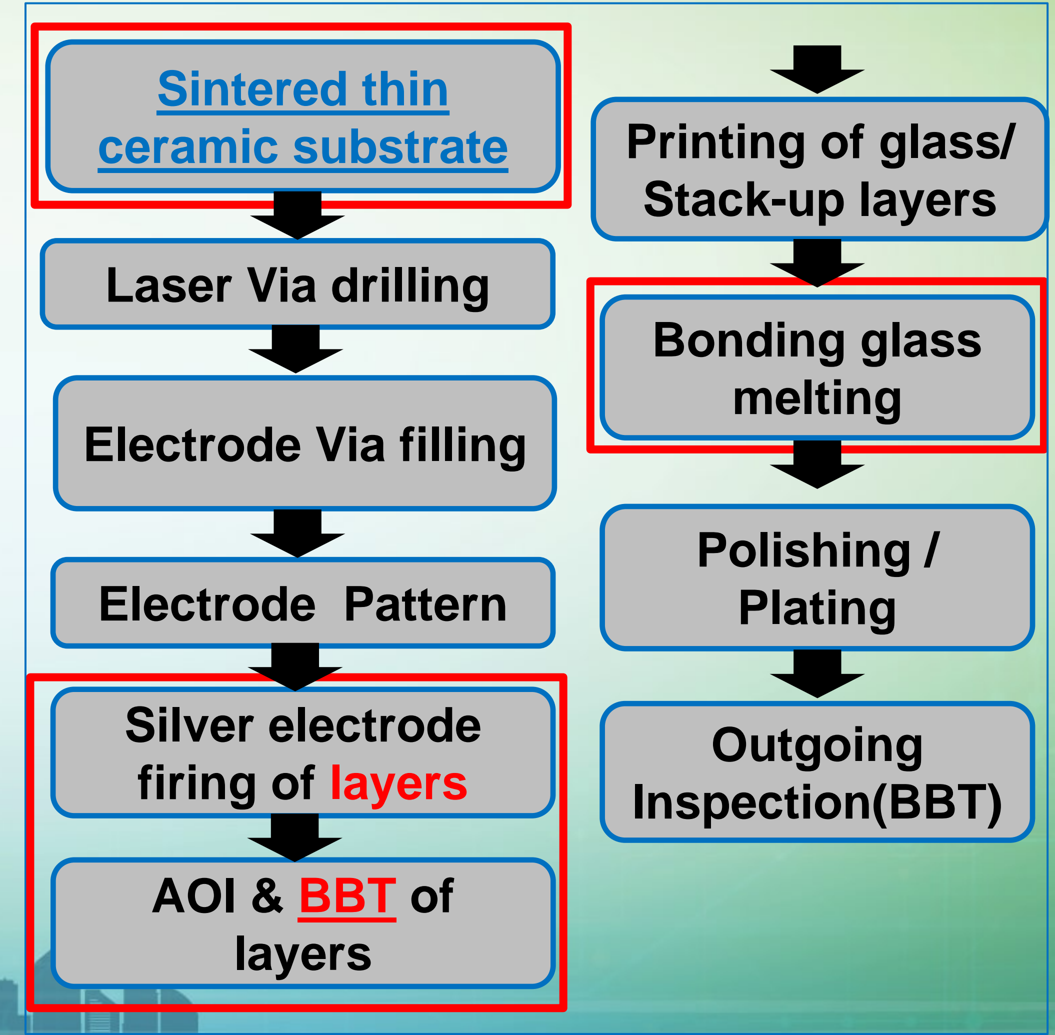
Introduction and Patent information

- R&D started 14 years ago (2008)
- What would be the future of MLC technology for probe cards?
- Would the MLC process be viable for future probe cards?
- Can it satisfy the specs that future consumers need? (# of holes, fine pitch)
- Can the current limitations for MLC be overcome?
- What would be the alternatives and new technology
- Ceramic substrate creation and production patent accepted in KR, JP, TW with US, CN, EP pending

MSC: Multi Stacked Ceramic

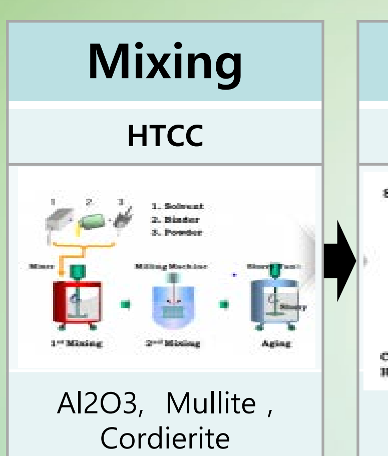
New Process Comparison

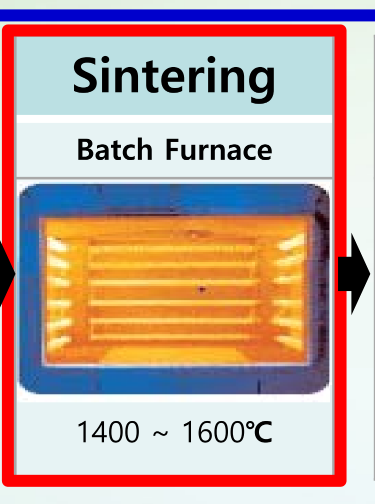


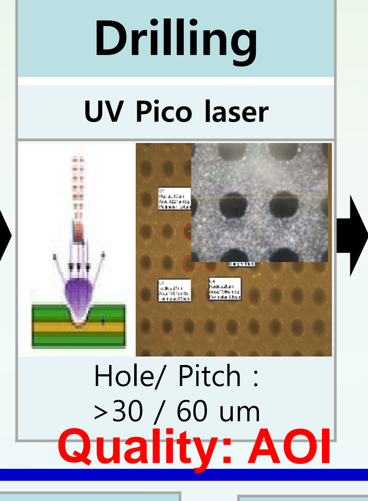


Detailed MSC Process Flow

New Materials & Process







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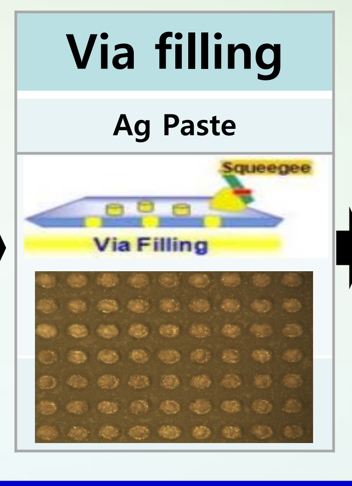
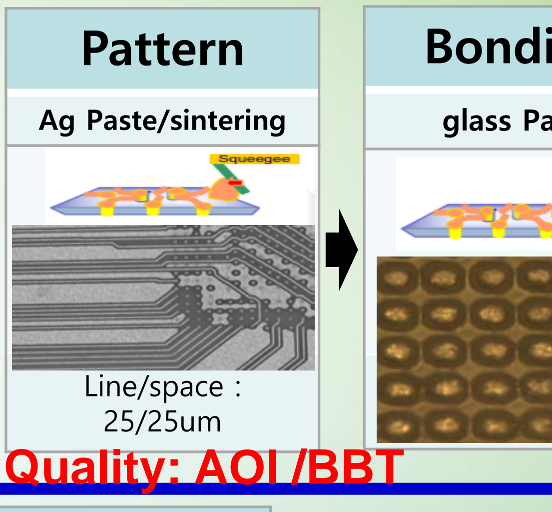
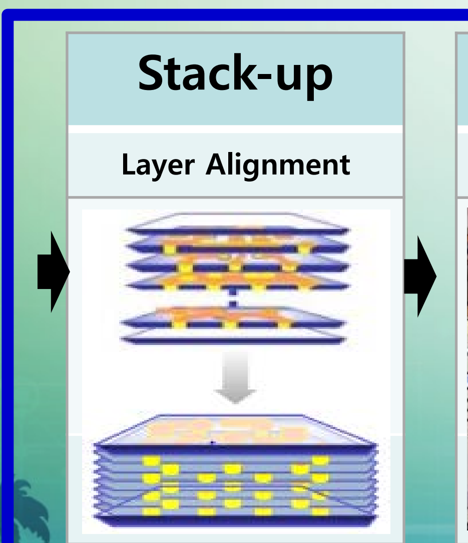
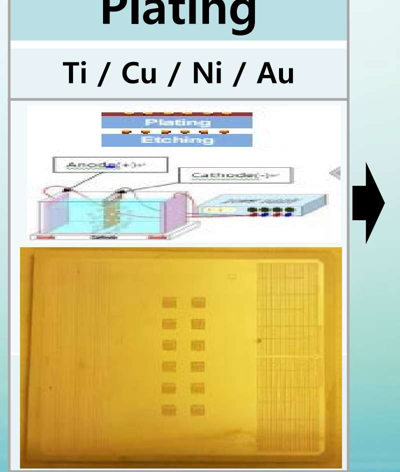
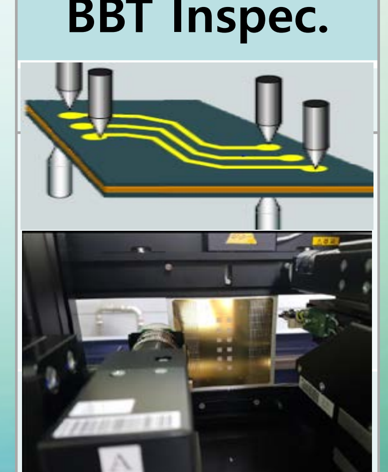




Quality: AOI /BBT







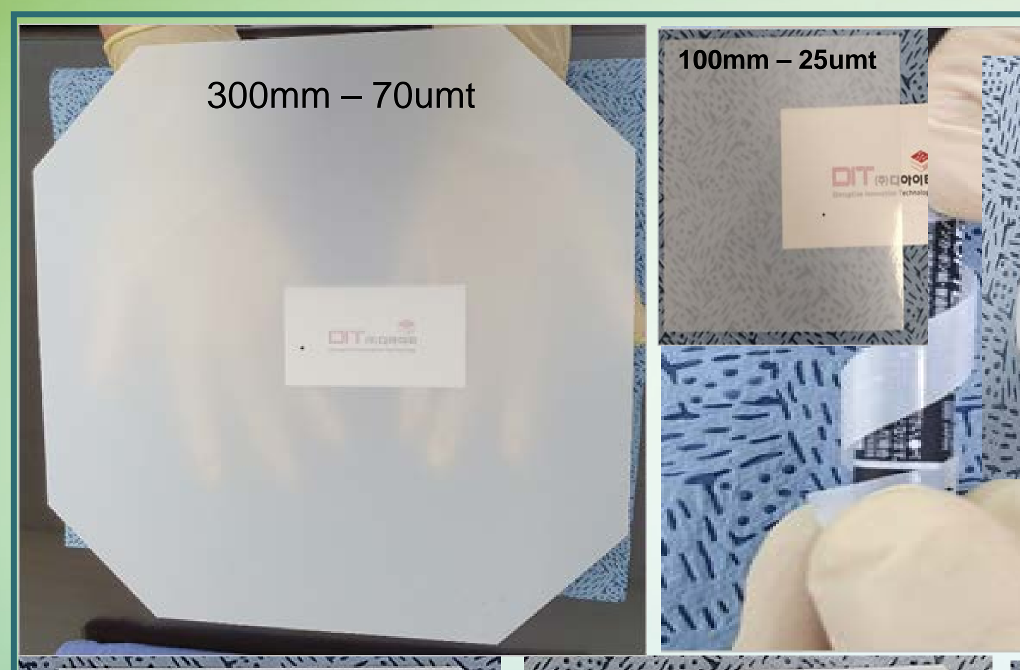
MSC: Multi Stacked Ceramic

Why MSC?

Key Tech needed for MSC

- Customizable raw material and ceramic composition.
- Customizable ceramic structures.
- Thin ceramic substrate mass production.
- Micro via laser Drilling.
- Electrode via filling.
- Fine pitch electrode patterning.
- Via alignment stacking technology
- House made monolithic layer production commercialization

Different Types of Ceramic Substrates

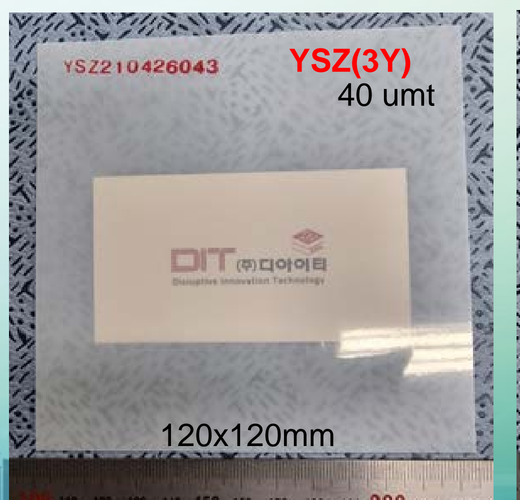


100mm – 25umt

No Grinding!!!

No Polishing !!!!

Category	Spec.
Ceramic Material(100%)	Al2O3, Mullite, Cordierite, .. All oxide
Thickness(um)	>25
Size(mm)	<340
TTV, BOW, Warp.(um)	<±2
Ra(um)	0.8

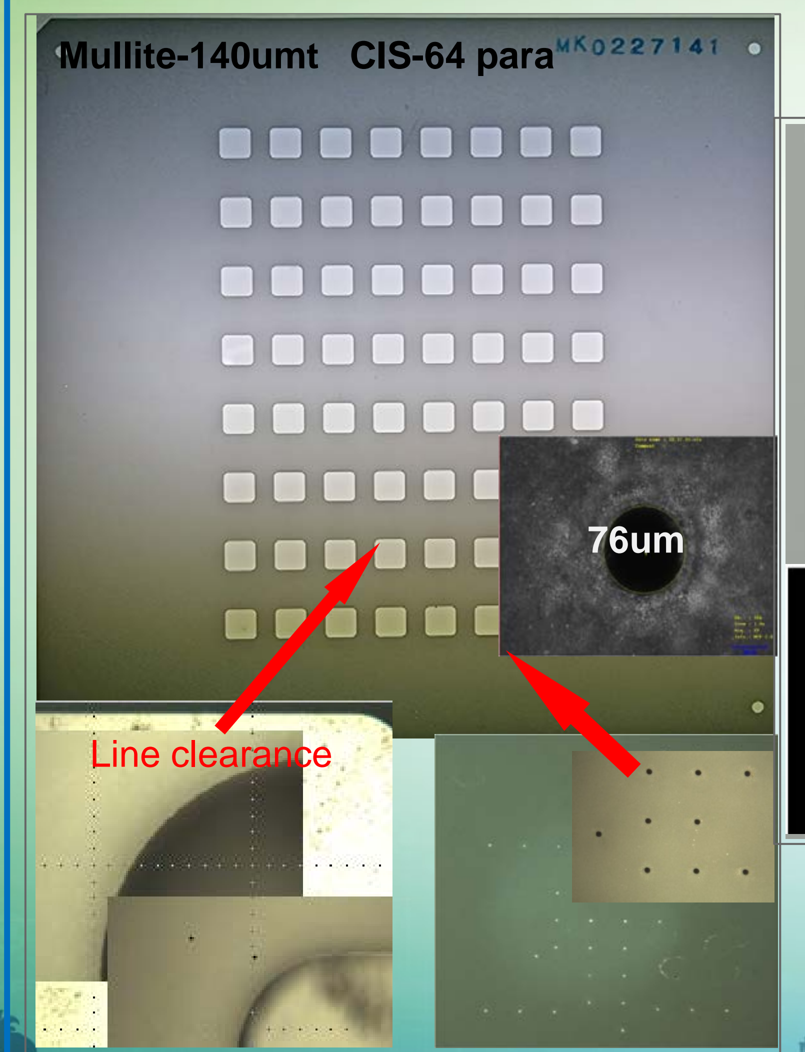


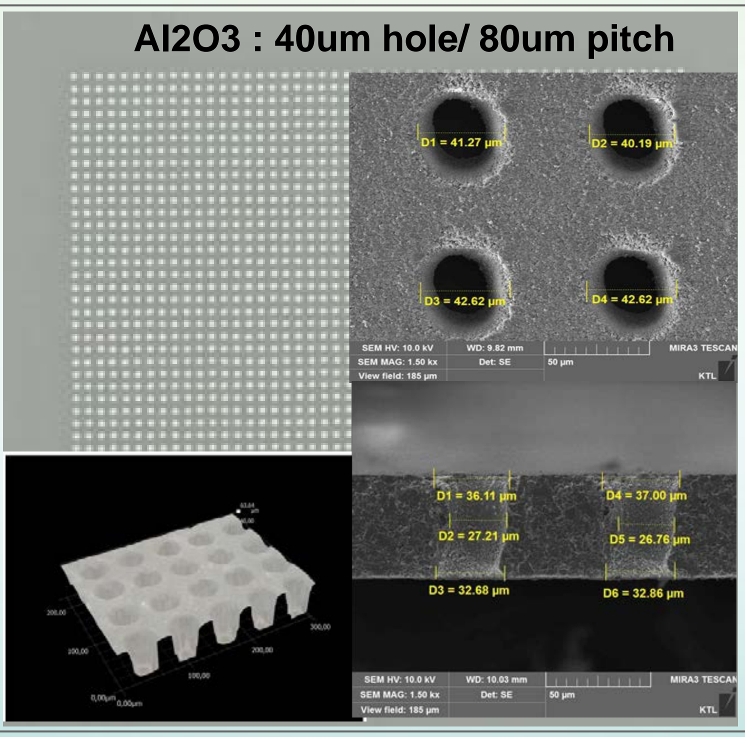
Alumina+Codierite
50 umt
120x120mm

Characteristics of ultra thin ceramic substrates

Substrate Material Properties	ceramic substrate		Etc.
1. Ceramic Materials	Based-Al2O3	Based-Cordierite Based-Mullite	control composition
2. Dielectric Constant(1MHz)	8~11	8~6	
3. Dielectric Loss(x-4)-(1MHz)	1~10	12~20	
4. Thermal Conductivity (W/m-K)	12~28	4~10	
5. Coefficient of thermal expansion(ppm/℃)	7~12	5~7	
6. Bulk density (g/㎤)	3.6	3.2	
7. Flexural Strength (Mpa)	300~400	280~350	
8. Young's modulus of Elasticity(Gpa)	380	200	
9. Heat capacity (J/g-K)	0.7	0.7	
10. Sintered Ceramic size(mm), Max.	340	340	
11. Sintered Ceramic Thickness(um), Min.	25	25	Special : 20um

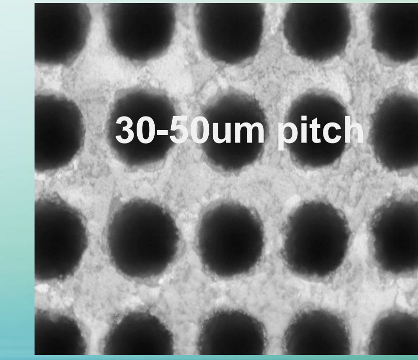
Laser Drilling Capabilities

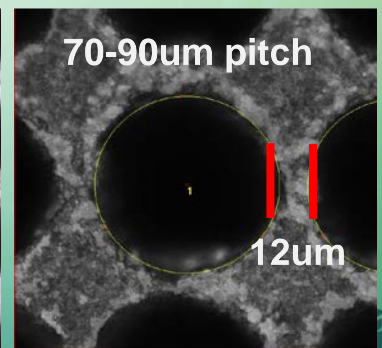




Category	Spec.	
Laser drilling mass production	UV Pico sec (12 watt)	120holes /sec
	Green Nano (60 watt)	360holes /sec
Hole size	>30um(50umT)	
Via to Via pitch	>60um	
Taper ratio	>70%	
Via position tolerance	<± 5um	

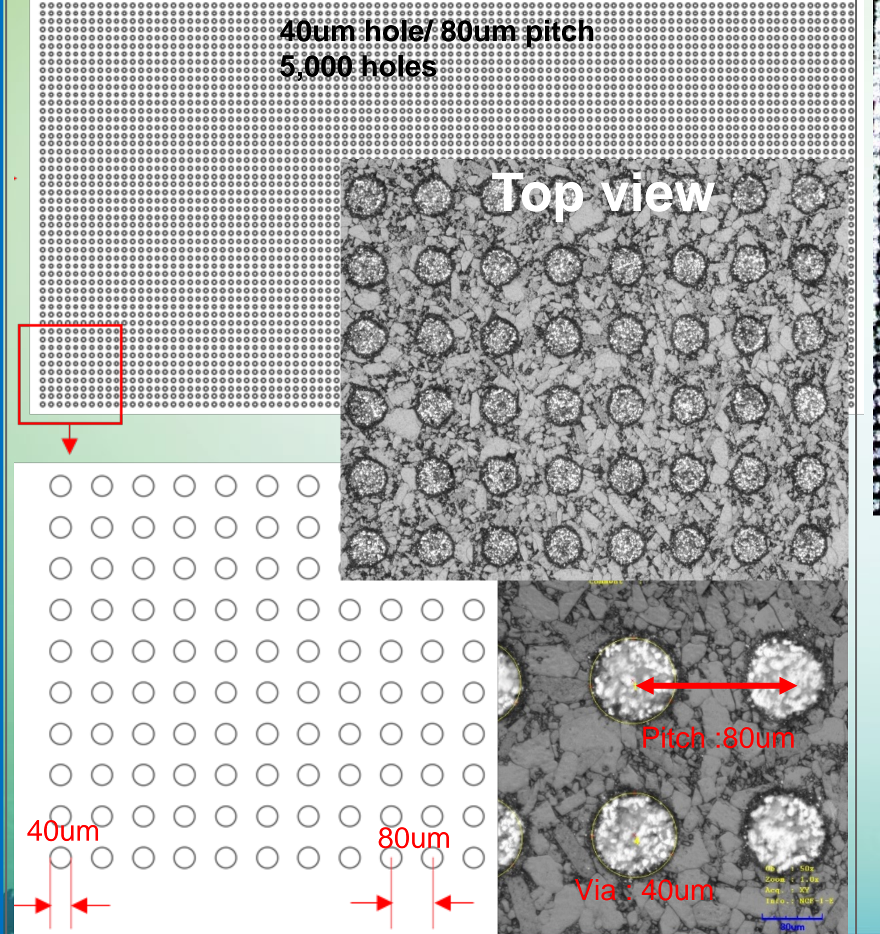
Drilling best condition





Via Filling Capabilities

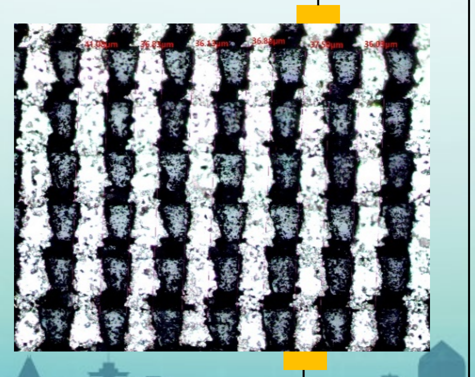
design of Via filling



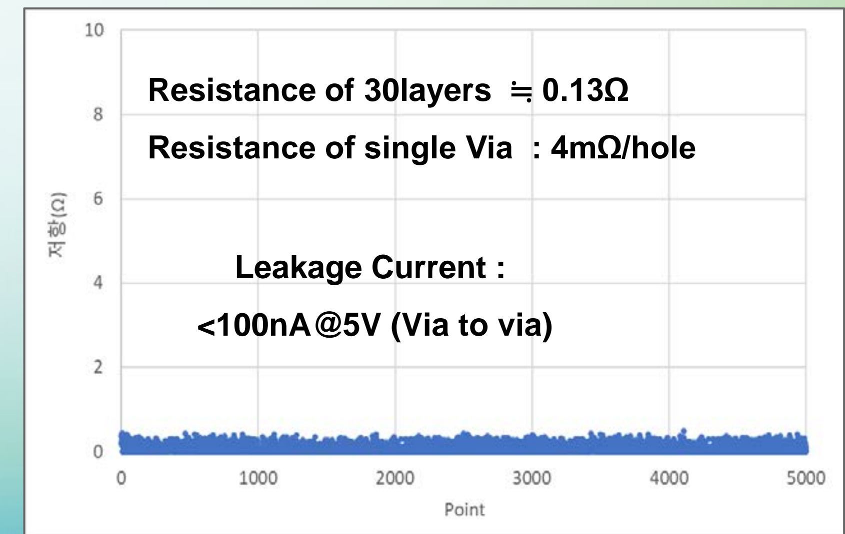
View cross section

30 layer stack-up

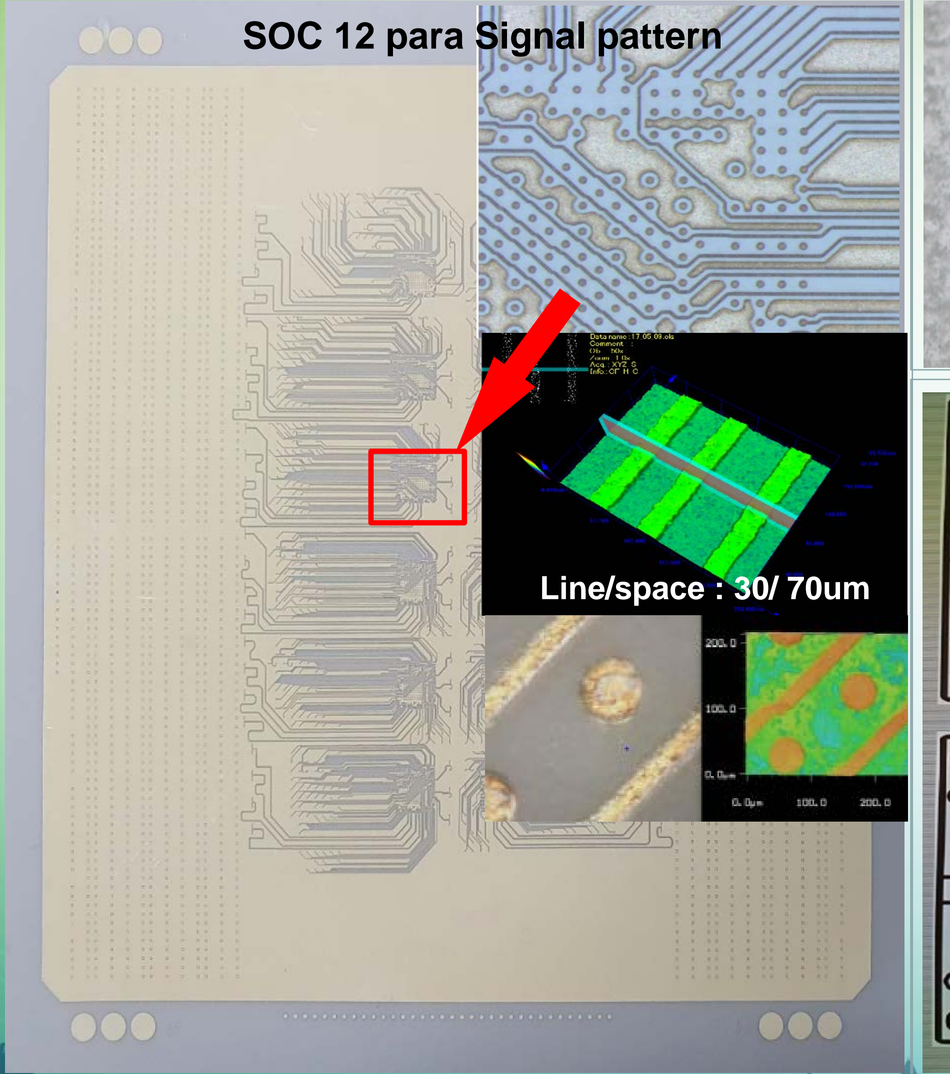
Category	Spec.
Via fill material	Pure Silver metal
Hole size	>30um(50umT)
Via to Via pitch	>60um

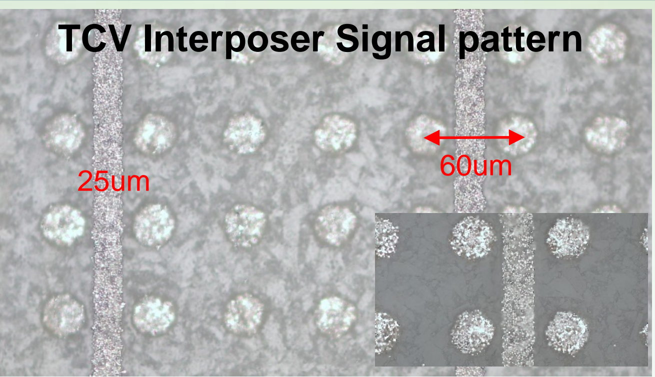


BBT TEST

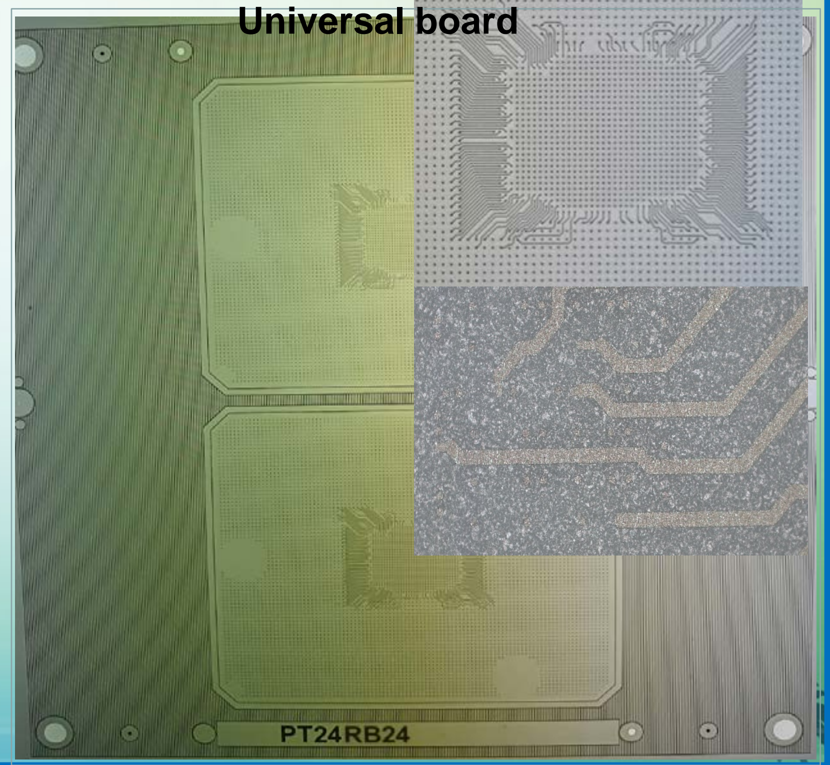


Patterning Capabilities



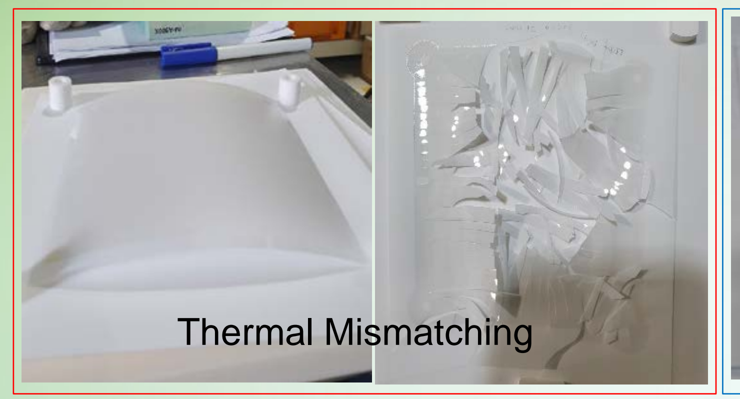


Category	Spec.
Pattern material	Pure Silver metal
Pattern	Line/space : >25/25um
Metal thick.	> 6um

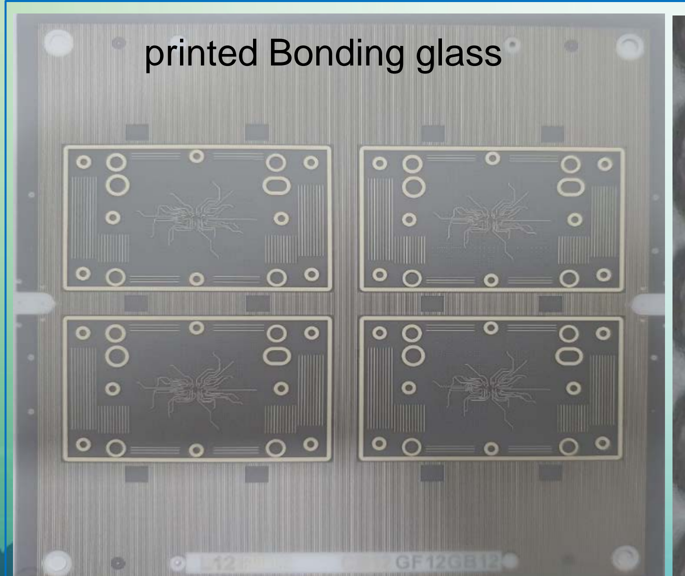


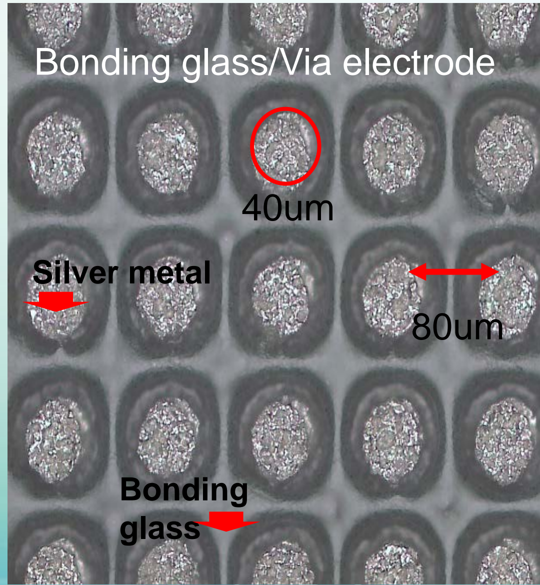
Ceramic Glass Bonding Capabilities

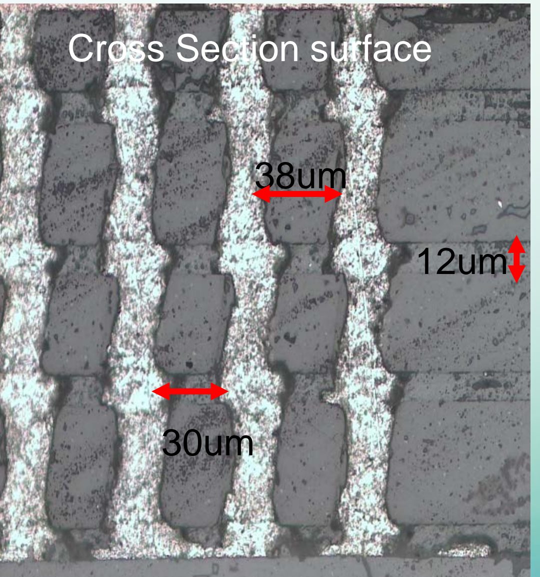
Thermal matching test @ Al2O3 substrate



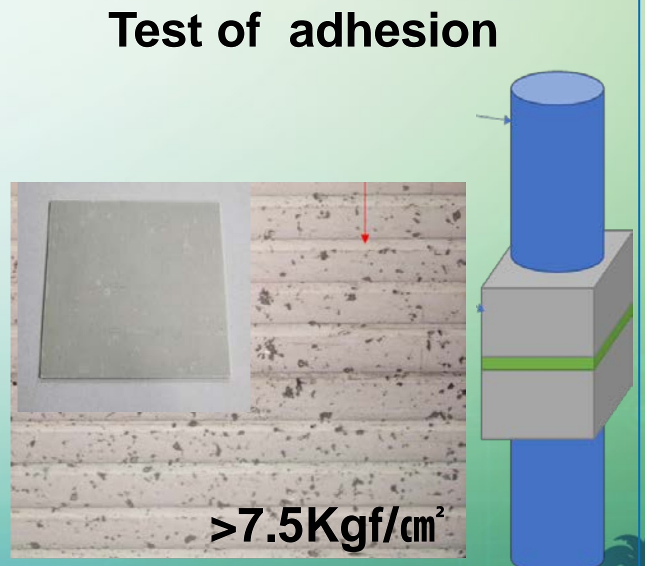
Category	Spec. (@Al2O3 substrate)
Glass Type	borosilicate glass
Thermal Expansion	6.6×10^{-6}℃(40-400℃)
Tg temperature	590℃
Bonding force	>7.5kgf/cm2



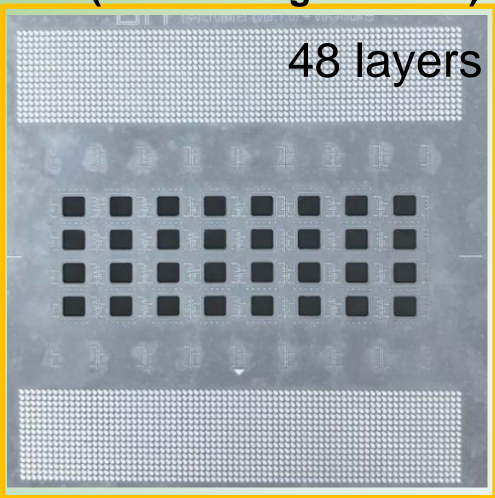


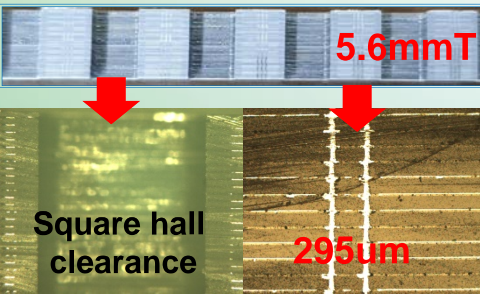


Test of adhesion



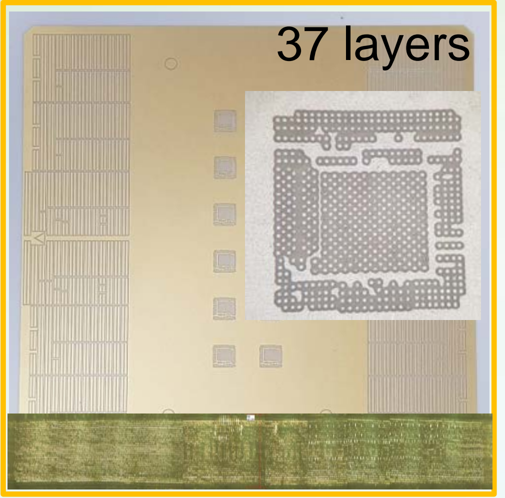
MSC Samples



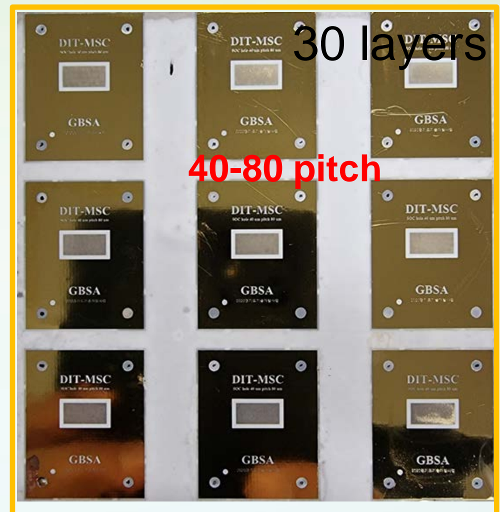


Via size : 80um
Pad size : 140um
Via pitch: 350um
Pad to pad clearance : 70um

SOC (System On Chip)

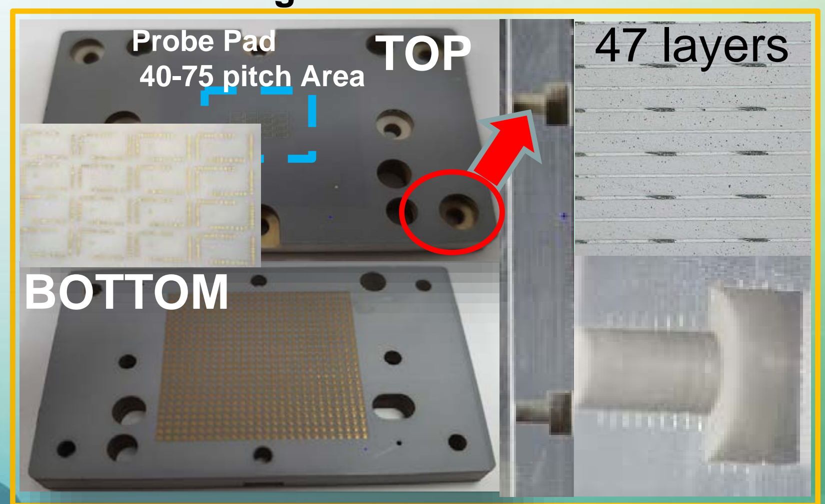


TCV interposer test sample



Category	Spec. (@Al2O3 substrate)
Stack up temp.	700℃
Via alignment tolerance	<± 5um

Various geometrical structures



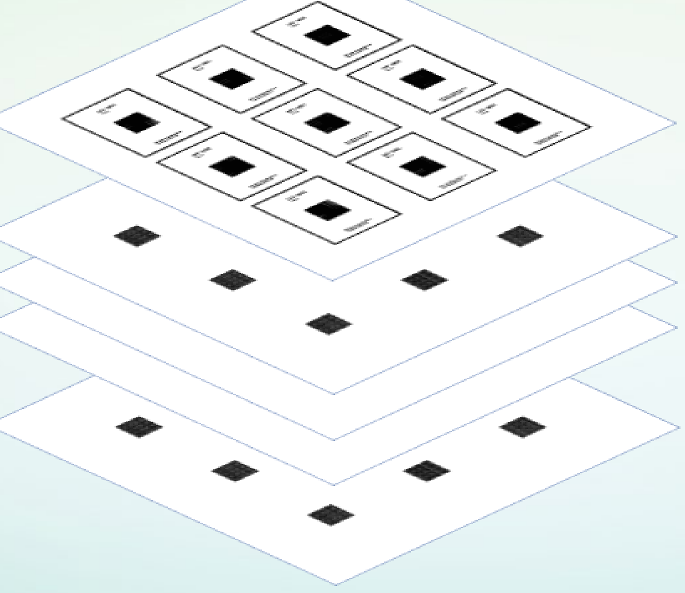
IL Crosstalk Daisy chain coupon(#1)

1. Design Diagram & Material properties

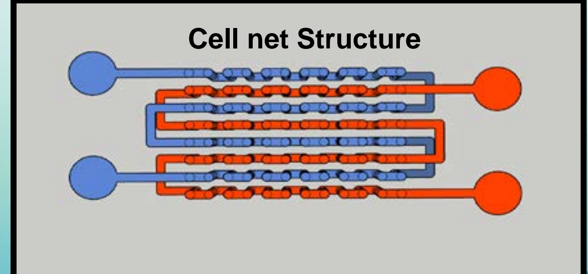
MSC Stack-up layer

Layer No.	Name	Material
1	Top Pad	Au, Ni, Cu, Ti
	Substrate	Alumina
	Bonding layer	Glass
2	Pattern	Ag
	Substrate	Alumina
	Bonding layer	Glass
3	Pattern	Ag
	Substrate	Alumina
	Bonding layer	Glass
4	Pattern	Ag
	Substrate	Alumina
	Bonding layer	Glass
5	Pattern	Ag
	Substrate	Alumina

MSC Stack-up diagram



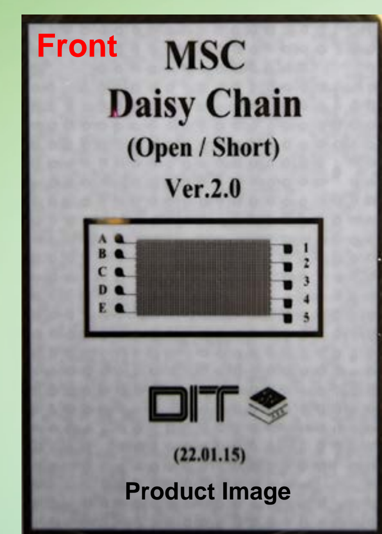
Cell net Structure



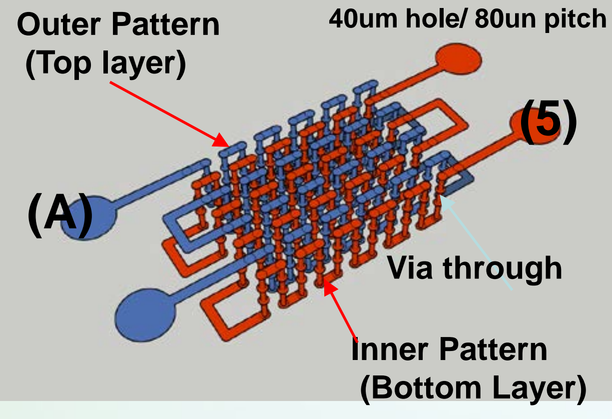
Substrate	Ceramic	Al_2O_3
	Dielectric constant	11.2
	Dielectric Loss	0.002
Metal	Inner Pattern	Ag
	Outer Pattern	(Ti-Cu)-Cu-Ni-Au Plating
	Via	Ag
Design	Layer Thickness	55㎛
	Total Layers	5
	Bonding Thickness	10㎛
	Via Size / Pitch	40㎛ / 80㎛
	Via number of one layer	4,800 holes/cell
	Total via number	19,200 holes/cell (4 layers)
	Top Pad Size	50㎛

IL Crosstalk Daisy chain coupon(#2)

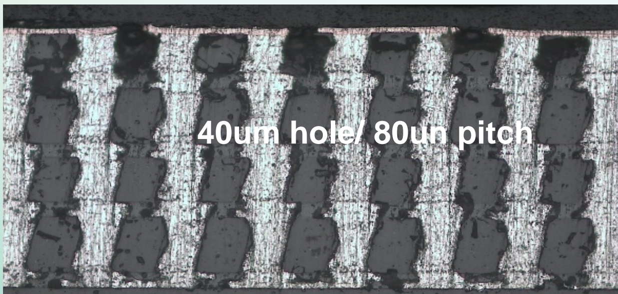
2. Electrical Property (BBT Test)



- Net Structure



- Cross Section surface

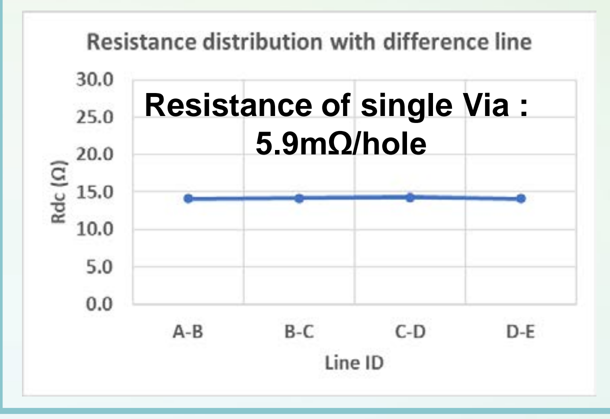


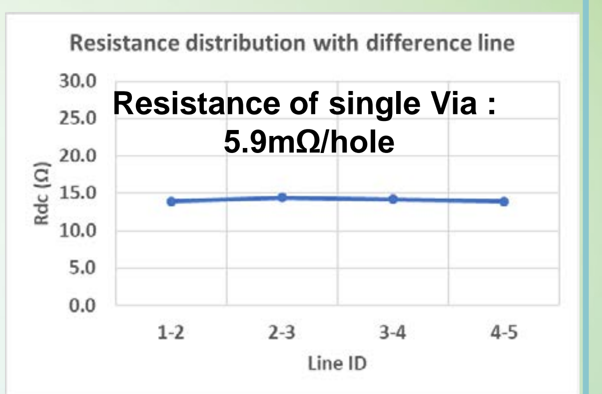
- Leakage Current

A-5 : 0.003uA @5V,
0.015uA @15V
Total via hole : 19,200 via holes

- Resistance of measure. Point

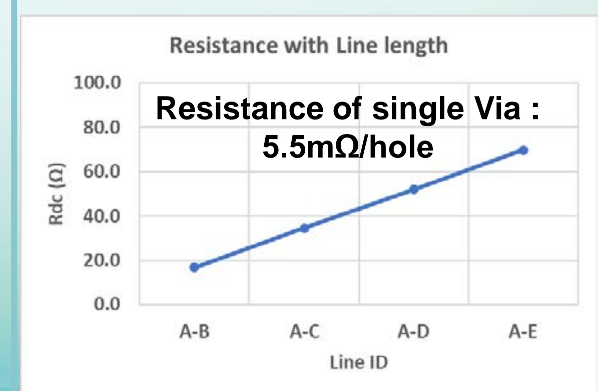
(A-B, B-C, ….1-2, 2-3…, respectively 2,400 via holes/line)

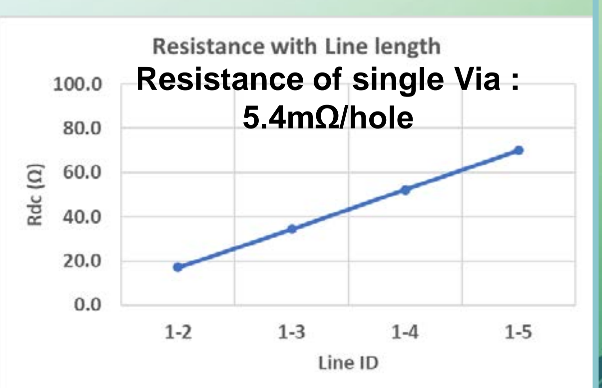




- Accumulated resistance of measure. Point

(A-E , 1-5 Total via hole : Each 9,600 via holes)

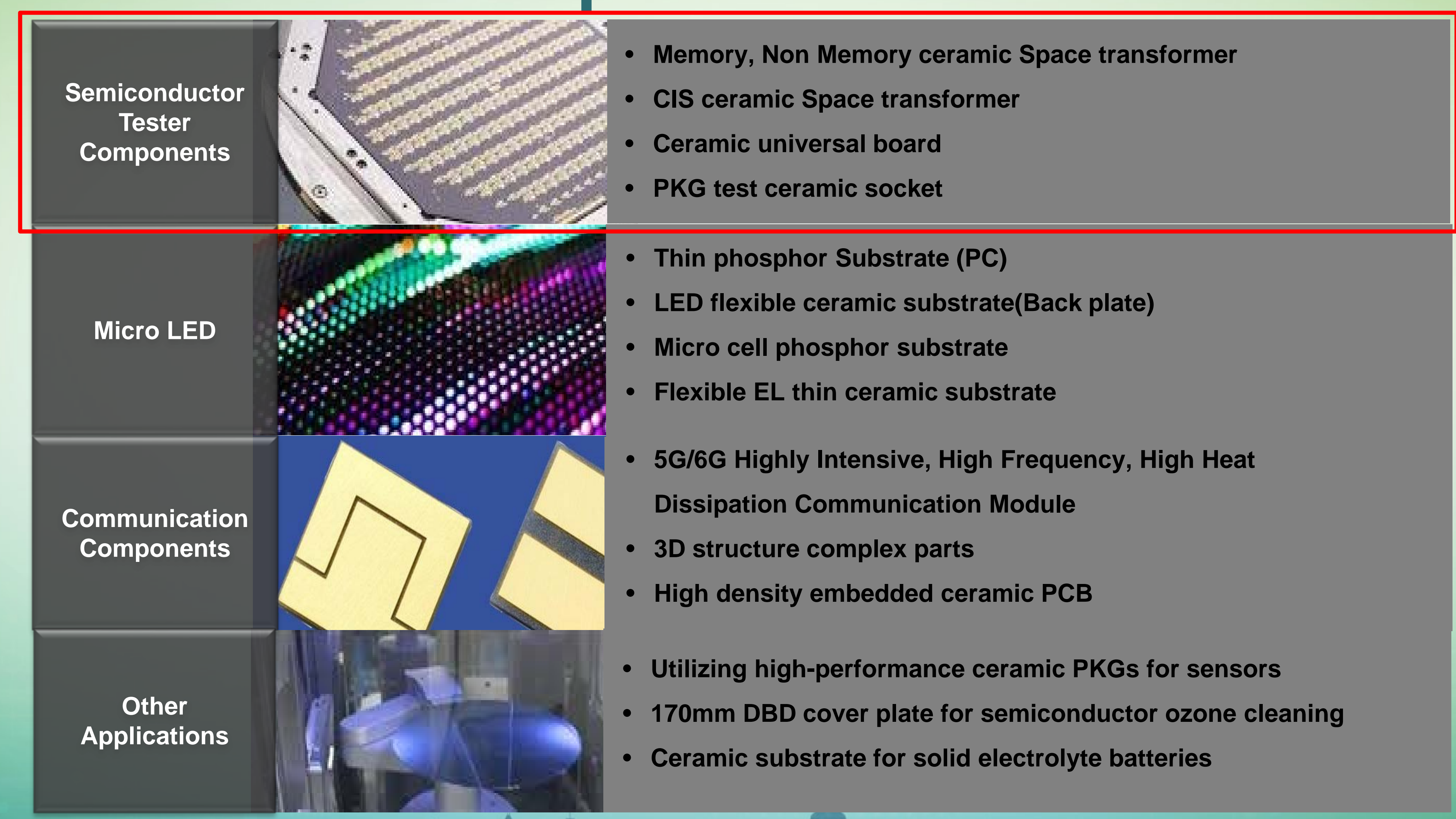




Comparison Between all STFs

List	MSC	MLC(HTCC)	MLO	MSC contents
Materials	Ceramic	Ceramic	PI***	HTCC+LTCC(Glass bonding)
Mechanical Strength	Good	Good	poor	
Thermal Properties	Good	Good	poor	Dependent on ceramic materials
Electrical Properties	Good(Ag)	Poor(Mo-W)	Good(Cu)	
Chemical Properties	Good	Good	poor	
Via pitch shrinkage	Good	poor	Good	No shrinkage
Via size	small	Middle	small	>30um(50umT)
Via to via(Pitch)	small	Middle	small	>60um pitch
Line/ space	Narrow	Middle	Narrow	Line/ space : 25/25um
Small via alignment	Good	poor	Good	<±5um
Layer Count	High	Middle	small	No limit
Cavity layer	Possible	No	No	Micro cavity (For Rf properties)
Mechanical Holes	Good	poor	Not bad	Each layer is drilled first than stacked
Embedded structure	Possible	No	No	Passive component
Polyimide layer	No(All ceramic)	Yes(Ceramic/PI)	Yes	Fine hole, Fine pitch

Where this New Ceramic Technology can be implemented



Future Plans for DIT

- We wanted to introduce the capabilities of this new MSC process through SWTest
- Sharing a solution to the hardships that MLC faces.
- Wanted design engineers to know about this new process so they can now use this technology to their advantage
- DIT still needs small fixes and tweaks to perfect this new process
- We strive to reach more difficult specs with good yield for customers

Thank you for listening

- DIT will be at booth #506 feel free to come if you are interested!

- Author : Tae-hyung Noh (CEO)
- Speaker/Translator: Paul Kim