SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

UFO Probe™ Card
New dimensions in wafer-level test of photonic integrated circuits.

MORE LIGHT

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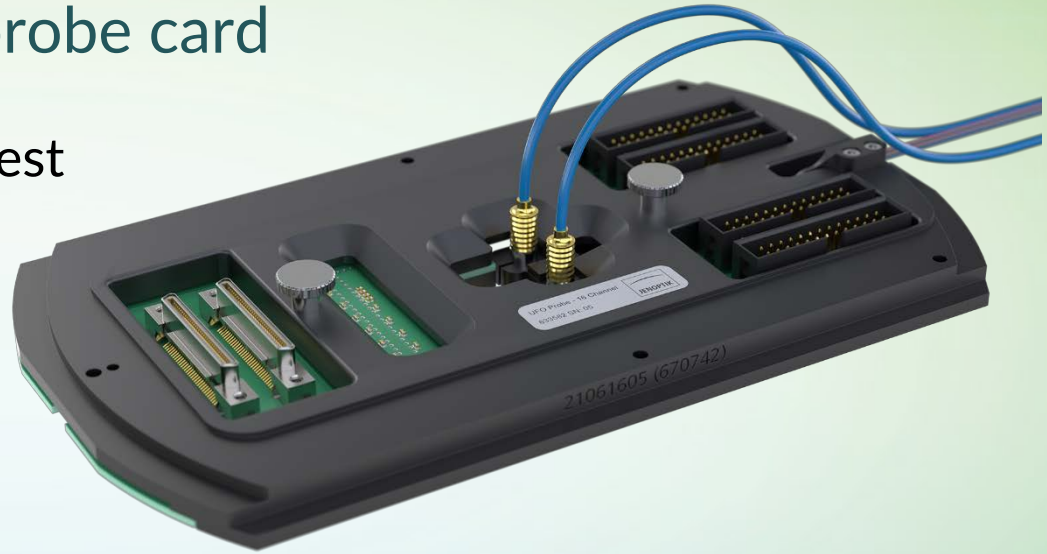
June 5 - 8, 2022

Application

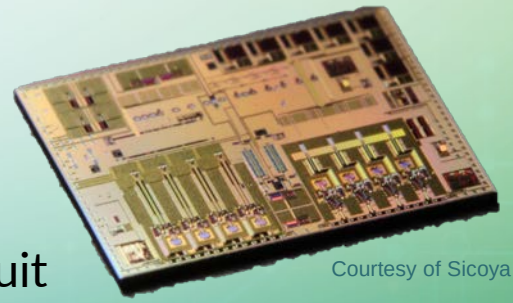
UFO Probe™ – ultra-fast opto-electrical probe card

JENOPTIK's solution for high-volume wafer-level test of photonic integrated circuits (PIC).



Key aspects:

- Targets wafer testing of ICs with integrated optics
- Utilization of existing test ecosystem and procedures
- Uses standard prober and test equipment



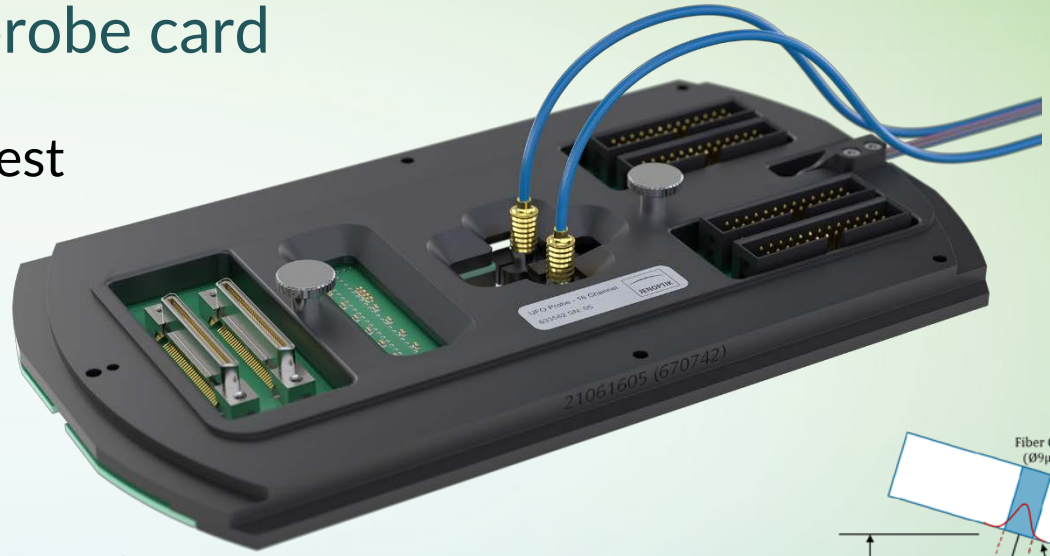
Photonic integrated circuit

Courtesy of Sicoya

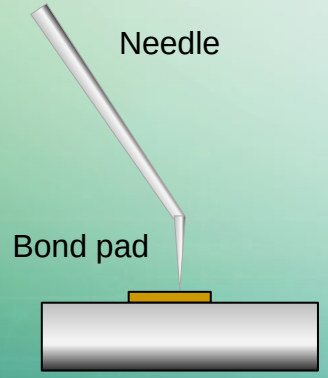
Application

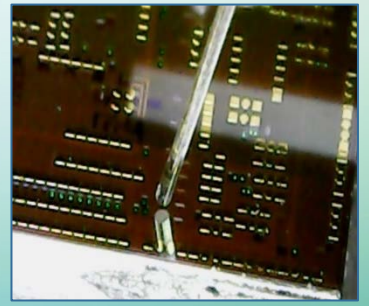
UFO Probe™ – ultra-fast opto-electrical probe card

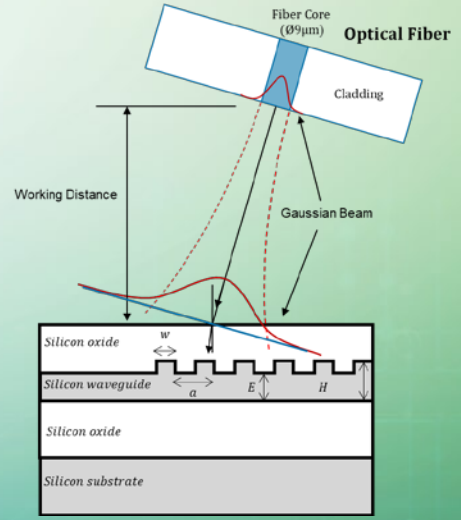
JENOPTIK's solution for high-volume wafer-level test of photonic integrated circuits (PIC).



Combination of electrical and optical probes in one single probe card.



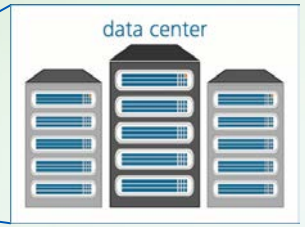




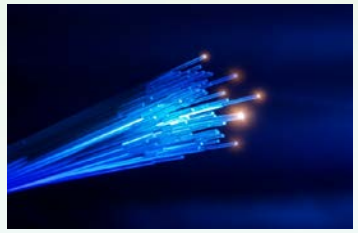
Market View

Optical communication – a major driver of integrated photonics

Connected World

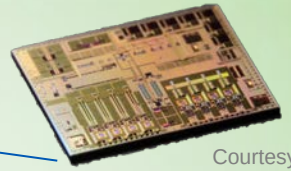


Higher data rates



Optical communication

Signal conversion

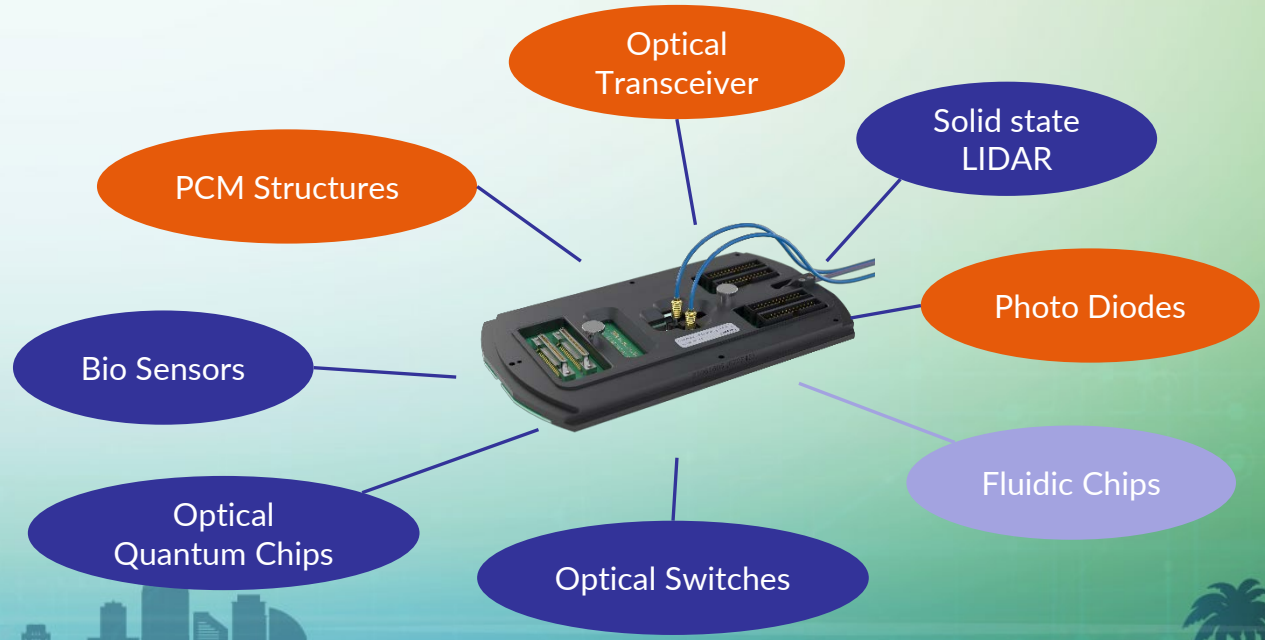


Courtesy of Sicoya

PIC as core component of optical transceivers.

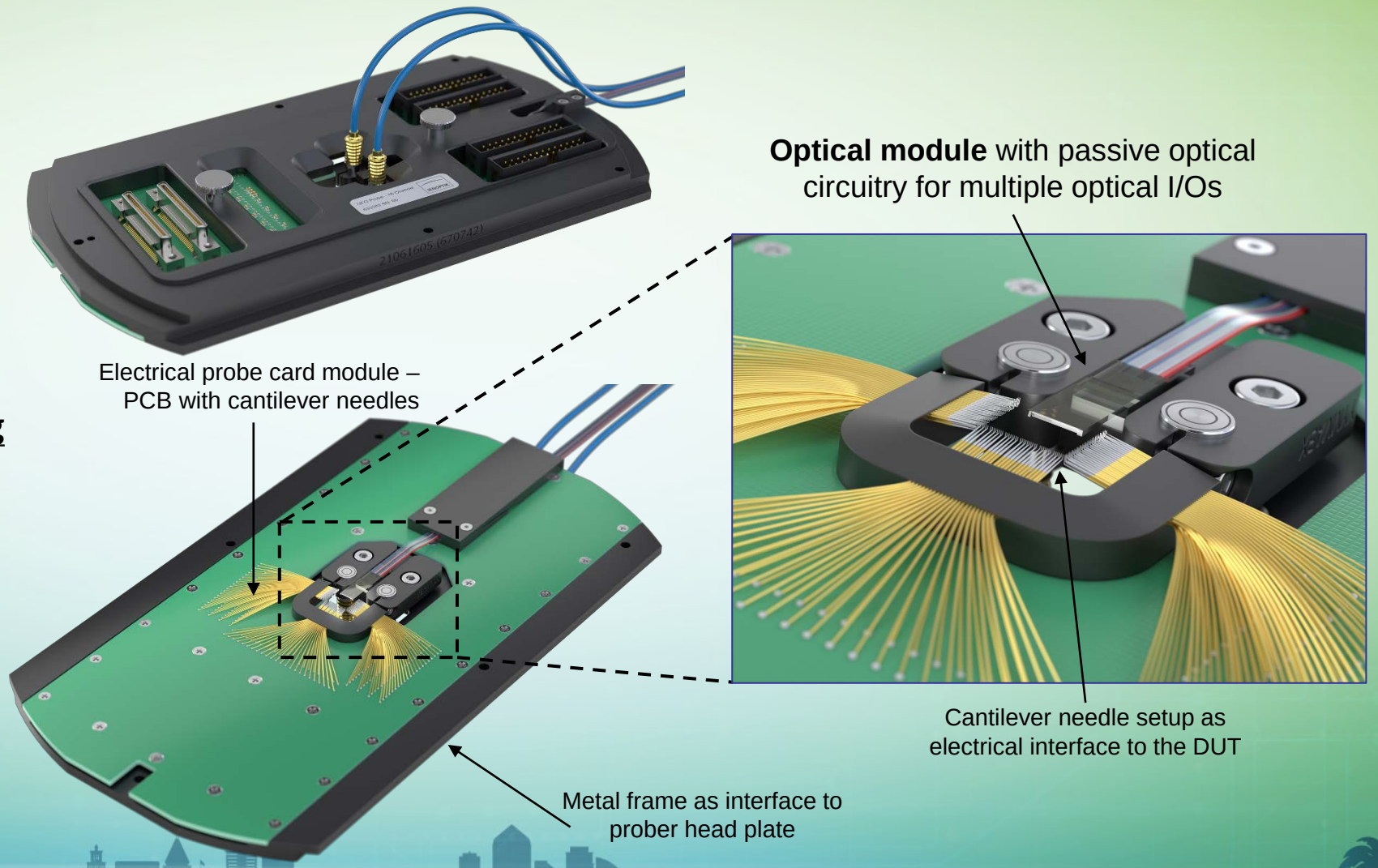
Current PIC test applications in focus

- **Optical transceivers** – ramping up
- Monitoring PIC Manufacturing Process (PCM)
- Photo Diodes



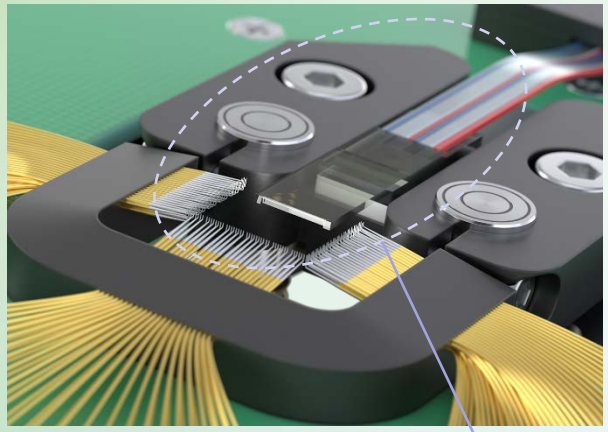
Key Features

- Standard prober interface (Eurocard format)
- **Monolithic optical module with 16 optical I/Os** at a **pitch of 250µm**
- Alignment insensitive optical coupling for **vertical emitting PICs**
- Simultaneous optical and electrical probing
- Utilize **proven needle technology** (partnering with probe card manufacturer)

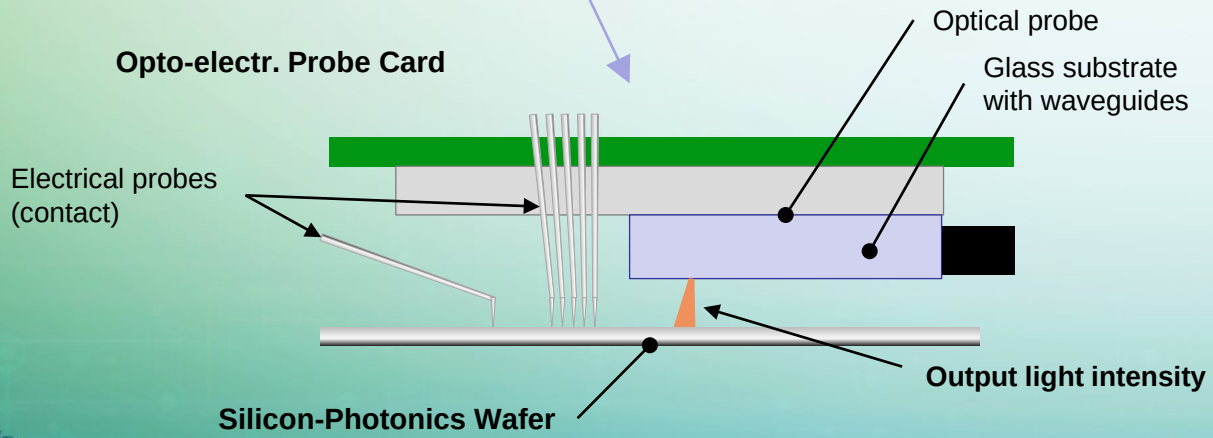


Working Principle

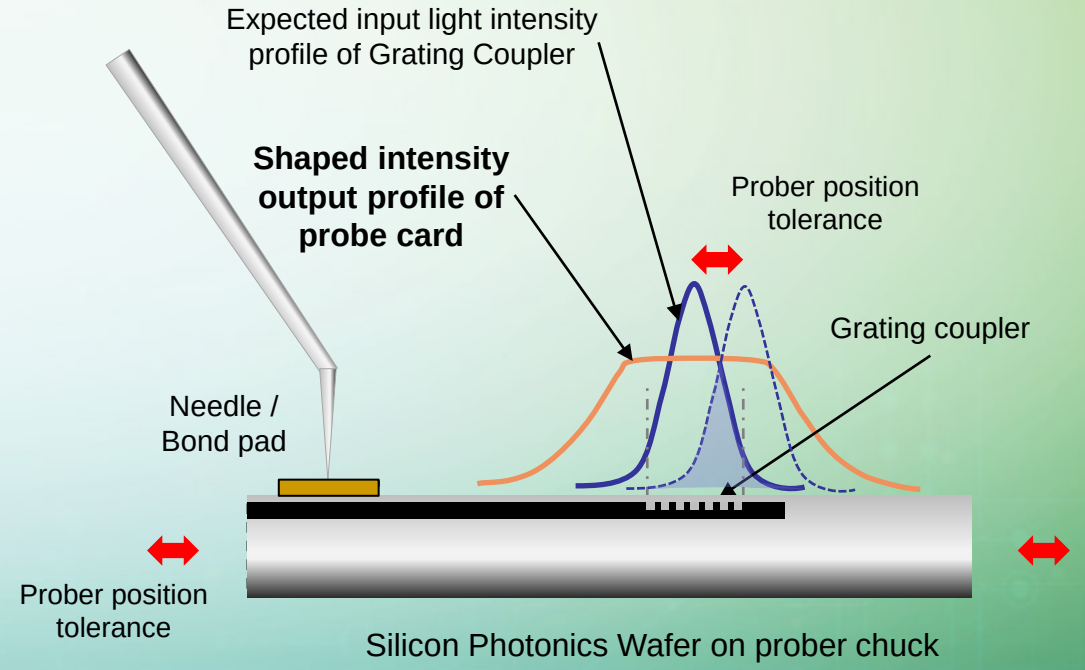
- **How does it work?**



Opto-electr. Probe Card



Optical concept compensates prober alignment tolerances.



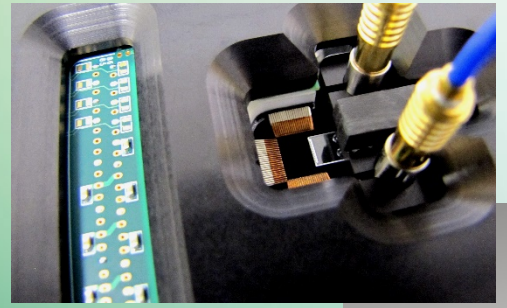
User Benefits

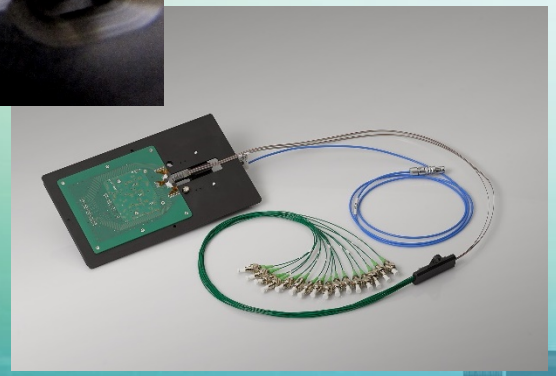
USPs

- **Plug & Play' ready** for existing **standard IC wafer probers** and **automated test equipment**
- **No active alignment** time per chip
- **Parallel qualification** possible → multi-DUT regime
- Operated by same personnel as standard IC equipment

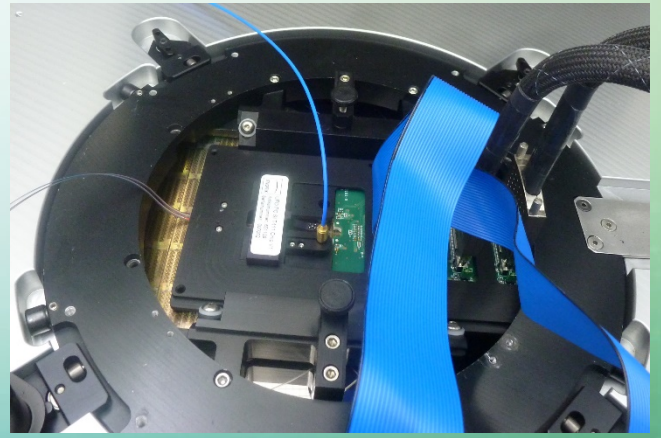
Benefits

- optical and electrical probe integrated in **a single probe card**
- Compatible to existing interfaces
- **Optics** that works **alignment insensitive** and
- Deals with **‚coarse' prober alignment tolerances**
- Scalable solution with simple handling



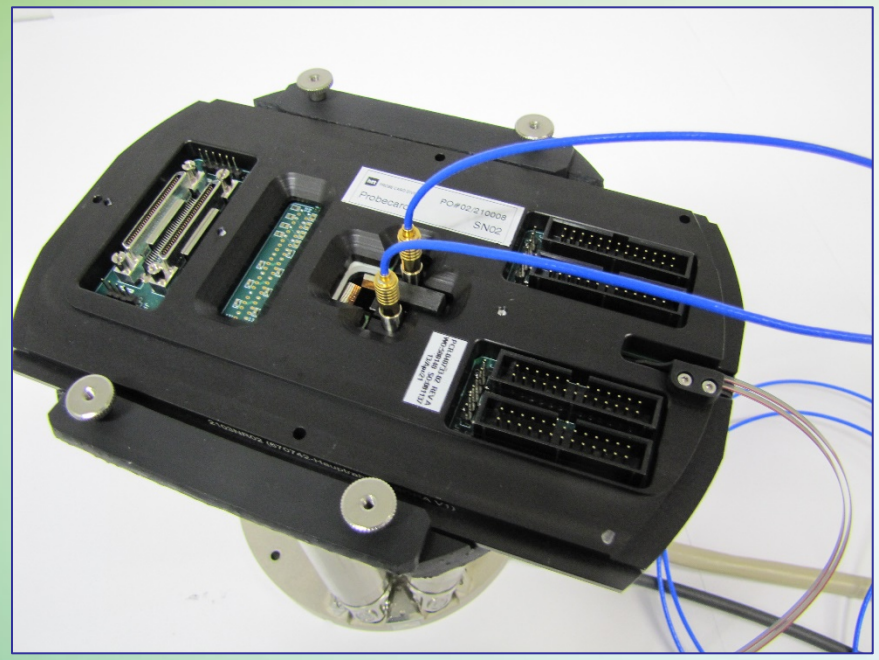


Source: Accretech

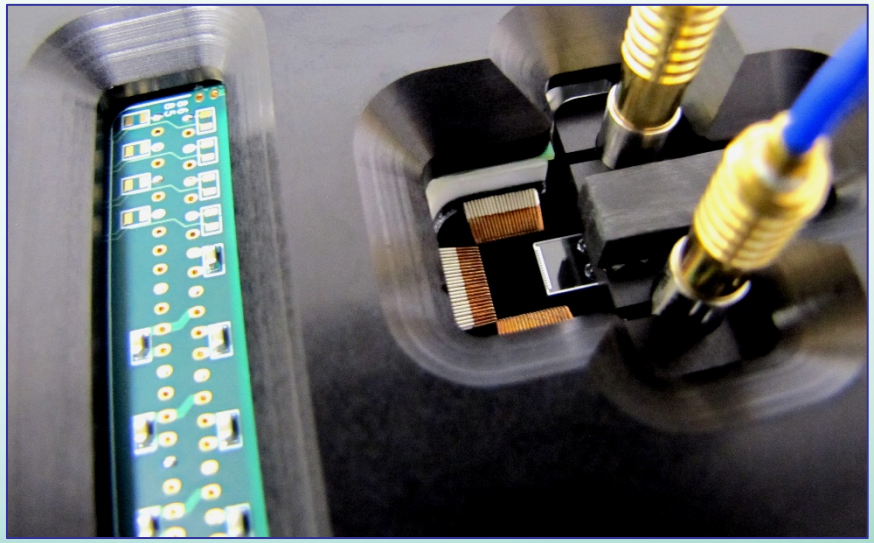


Courtesy of Rood Microtec

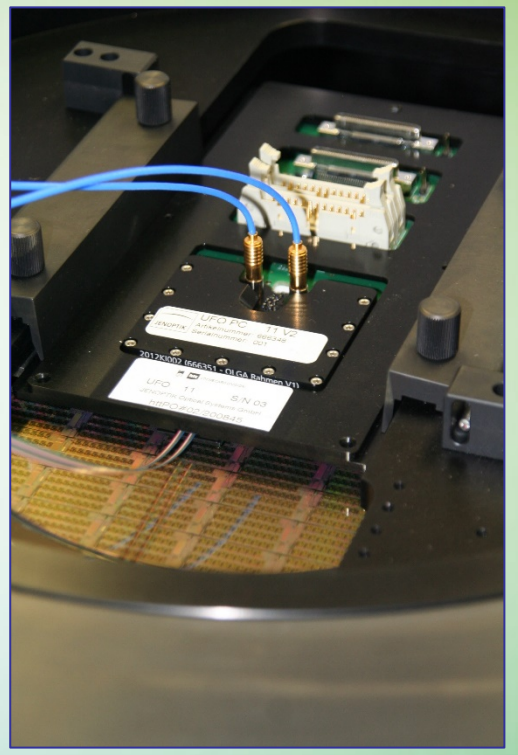
Probe Card Impressions



UFO Probe™ in Europe Card format



Detail of optical and electrical interfaces

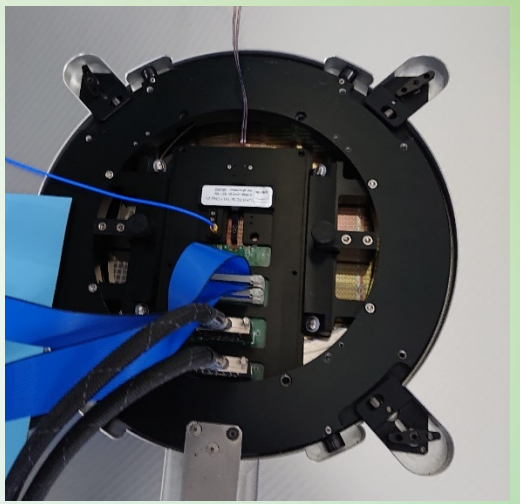


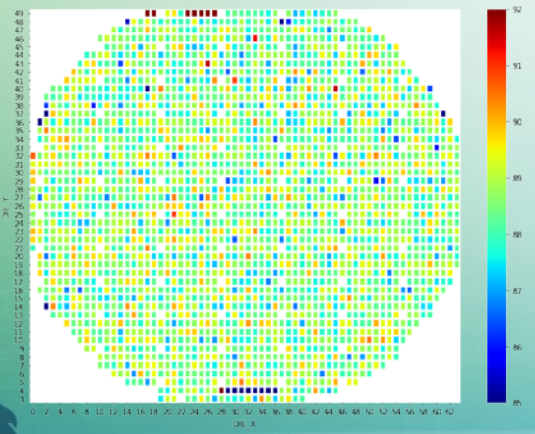
Probe card mounted on a prober

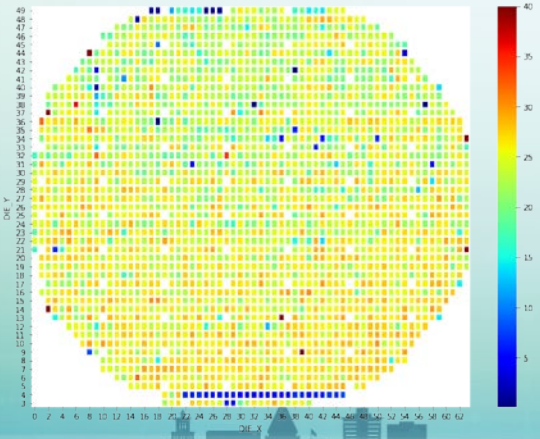
Field Usage

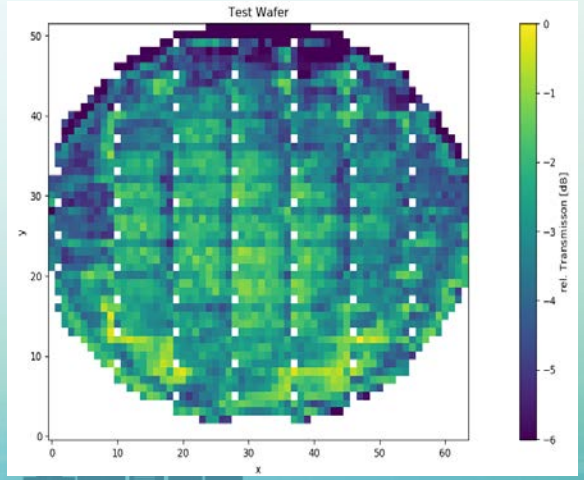
Wafer-level test of transceiver device

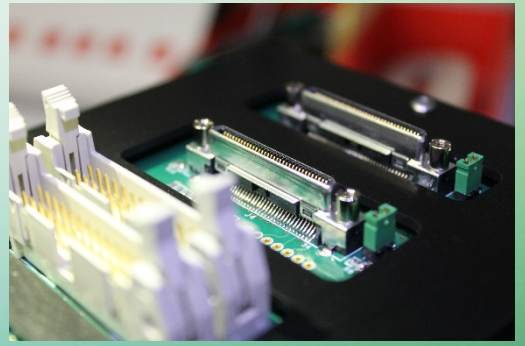
- Running as **final production test in a customer setup**
- RX, TX, alignment channel and comprehensive electrical tests in one **single touch-down**
- **1x alignment per batch**, no additional alignment per chip
- Example of wafer map for Contact Resistance, Receiver supply current and optical alignment channel







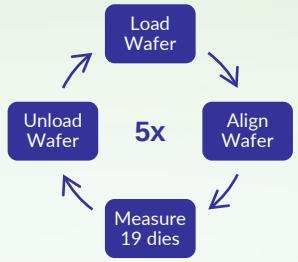




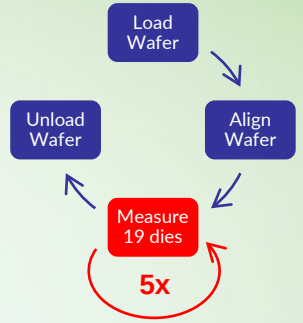
Measurement Capabilities

Verification of test capabilities under realistic conditions:

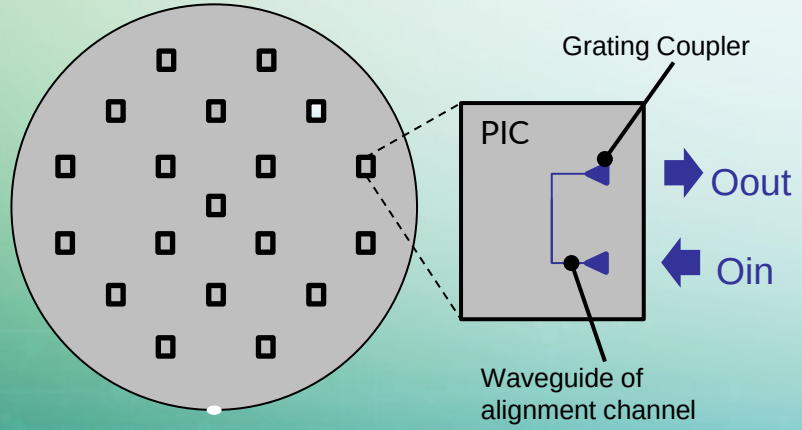
- Measurement of **insertion loss** of an optical alignment channel
- 19 different chips, spread over the complete wafer
- 5 repetitions of each measurement with and without wafer load

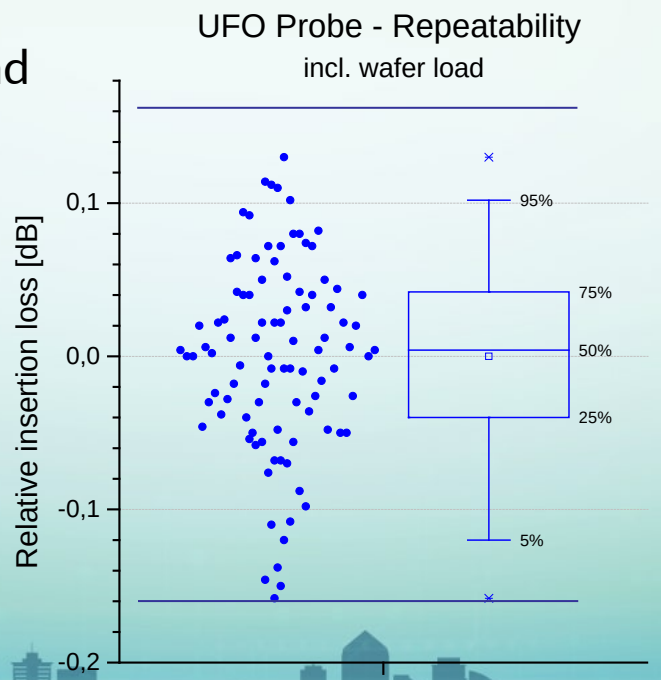


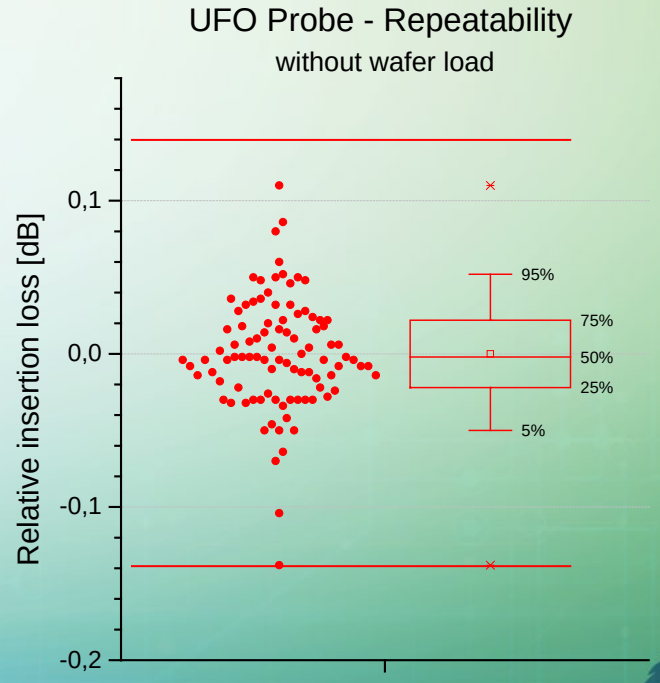
Max. : ± 0.16dB
95/5%: ± 0.12dB



Max. : ± 0.14dB
95/5%: ± 0.06dB



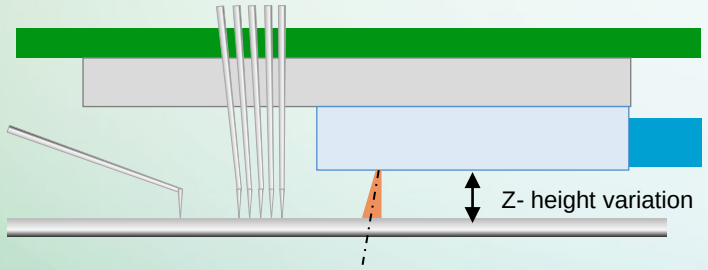


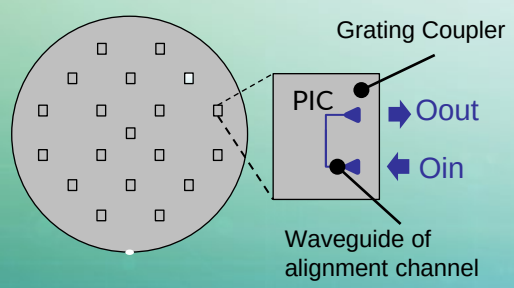


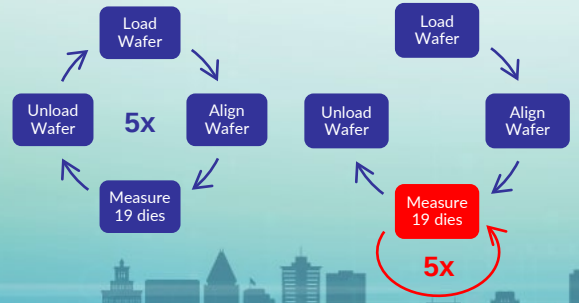
Measurement Capabilities

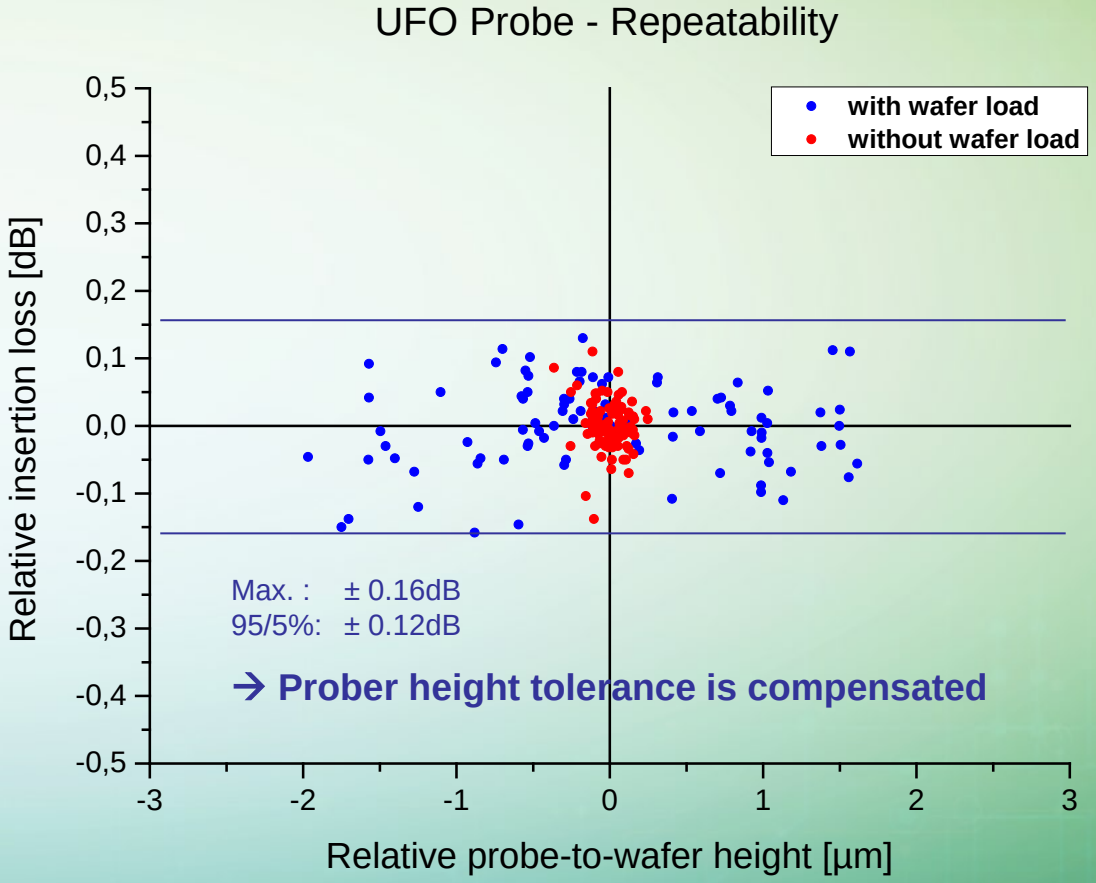
Verification of test capabilities under realistic conditions:

- Measurement of **insertion loss** relative to the **prober-to-wafer height** at optimal coupling angle
- 19 different chips on the wafer in 5 repetitions





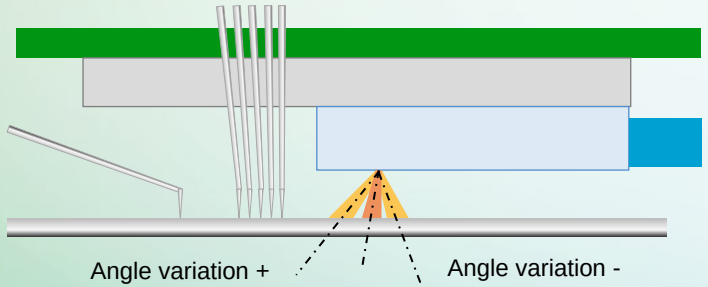


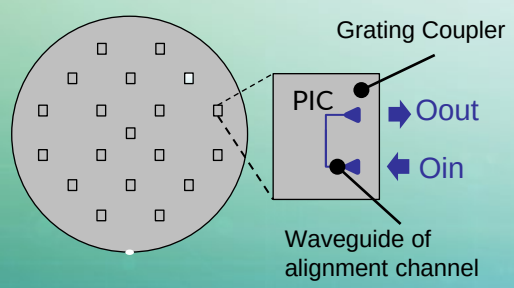


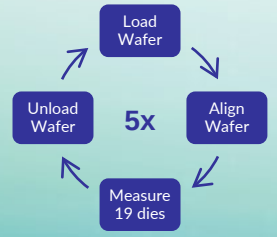
Measurement Capabilities

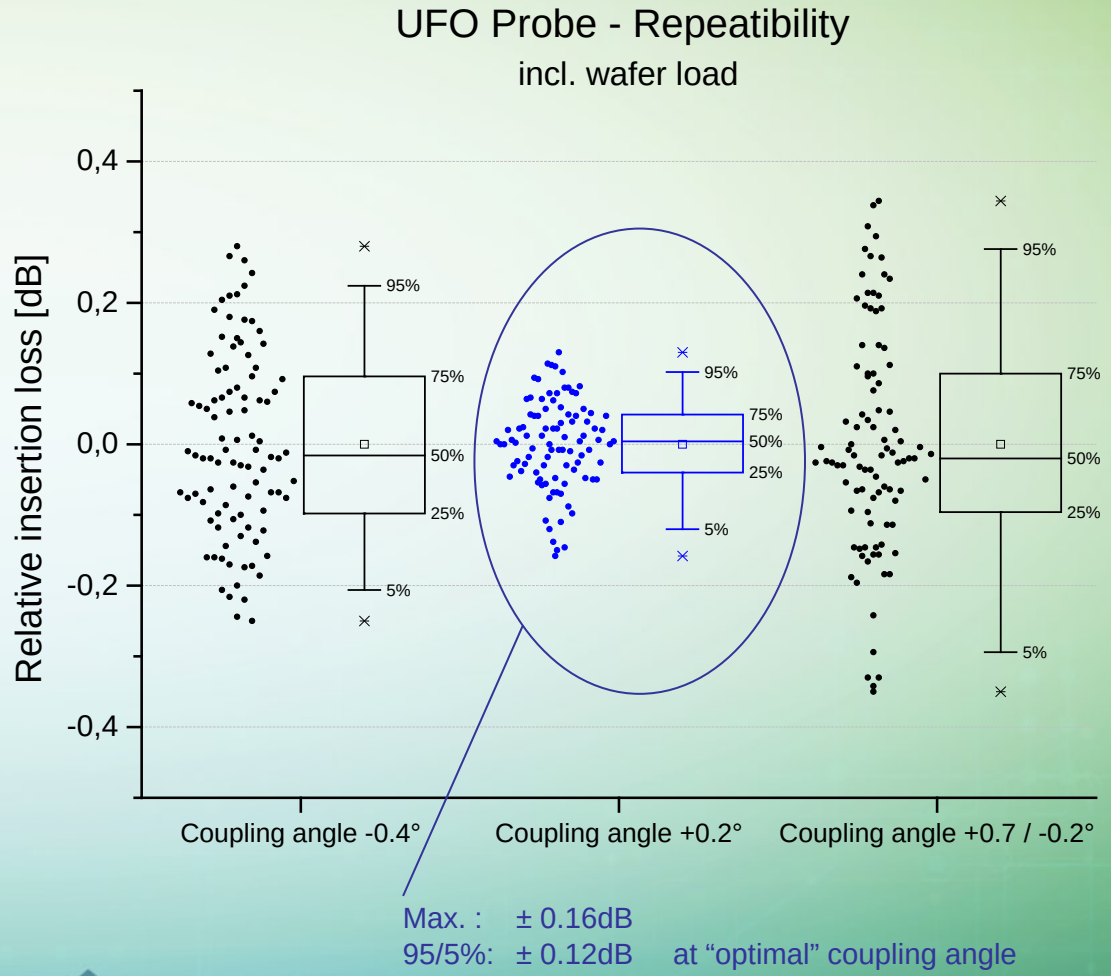
Verification of test capabilities under realistic conditions:

- Measurement of **insertion loss** of an optical alignment channel in dependence of the actual **coupling angle**
- 19 different chips on the wafer in 5 repetitions





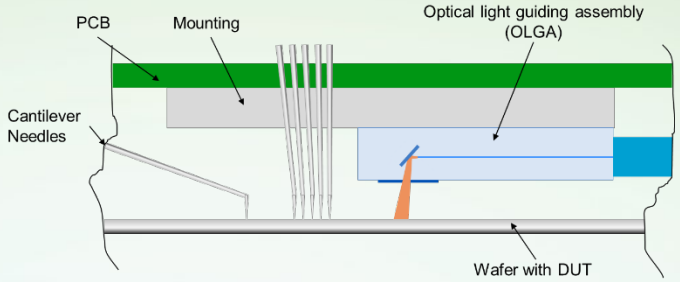


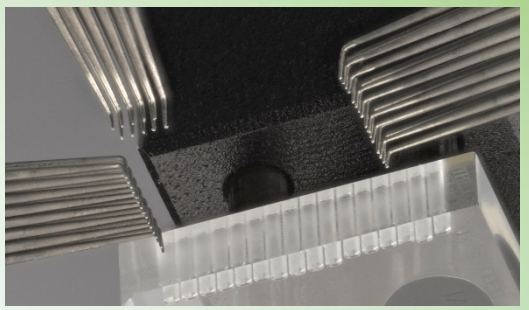


Full Characterization of Optical Module

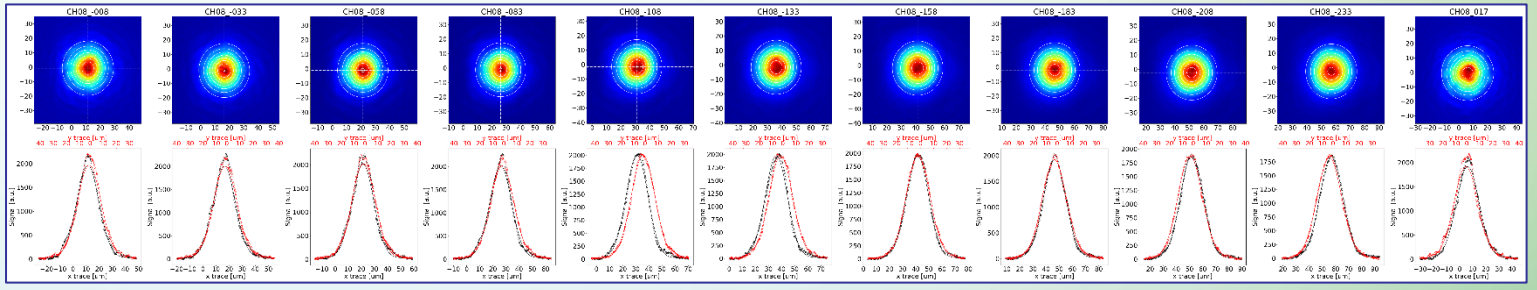
All optical channels

- Beam profile in different Z-heights
- Beam X,Y-position and angle
- Divergence
- Wavelength dependency
- Polarization dependency
- Insertion Loss
- Geometrical dimension



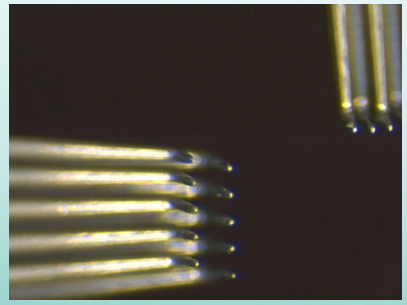


Beam profiles of optical module in Z-scan



Electrical needles

- Position
- Relative position to optical channels
- Tip quality
- Electrical contact



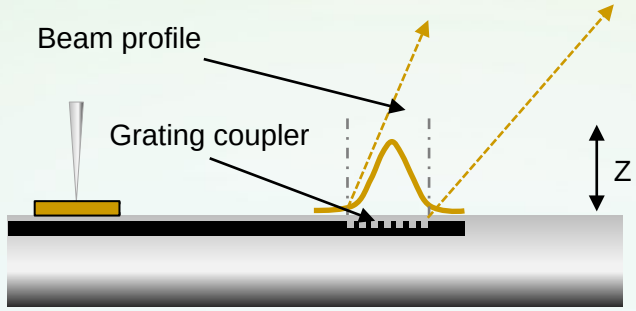
Different needle tip profiles for pad and bump testing

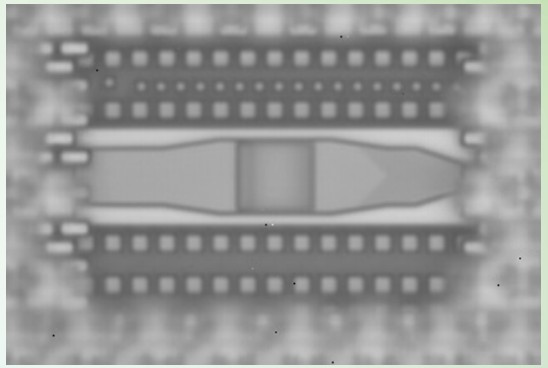
Characterization of PIC Grating Coupler

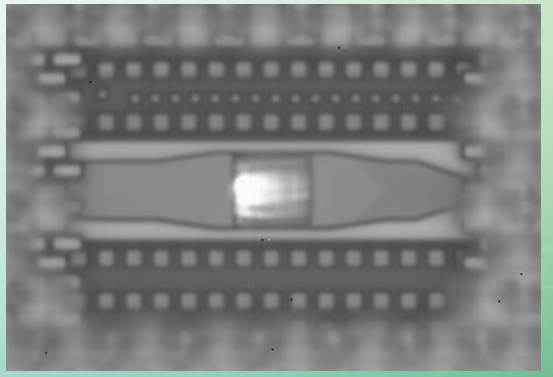
PIC qualification

- Exit beam profile
- Beam X,Y-position and angle
- Divergence
- Wavelength dependency
- Polarization dependency

Beam profile of PIC Exit Channel at grating level







Conclusion and Outlook

- **Introduced an opto-electrical probe card to the market**
- **Verified testing capabilities**
- **Established a first standard configuration (Europe card format, cantilever needles)**
- **Extended measurement capabilities to qualify device-under-test**
- **Next steps:**
  - Implement other needle types
  - Allow electrical RF-testing
  - Utilize automated test equipment
  - Possibility to implement 2D-configuration of optical I/Os

Thank you
for your attention!

Q & A