SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

Extreme Power Probing Challenges of 3000A +more

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Overview

- Introduction
- Motivation
- Power distribution
- Extreme power probing
- Challenges
- Important parameters
- Conclusion

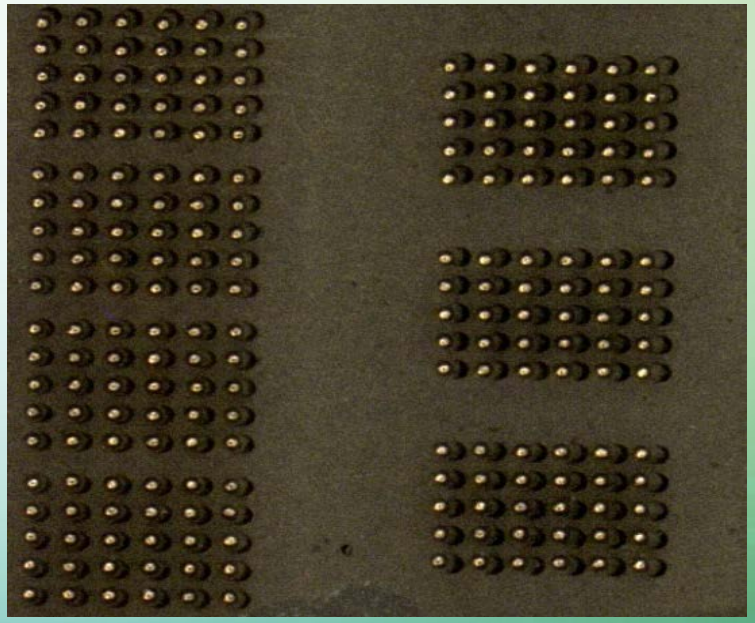
Introduction

Newest test requirements

?

extreme current levels for chip testing

Cantilever technology



Vertical technology

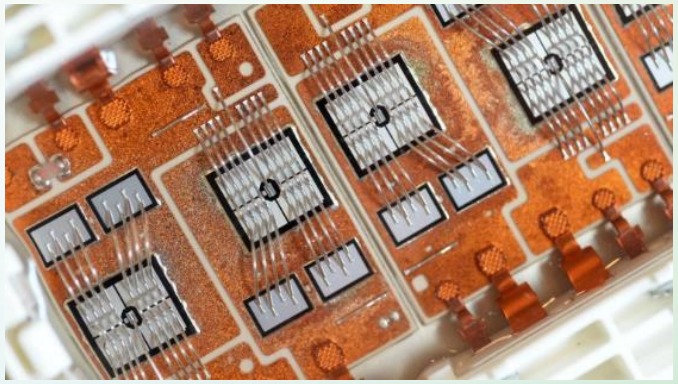
https://www.swtest.org/swtw_library/2021proc/pdf/od_06_salbrechter_swtest_2021.pdf

Motivation

- Device makers, besides selling packaged devices, they sell also bare chips → increased demand for tested bare chips for power devices

Waffle tray with bare chips

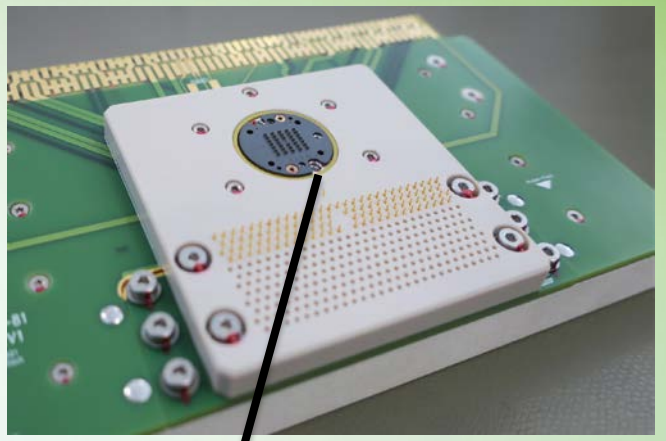
Known Good `Power' Die

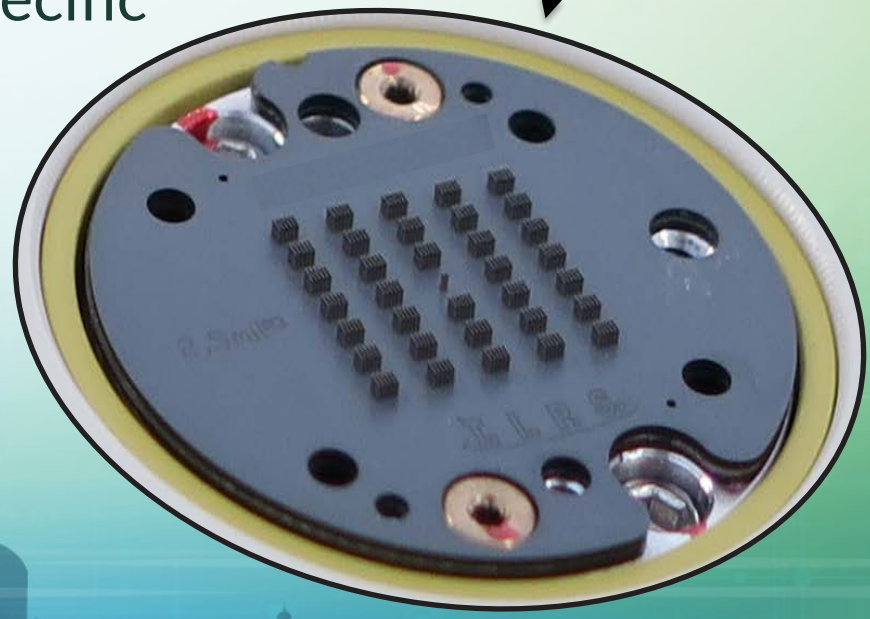


IGBT and Diode chips mounted into a single power module (typically up to 32 chips)

Power distribution to chip – Macro scale

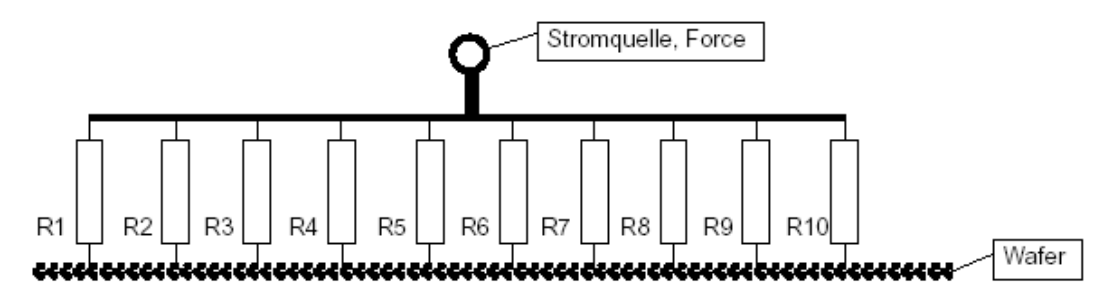
- **Target**
  - Equal distribution of current over chip surface
- **Solution:**
  - 100 balanced current sources
    - SmartClamps, balance resistors, channel specific current limitation via tester (CREA)



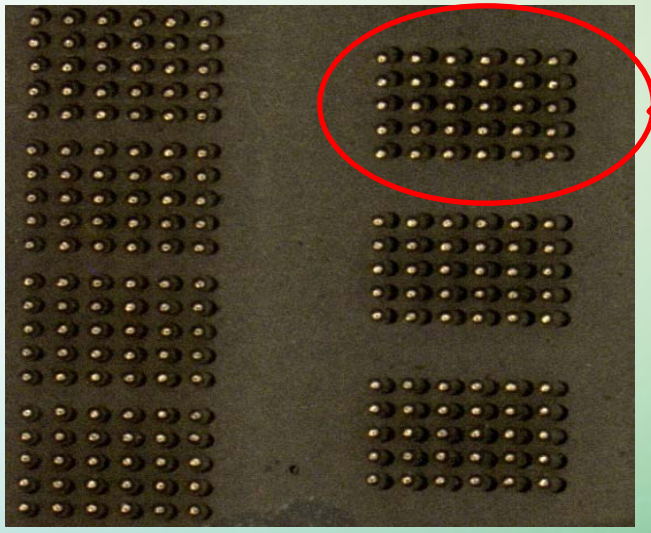


Power distribution to chip - Micro scale

- Each source connected to a bundle of needles carrying up to 30A
- Individual needle resistance
- Cres stability



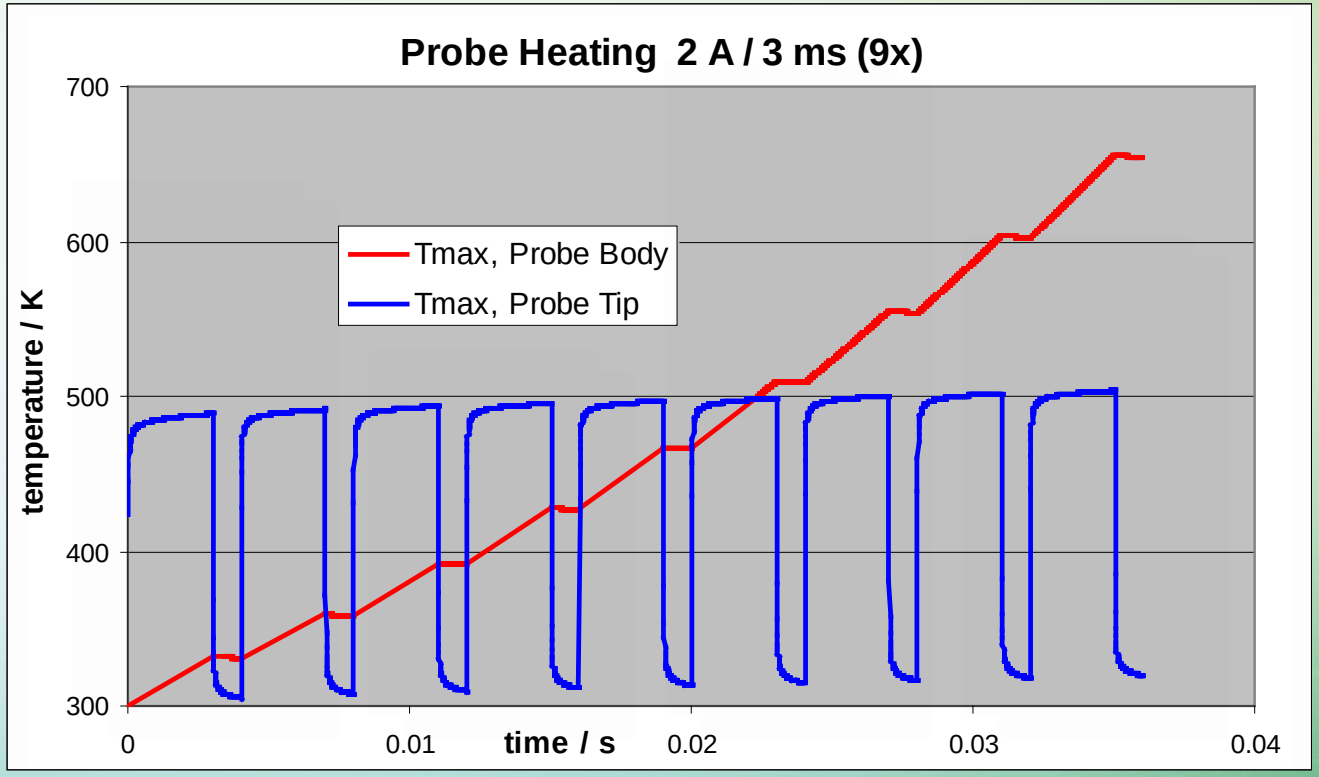
Probes with same resistance value → good CRES



Probe bundles

Power distribution to chip - Micro scale

- **Probecard can withstand given current specs and requirements**
  - Simulation results
  - Experimental verification



https://www.swtest.org/swtw_library/2011proc/PDF/S03_03_Gaggl_SWTW2011.pdf

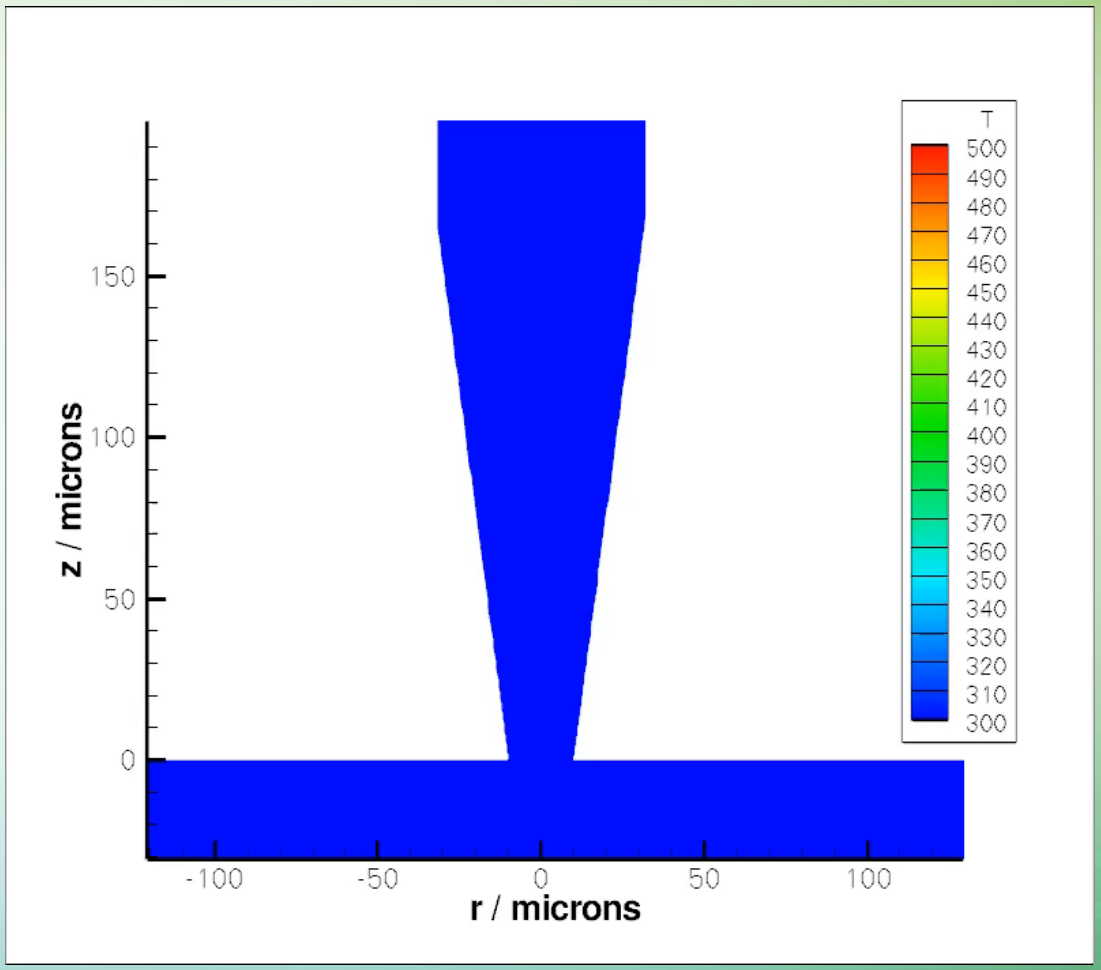
Power distribution to chip - Micro scale

- The heat distribution in a probe for the typical high power application (short high current pulses):

Probe tip heating is the limiting factor!

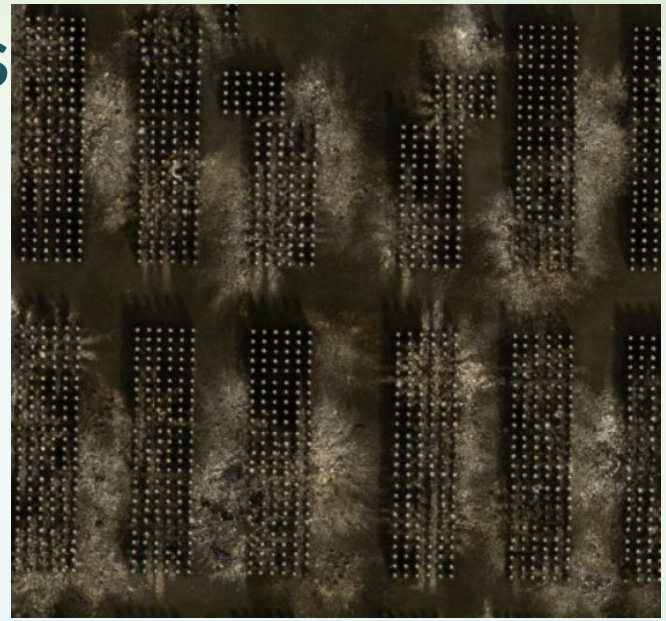
…can be kept within safe limits ☺

BUT what happens if the chip fails?



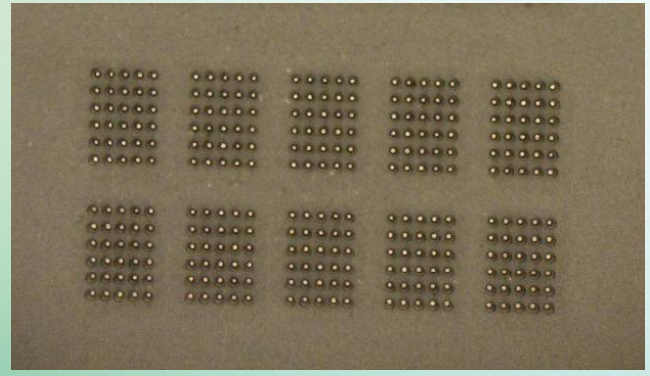
Extreme Power Probing

- Metal splashes on ceramics
- Chip metal fused to probes



Metal splashes on ceramics

"Hot spot" on chip pad



New probe head

...compromise with the lifetime of the probecard!

Challenges

Catastrophic chip failure mode during high power testing

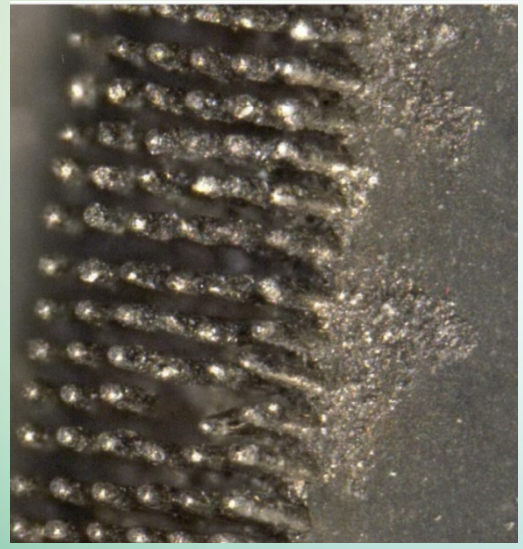
Tester can't fully protect

Hot spot →Melting pad metalization

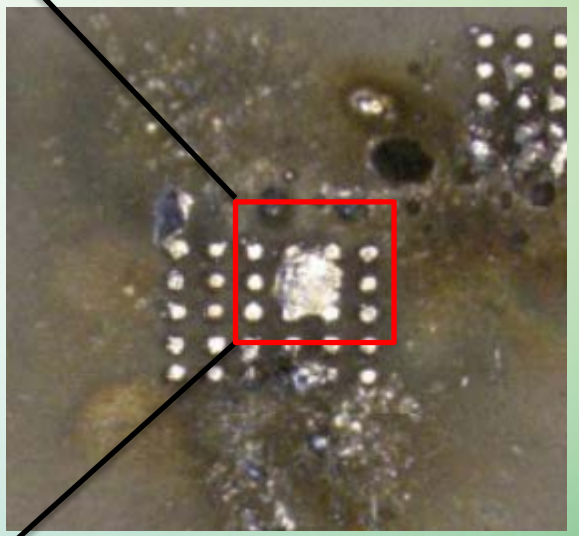
Metal splashes and "nuggets" fused to probes

Extreme Power Probing

- Probe head damages



Needle motion blocked in ceramics guide plate → ceramics fail

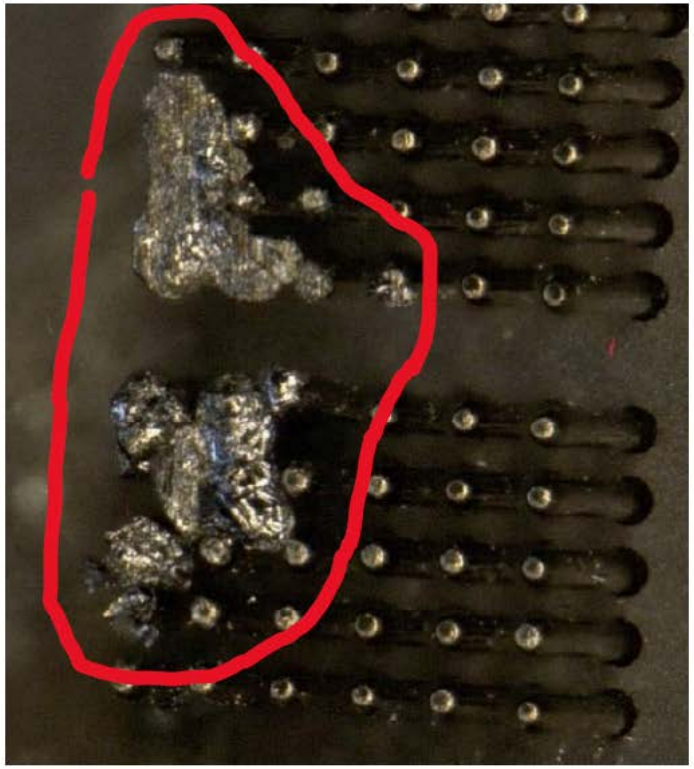


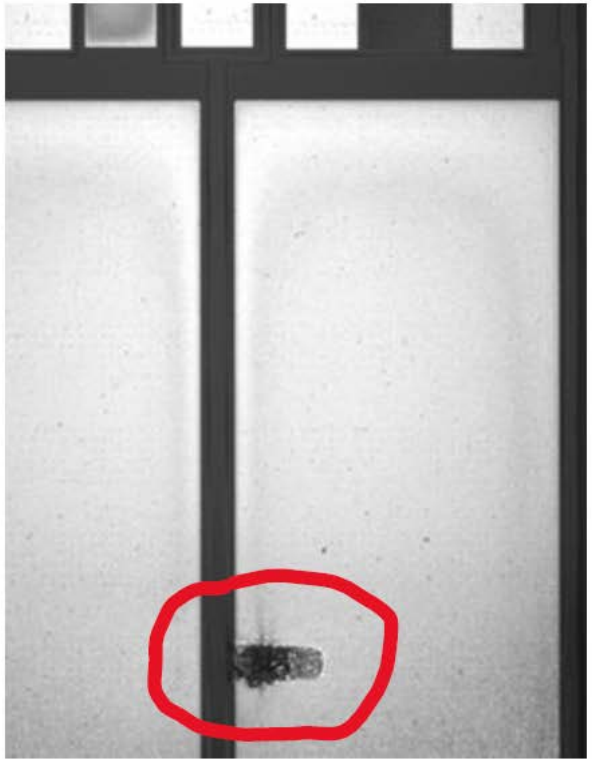
"Nuggets" on probe tip

Extreme Power Probing

- Chip damage

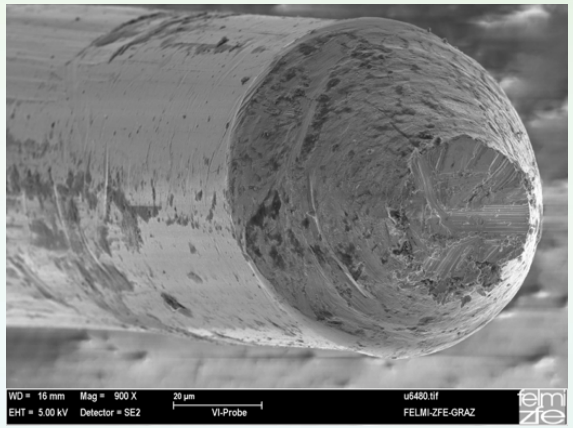
"Hot spot" on chip pad



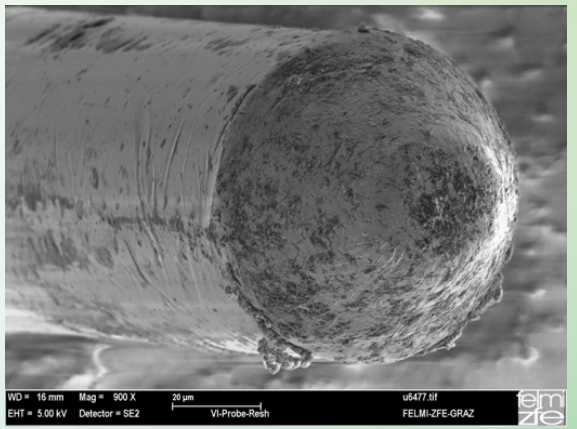


Important Parameters

- Cres stability
- Needle online cleaning
- Overtravel settings
- Current balancing
- Test Temperature
- Energy deposited on chip during test



Used probe



After online cleaning

Conclusion

- **Lessons learned**
  - Despite significant improvements… it looks like metal splashing from chip can't be avoided with current tester technology

- **So…"Let's get to work" … next steps:**
  - „Ruggedized“ vertical probe card technology:
    - Minimize impact of metal splashes to functionality of probecard

Acknowledgement / Q&A

- Thanks to the ‘investigation’ team of T.I.P.S. Messtechnik GmbH
- Questions?