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Copper pad probing with vertical technologies featuring hard metal tip: ARIANNA™ probe family

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Outline

- Introduction
- ARIANNA™ solution
- DOE conditions
- First product tested for DCI
- Oxidation / Corrosion risk given by “bare” Cu
- Protection layer introduction
- Electrical probing at 150°C
- Conclusions
- References & Acknowledgements

Introduction

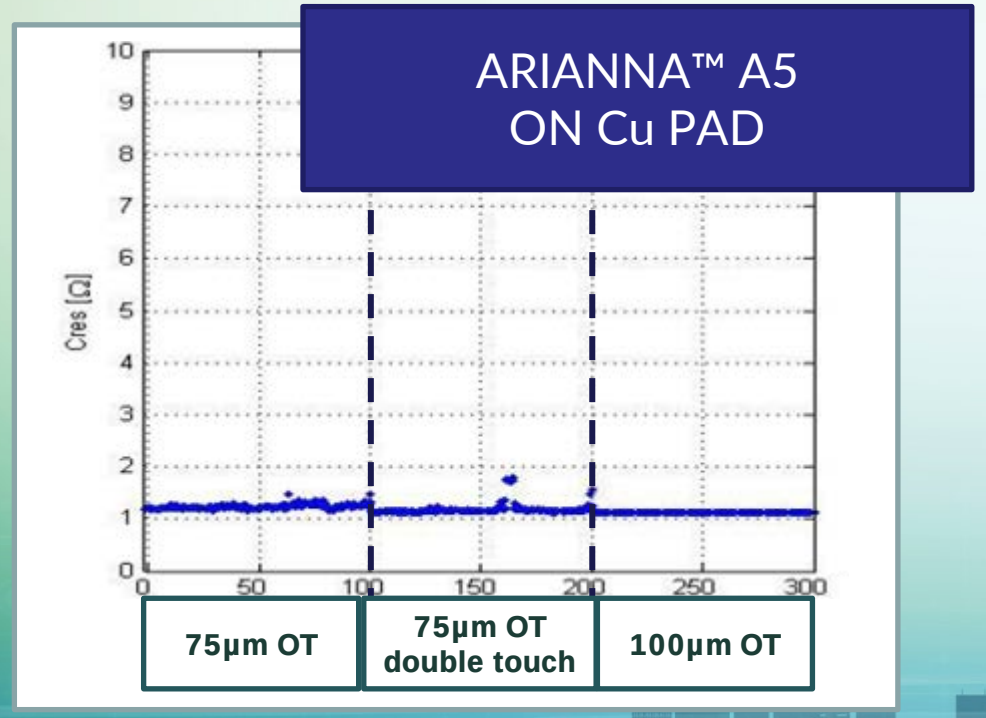
- Cu probing on different structures (pads, pillars, µ-pillars) is gaining momentum driven by processors, high-performance memories and smart power ICs testing requirements, in the evolving 3D packing architectures scenario

- Key ingredients implemented by Technoprobe to successfully probe on different Cu structures are:
  - Customized tip geometry and alloys
  - Scrub control to guarantee contact stability during probing process
  - ... and a joint development path with Customers, allowing Technoprobe to verify and further customize probing solution for unprecedented electrical and mechanical performances

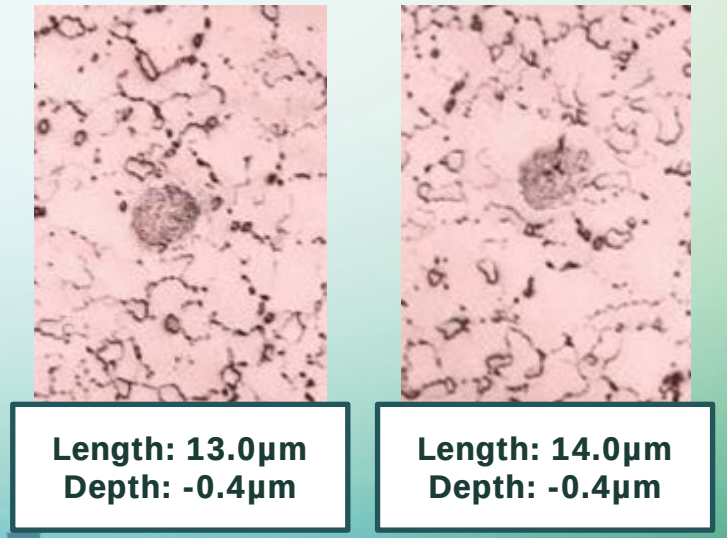
ARIANNA™ solution

- ARIANNA™ technology provides solutions for fine pitch applications (down to 40µm) targeting to minimize contact resistance (Cres) and maintain optimal results also at low/high temperatures (-40°C to +150°C). Below examples of study on customer wafers

  - **CRES data**
    - No cleaning during each test



  - **Probe marks**
    - High magnification OM
    - Single touchdown at 75 um OT



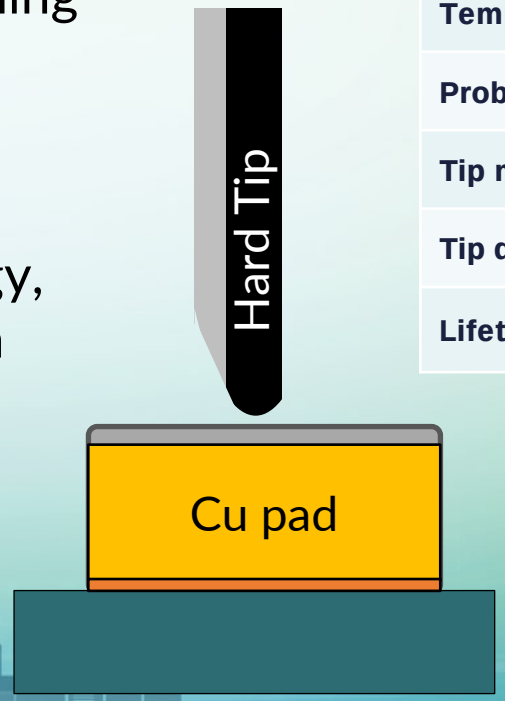
ARIANNA™ solution

ARIANNA™ technology is conceived to ensure best probing performances on Cu PAD finishing, including bare Cu or with ALD (Atomic Layer Deposition) but also other pad metallurgies such as Al or NiPd

- Hard Tip solution
- Scrubbing action optimized based on pad metal finishing
- Minimum pitch down to 40µm full array

Following slides refer to ARIANNA™ A4 HC5 technology, especially developed for STMicroelectronics application

PARAMETER	ARIANNA™ A4 HC5
Needle diameter	2,6 mils equiv.
Min pitch and configuration	78 µm linear 105 µm full array
Pin Current (CCC)	1100 mA
Force (at 75 um OT)	4.5 g
Temperature range	- 45 °C / + 150 °C
Probe alloy	HC5
Tip material	Hard tip
Tip diameter	8 ± 4 µm
Lifetime (typical)	>1M TDs



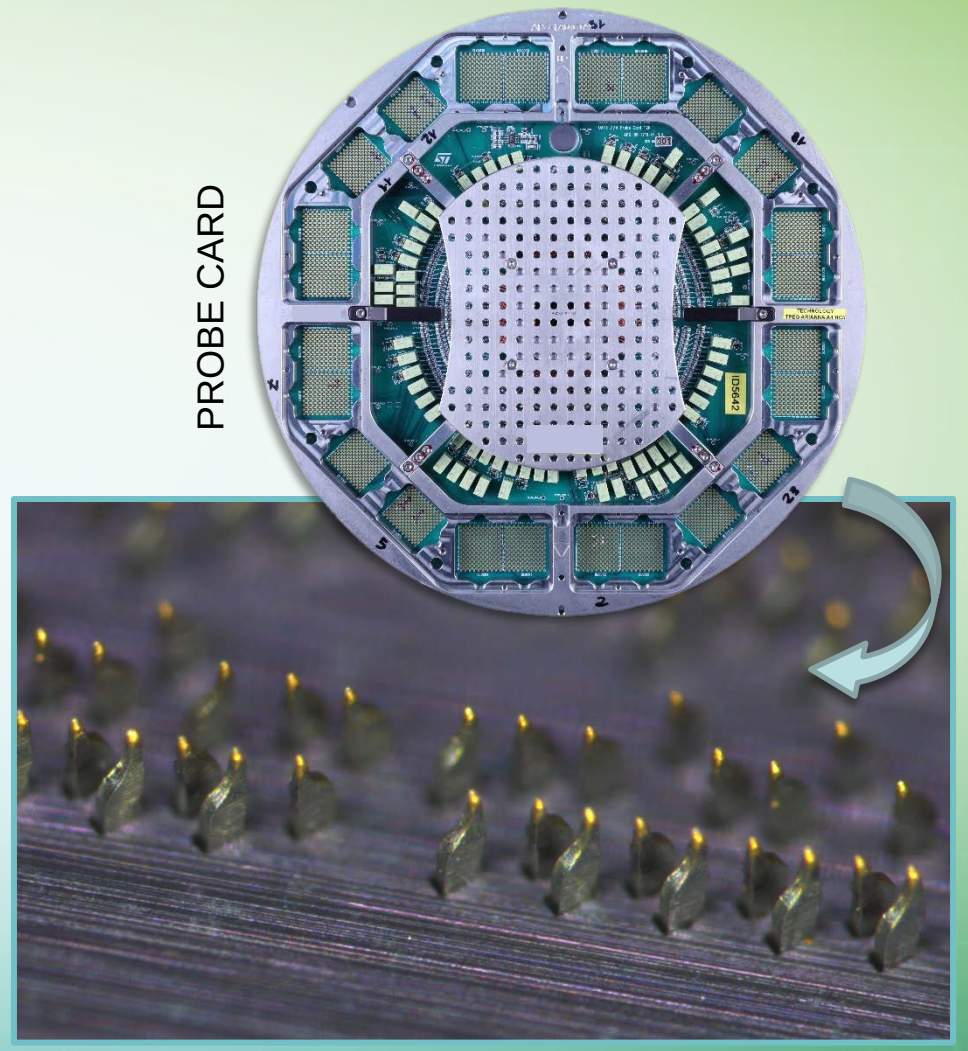
DOE conditions

Experimental set up

TESTER SYSTEM

PROBER

PROBE CARD



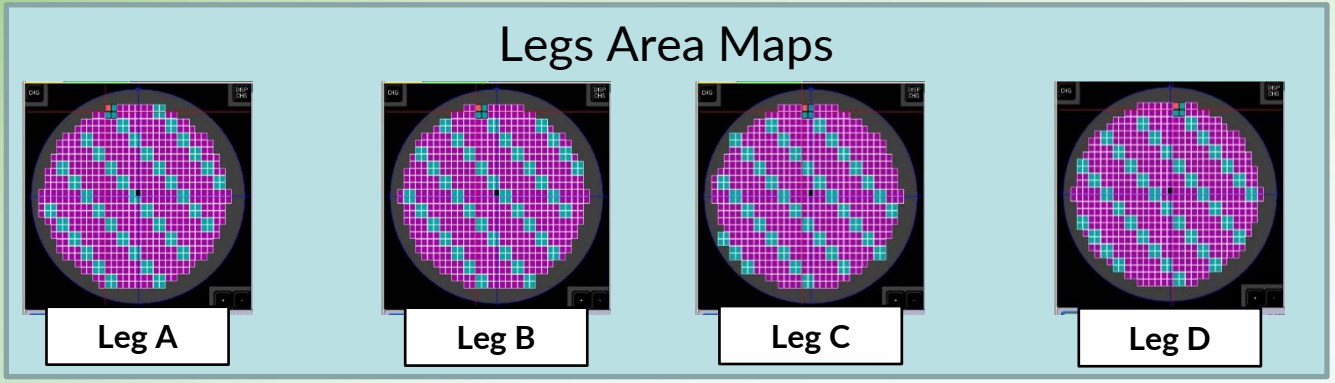
PROBE CARD: ARIANNA™ A4 tech (by Technoprobe)

- Hard Tip solution
- Optimized scrubbing action
- Long Lifetime (>1M TDs)

APPLICATION: STMicroelectronics wafer product

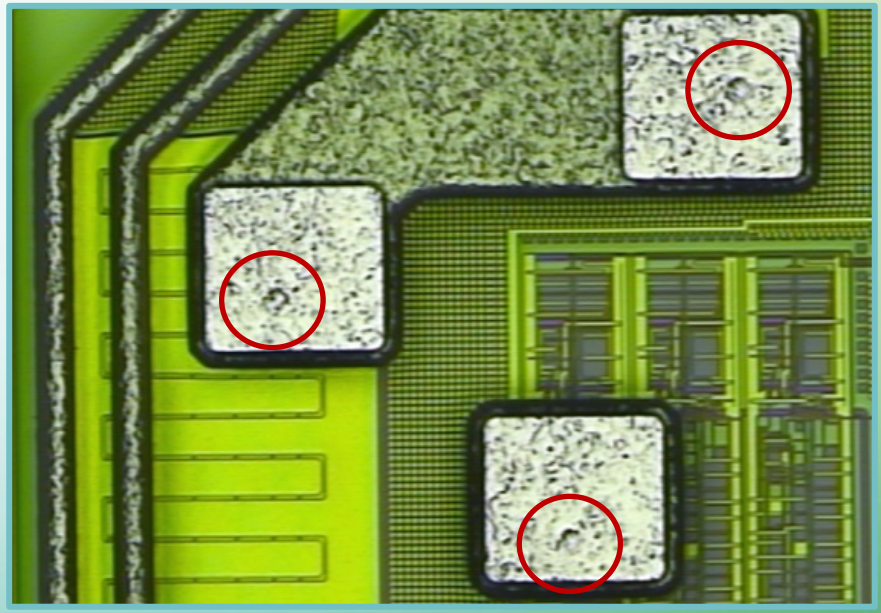
Cu PAD finishing, including bare Cu or Cu with ALD (Atomic Layer Deposition) protection layer

DOE conditions



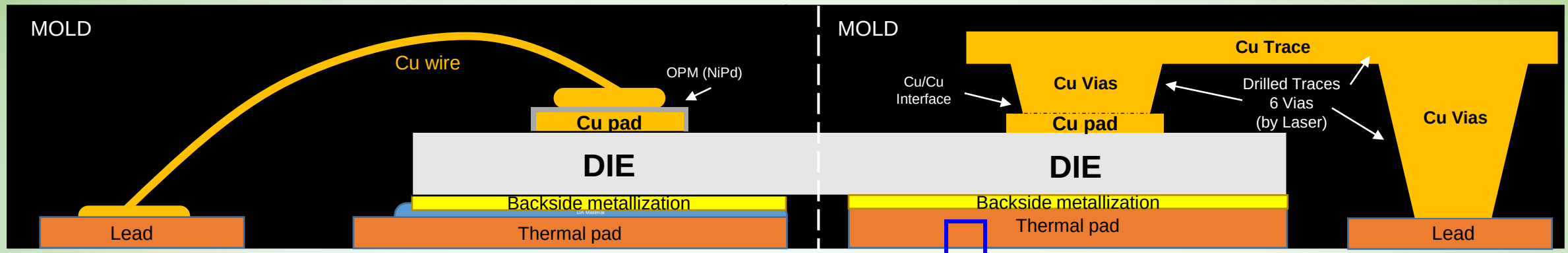
D.o.E. Legs	Leg Area	Leg Temp (C°)	Single/Double touchdown	Aging @150°C (min)
1	A	30	S	0
2	B	30	D	0
3	C	150	S	25
4	D	150	D	50
5	D	150	D	170
6	C	150	S	195
7	B	30	S	195
8	A	30	D	195

- Probing OverDrive (OD): 75µm
- Contact profile: single, double touchdown
- Pad Finishing: Cu (bare)
- Cleaning: before each leg
- Soak Time: 15min + wafer and probe alignment
- Aging: 1 week @30°C before electrical trials



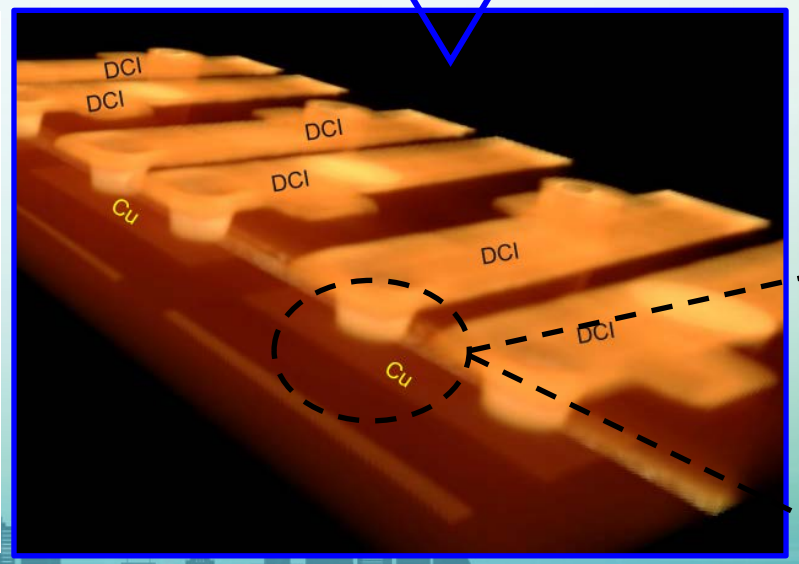
First product tested for DCI

Traditional wire bonding → **Direct Copper Interconnect (DCI)**

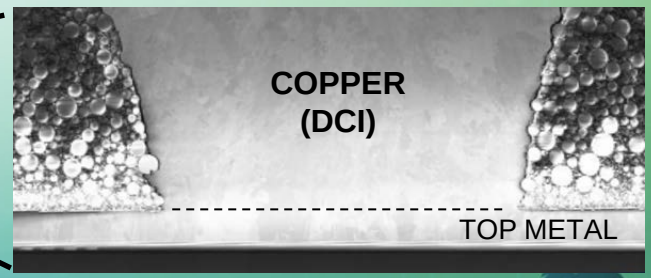


REQUIREMENT:
Cu electroplating step requires an ***accessible Cu*** surface on the last metal

BENEFITS:
- Low resistance & inductance interconnect
- Footprint reduction (miniaturization)
- Low-cost package
- Enabling innovative product design

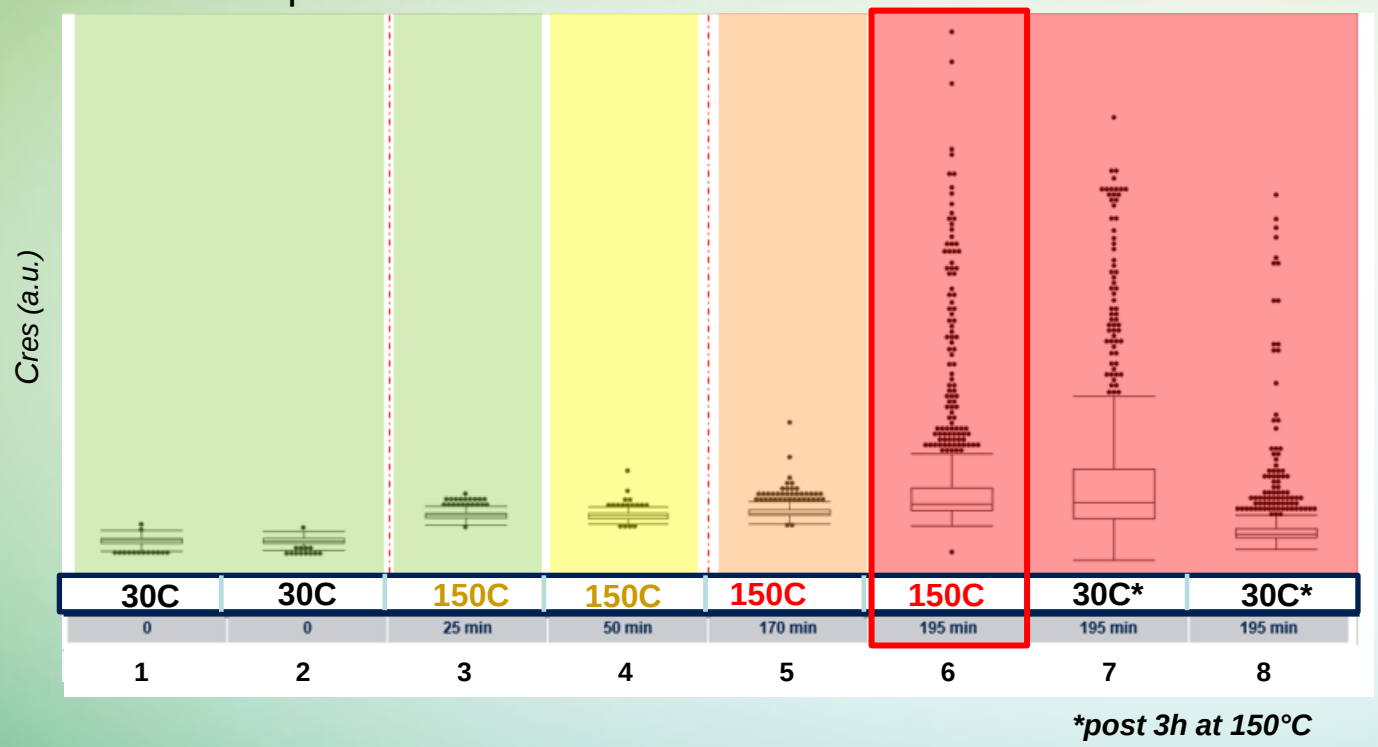


Scanning Acoustic Microscopy (SAM) on real Smart Power product of STMicroelectronics



Oxidation / Corrosion risk given by “bare” Cu

Cres box plot of EWS (Electrical Wafer Sort) probing of bare Cu pad at room temperature and 150°C



Cres is measured at wafer level on real Smart Power product using a STMicroelectronics proprietary technique (no Kelvin test).

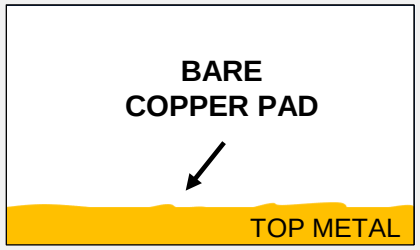
Intrinsic weakness due to unprotected Cu surface:

- **Oxidation / Corrosion**
- **Electrical testability**

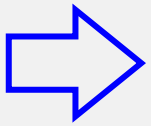
Contact resistance (Cres) degradation due to Cu oxidation after 25min at high temperature

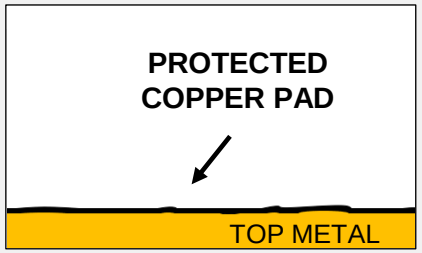
Limitation in production testability

Protection layer introduction



Issues:
- Corrosion Risk
- No Hot EWS probing

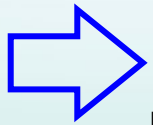




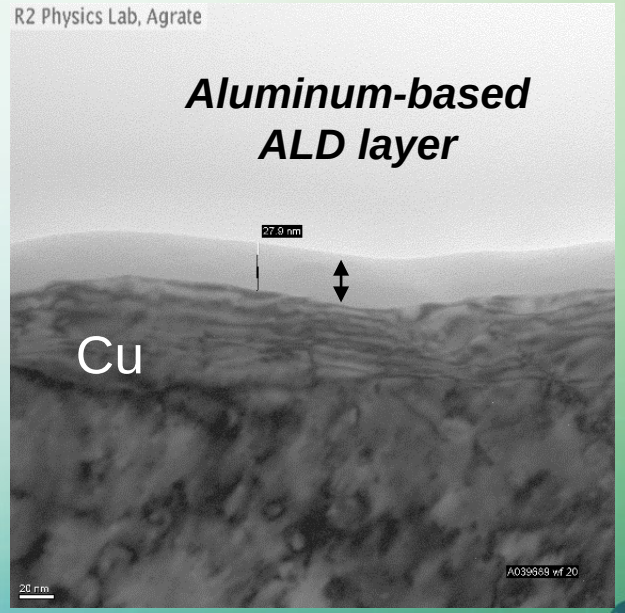
Need a protective layer
- → Thick enough to protect Cu surface
- → Thin enough to guarantee probing
- → Thin enough to be compatible with DCI (laser drilling process)

LAYER REQUIREMENTS:

- ***Good corrosion resistance***
- ***Electrical probing compatibility***
- ***Controlled & Repeatable thickness*** *(nm scale)*
- ***Insulator layer***
- ***Good adhesion*** *to Cu*

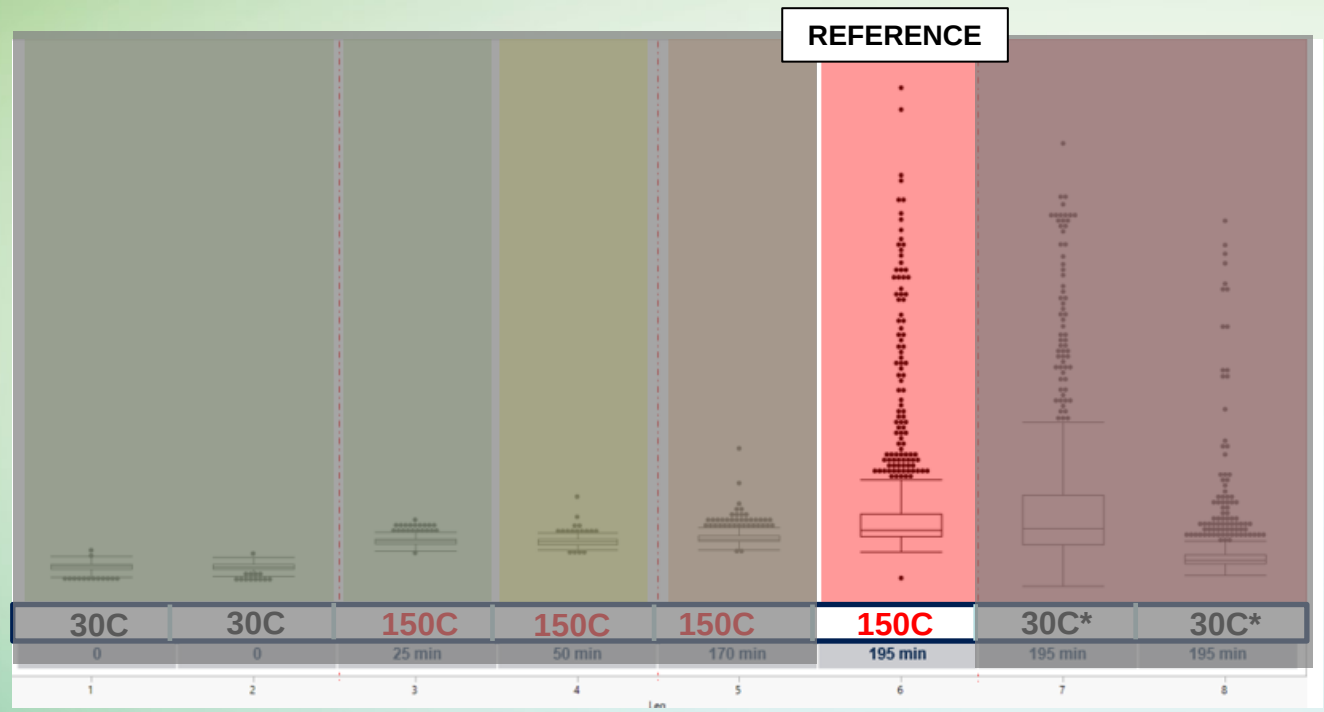


ATOMIC LAYER DEPOSITION (ALD)
Layer: **Aluminum-based**

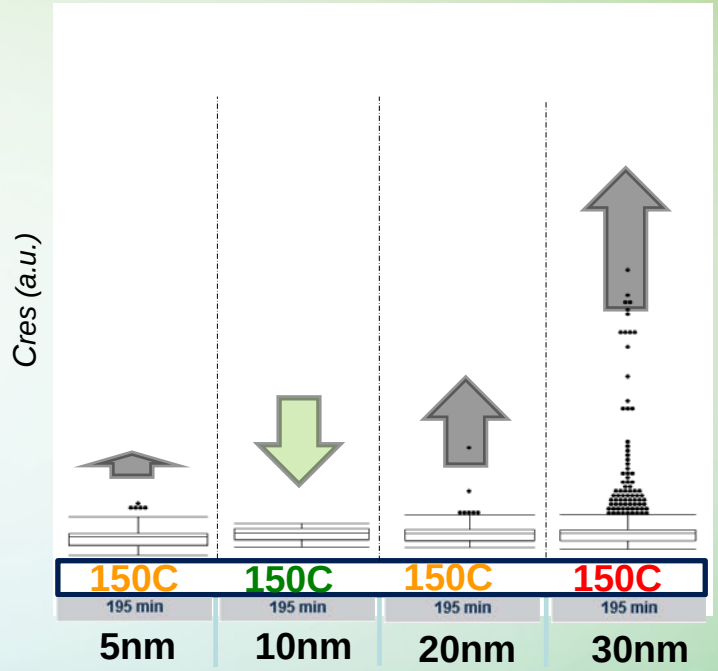


Electrical probing at 150°C

Cres distribution: **Bare Cu**

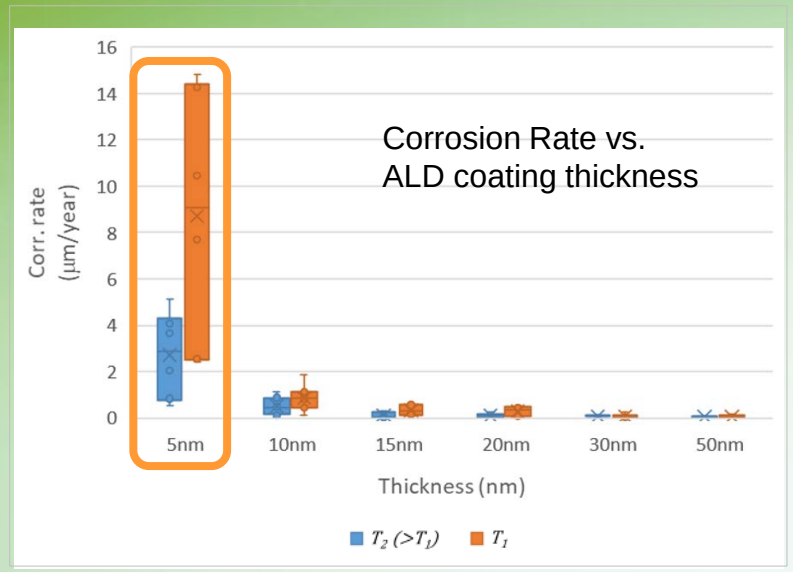


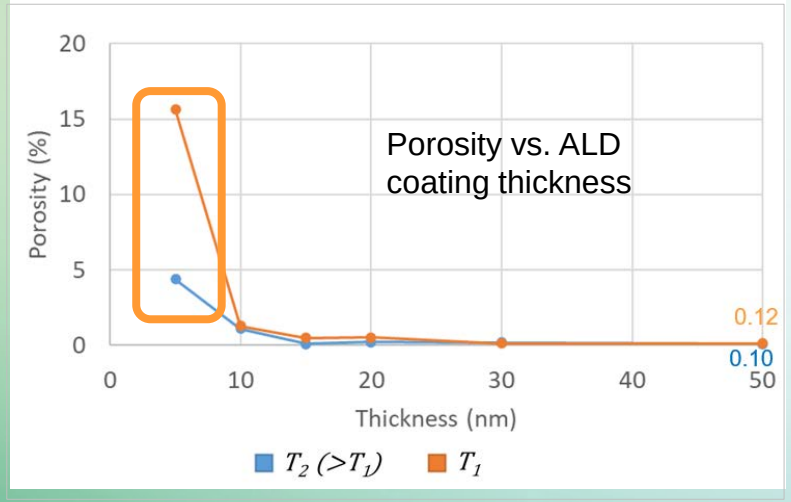
Cres distribution: **Cu coated by ALD**



Overall, ***ALD protection*** show ***evident benefit in Cres*** distribution, ***but a dual behavior*** is evident changing ALD thickness (from 5nm to 30nm)

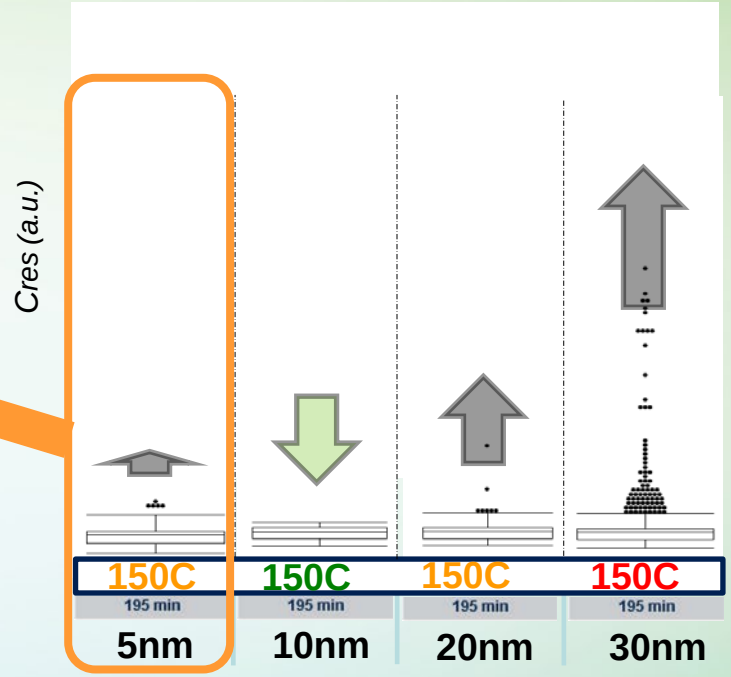
Electrical probing at 150°C





ALD Protection to oxidation not enough during EWS thermal budget

Cres distribution: **Cu coated by ALD**



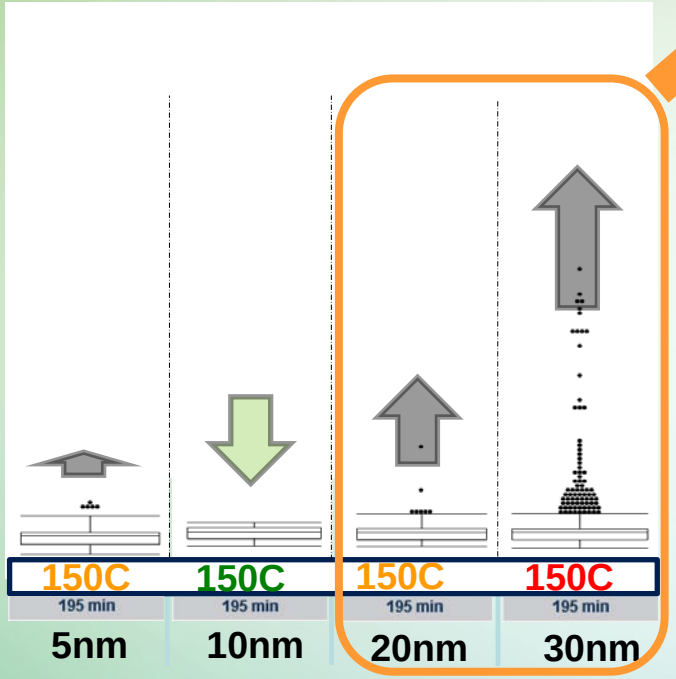
At 5 nm, Cres is affected by ***local oxidized Cu*** due to a not homogeneous coating layer

Significant improvement in terms of corrosion resistance with higher deposition temperature $T_2 > T_1$ ***for thickness ≤ 20nm***

HYPOTHESYS: ***High T deposition*** → better ALD nucleation → ***lower porosity***

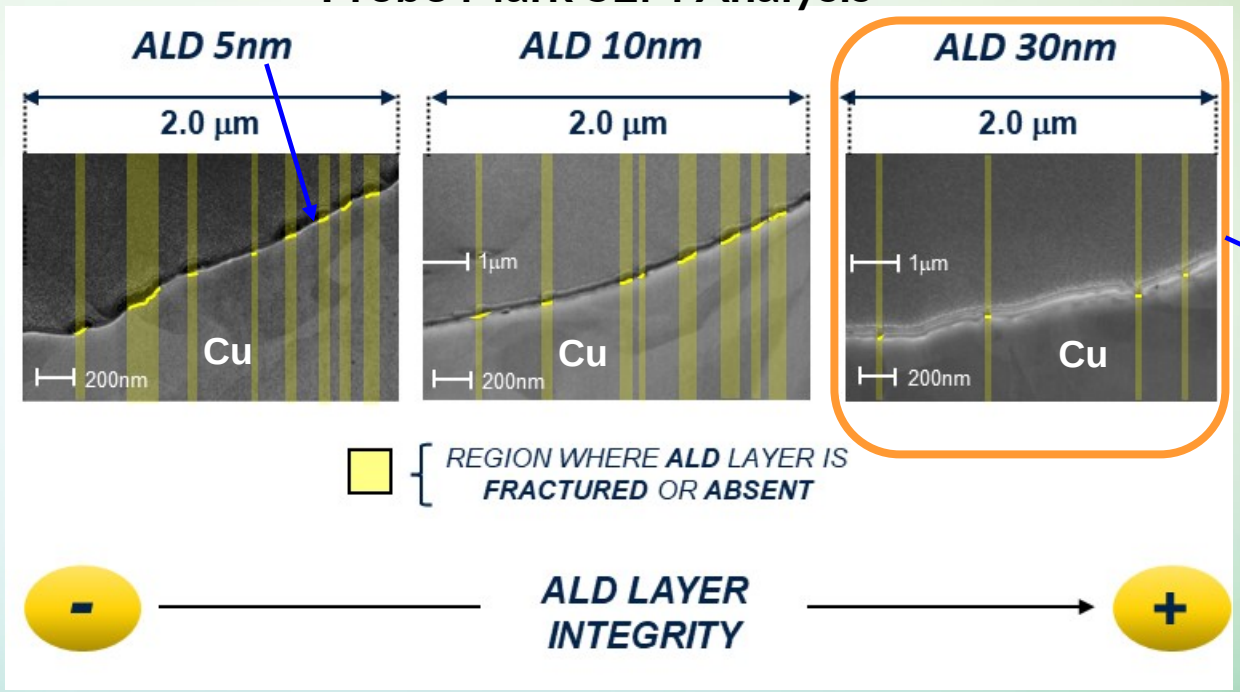
Electrical probing at 150°C

Cres distribution: **Cu coated by ALD**

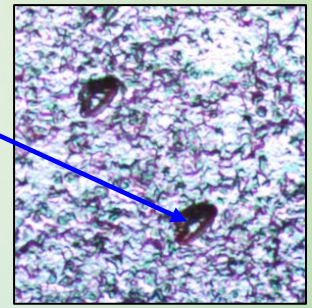


ALD Layer not fractured enough

Probe Mark SEM Analysis



PROBING MARKS AREA



HYPOTHESYS (for 20-30nm): Cres affected *by* ***absence of effective channels for the electrical conduction***
→ the higher the thickness, the lower the Cu depression, the lower the ALD fracturing, the lower the α-spot number (see Ragnar Holm book)

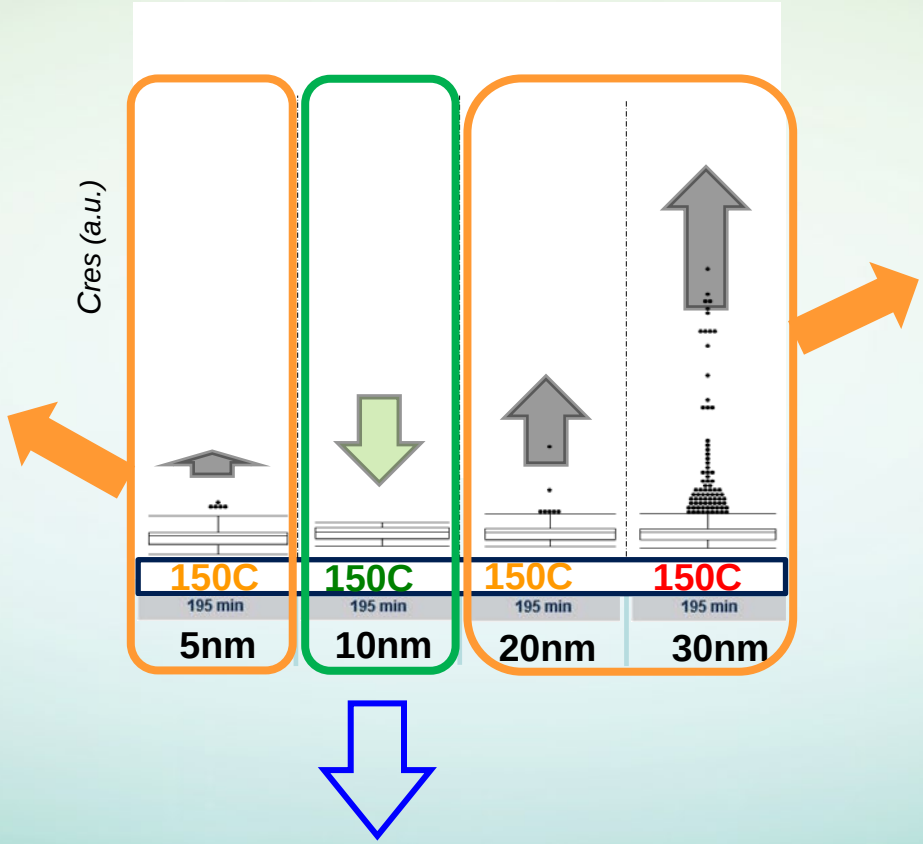
Electrical probing at 150°C

Cres distribution: **Cu coated by ALD**

HYPOTHESYS (for 5nm):

Cres affected by ***local oxidized Cu*** due to a not homogeneous coating layer

→ Few PADs are affected by oxidation



HYPOTHESYS (for 20-30nm):

Cres affected *by* ***absence of effective channel for the electrical conduction***

→ the higher the thickness, the lower the Cu depression, the lower the ALD fractures

10nm is an optimal working condition, with a very good electrical performance

(No damage of structure under pad in worst probing conditions after delayering analysis)

Conclusions

- **DCI based package options require new solutions in term of metal pad finishing**
  - Bare copper PADs show some intrinsic limitations, such as high corrosion risk and incompatibility with high T electrical testing

- **ALD layers offer a robust copper surface protection to oxidation**

- **Electrical testability at high T (by innovative ARIANNA™ A4 probing technology by Technoprobe) shows a promising working point for ALD 10nm**

Acnowledgements

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- *Raffaele Vallauri*

References

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[2] Hsiang-Yao Hsiao, IEEE 22nd Electronics Packaging Technology Conference, 978-1-7281-8911-6/20 (2020)

[3] Fuhan Liu, Chandrasekharan Nair, IEEE Transitions on Components, Packaging and Manufacturing Technology, Vol. 8, No. 5, (2018)

[4] Samuele Sciarrillo, MAM2022 conference

[5] Ragnar Holm, Electric Contacts: Theory and Applications, Springer

Q&A