SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

An Advanced Method for Pad Stack Crack Assessment during Probe-Over-Active-Area

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Test for Infineon Segments

Connected Secure Systems

Automotive

Power & Sensor Systems

Industrial Power Control

BE

BL

FE

Wafer Test

POAA

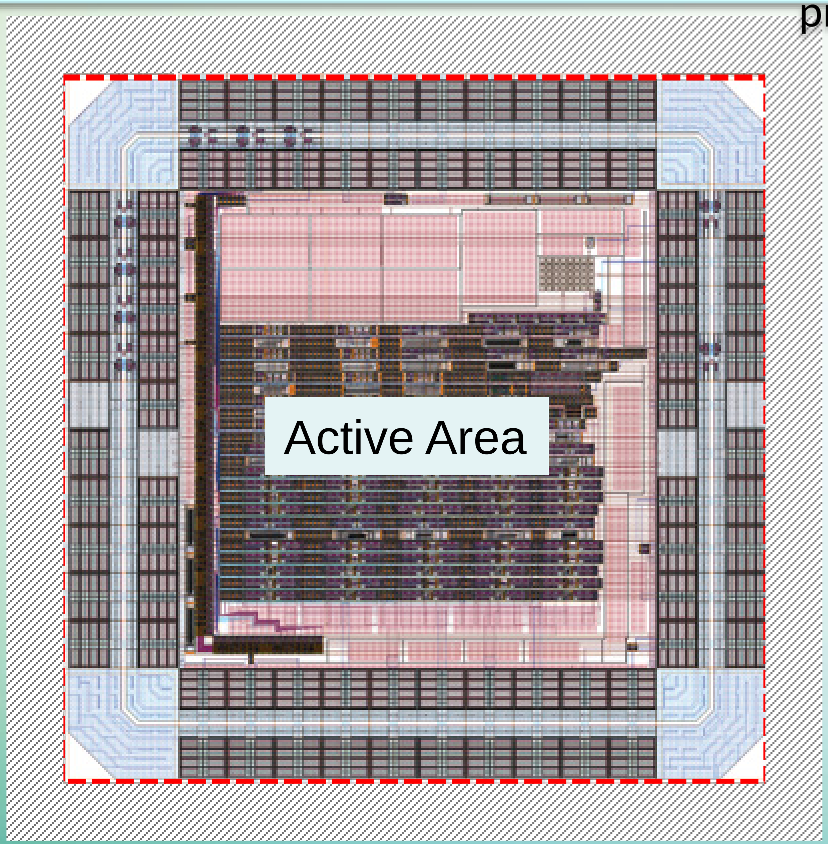
QM

OP

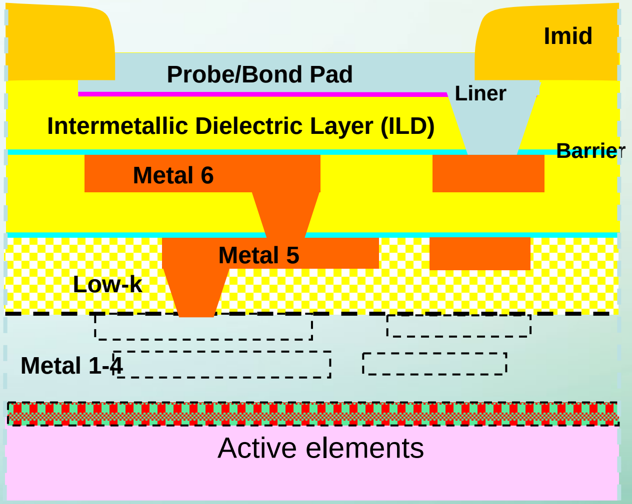
Supplier

POAA Concept for CMOS Technology

In most advanced CMOS technologies, in order to optimize the area consumption,
Probe Over Active Area (POAA) structures have been introduced.
Active circuitry is therefore designed below the probing area with potential stress-induced problems.

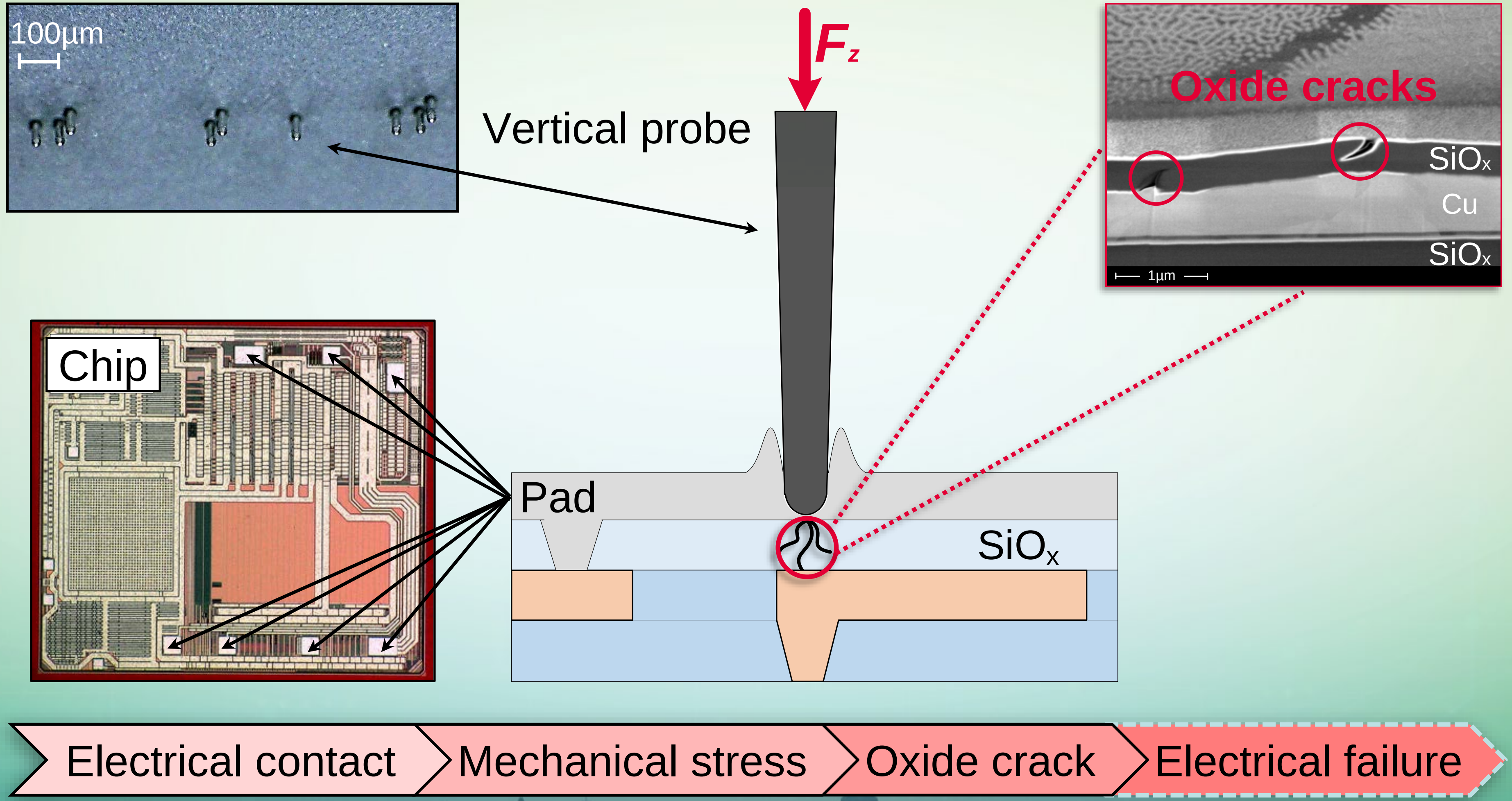


- ➔ up to 20% area savings
- ➔ cost reduction



BEOL Stack

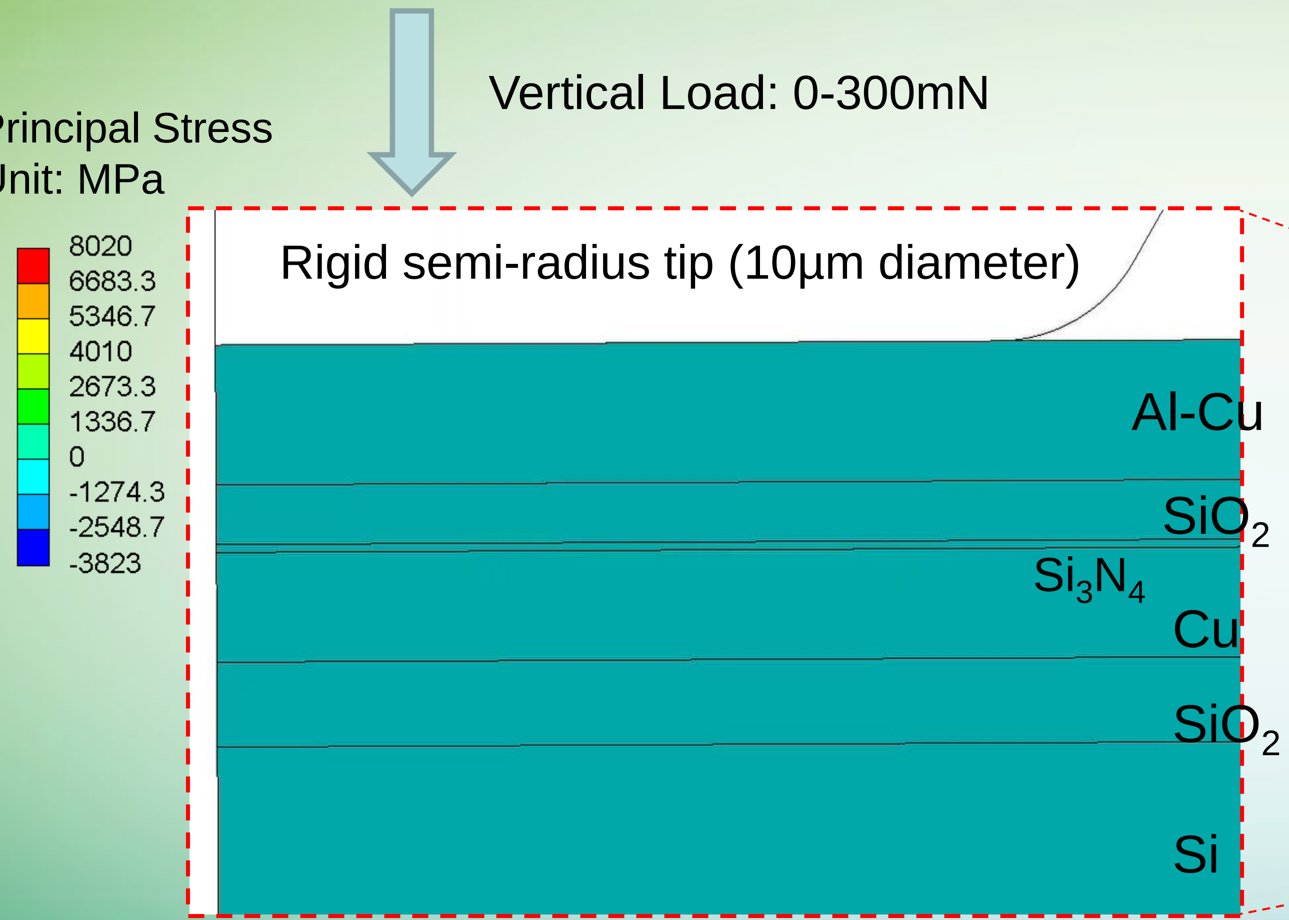
Challenges during POAA



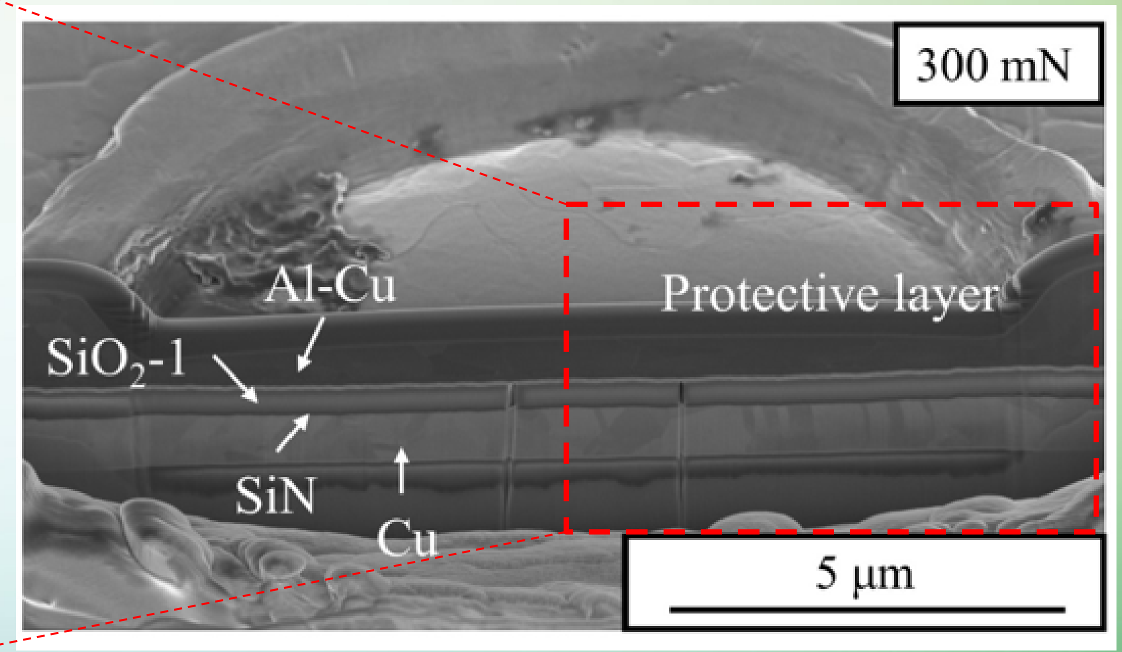
Stress in Layer Stack During Contacting

Vertical Load: 0-300mN

Principal Stress
Unit: MPa

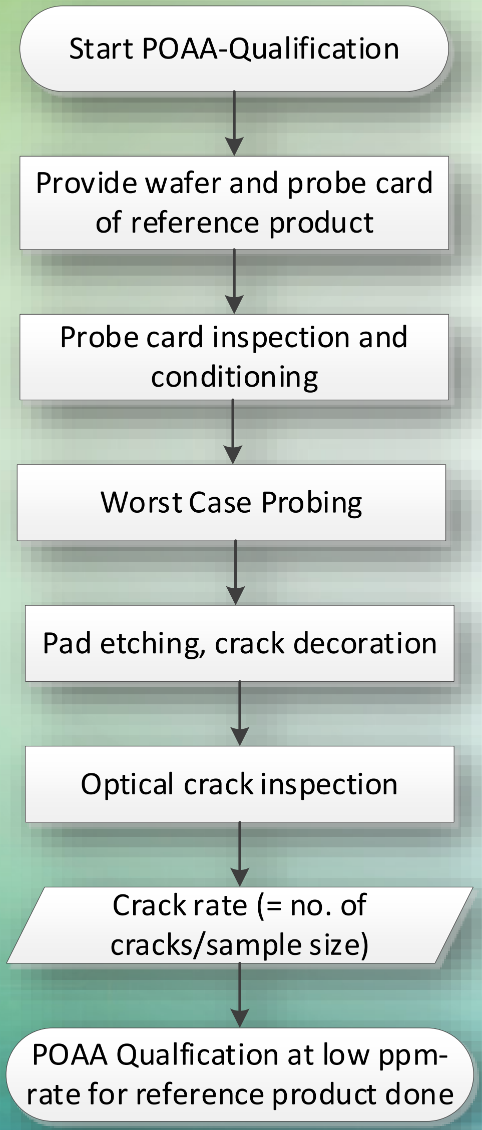


Stanford University
Author: Chen Liu



Tensile stress in Si_3N_3 layer initiating cracks in upper oxide layer

Classical POAA Qualification Process Flow

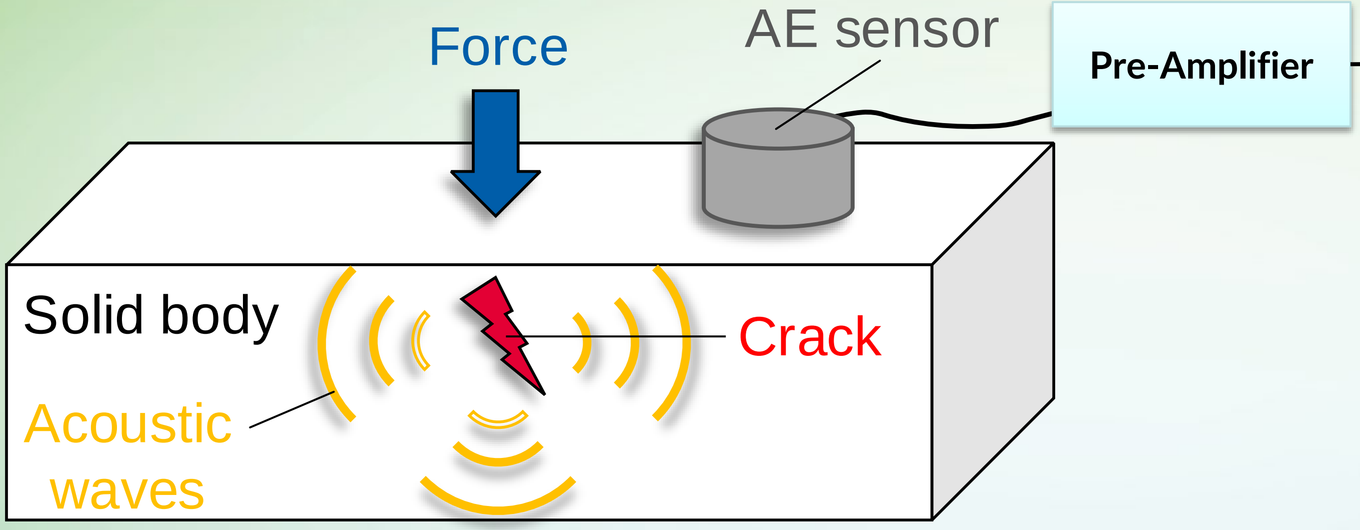


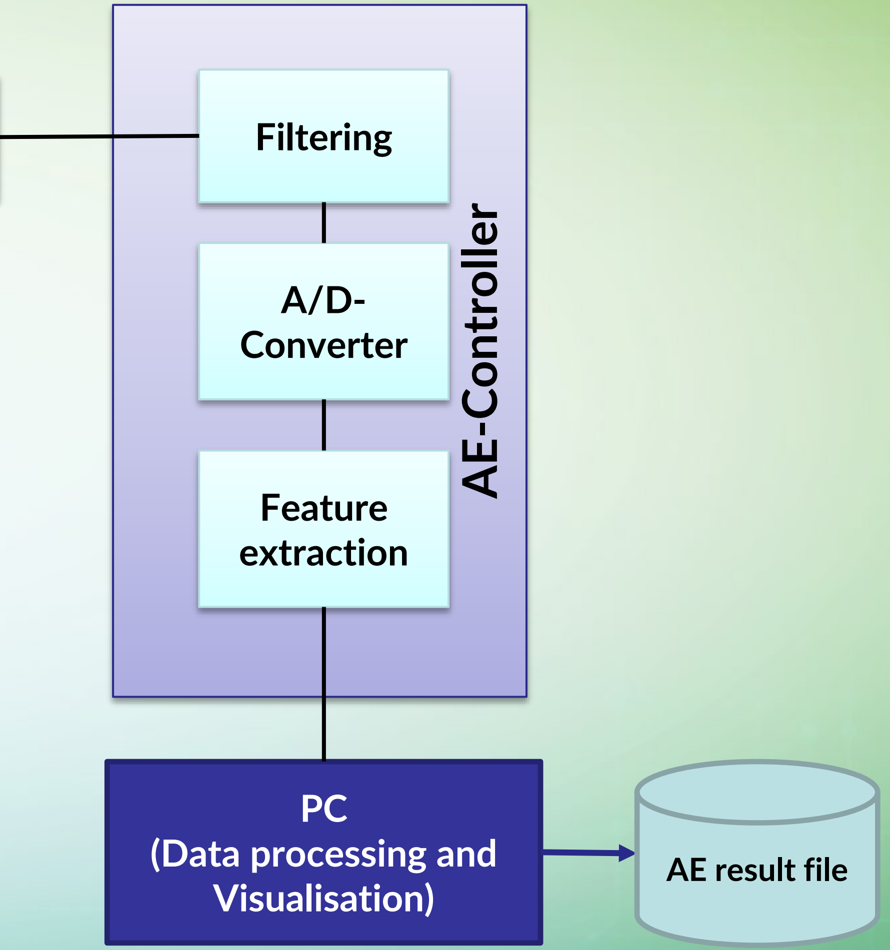
Disadvantages:

- At which contact stress do cracks initiate?
- Large sample size (up to 100k pads) needed to estimate crack risk at low ppm-level
- Optical inspection is time consuming and prone to human errors
- Critical probing parameters unknown
- Crack decoration method not applicable to certain pad stacks
- POAA qualification only possible at late phase of probing qualification

Find a faster, more efficient and more reliable crack detection method

Principle of Acoustic Emission Testing





Event Monitoring

Condition Monitoring

Material Testing

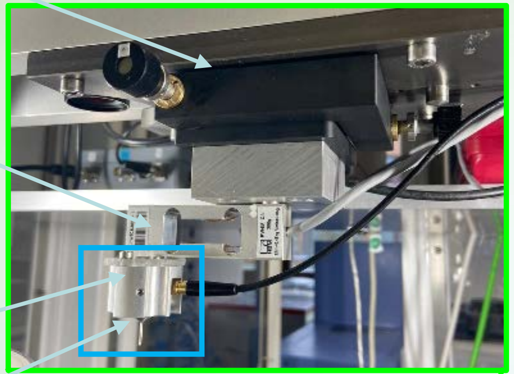
Test Bench *PROFIT*-2

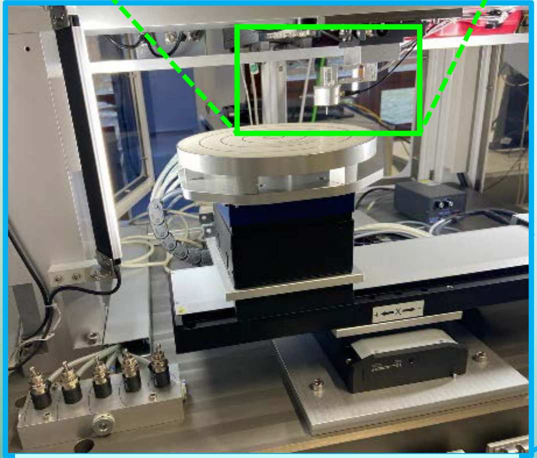
2-axis tilting stage

z-force sensor

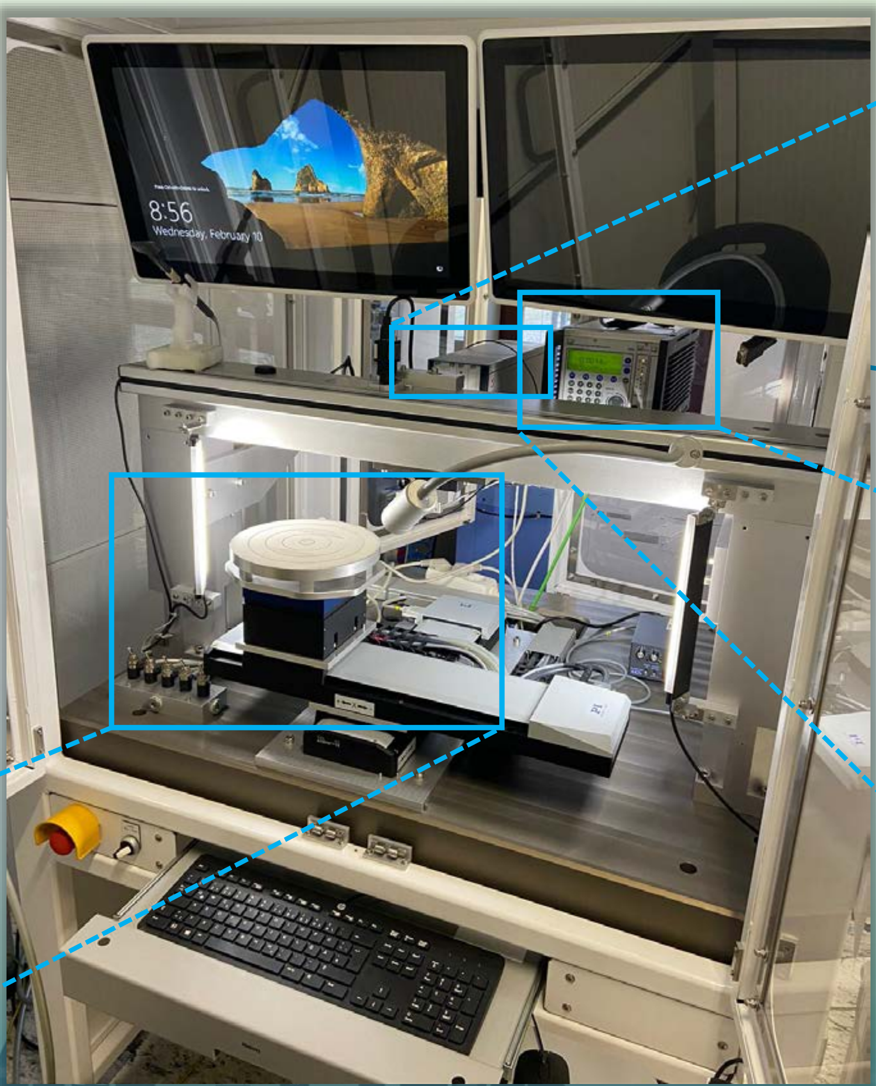
AE sensor holder

Sensor-indenter system





3-axis motorized stage with 200mm vacuum chuck

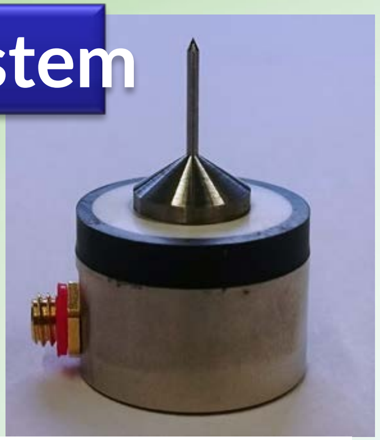


AE pre-amplifier & controller

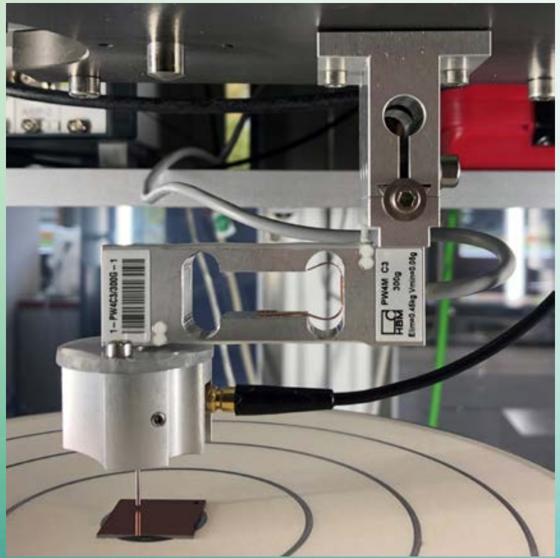
Force controller

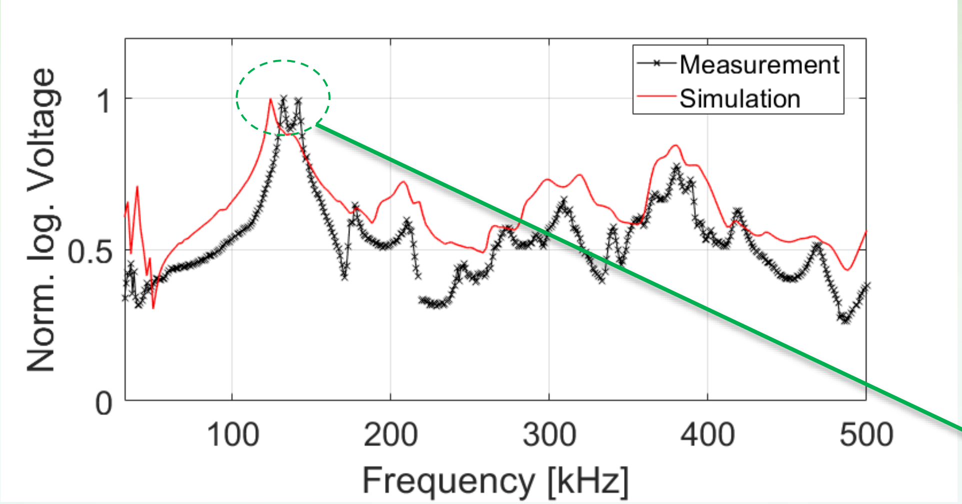
Resonating Sensor-Indenter System

Real System

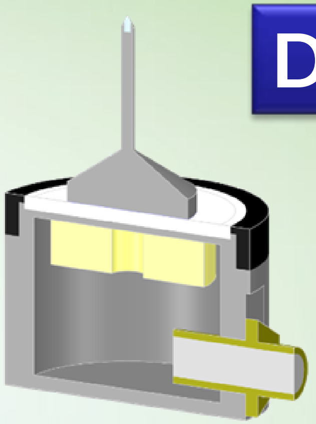


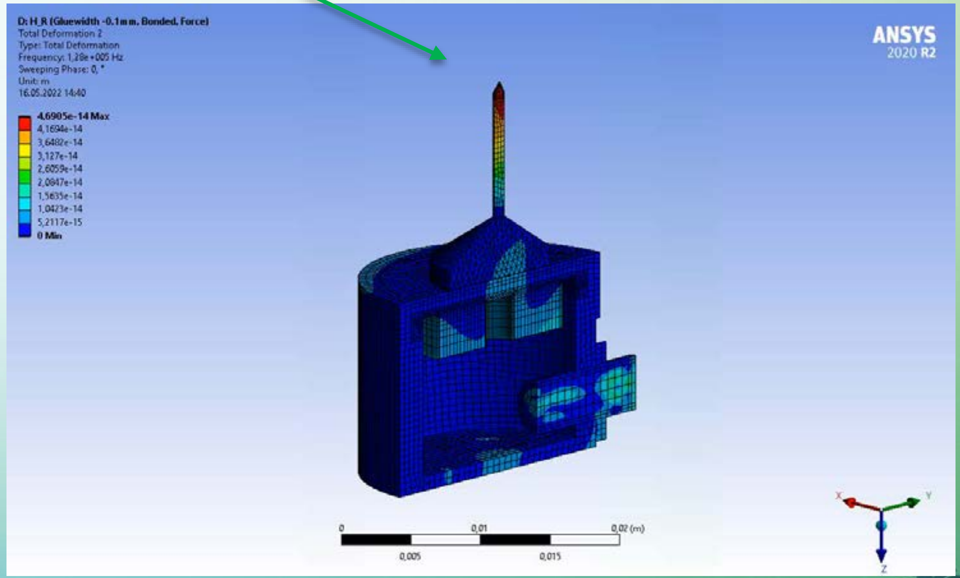
Patent No.: US 10,859,534 B2





Digital twin



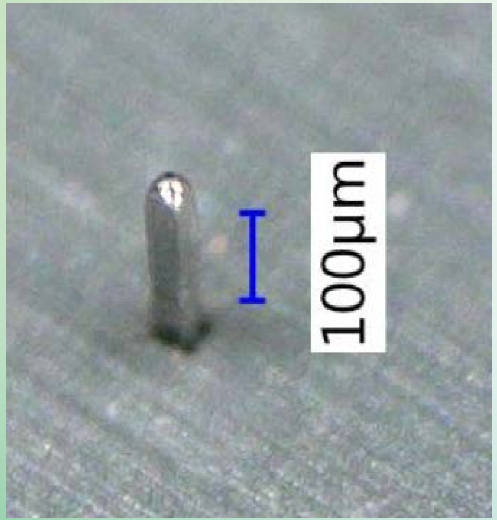


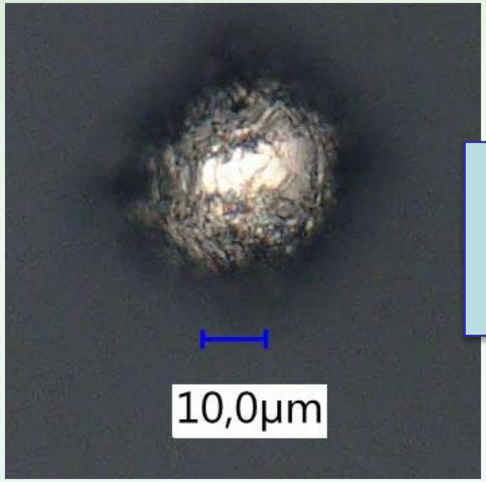
FEM-Simulations by PhD-student Florian Tremmel

Coupling of resonating sensor and indenter for high-sensitive acoustic signal detection

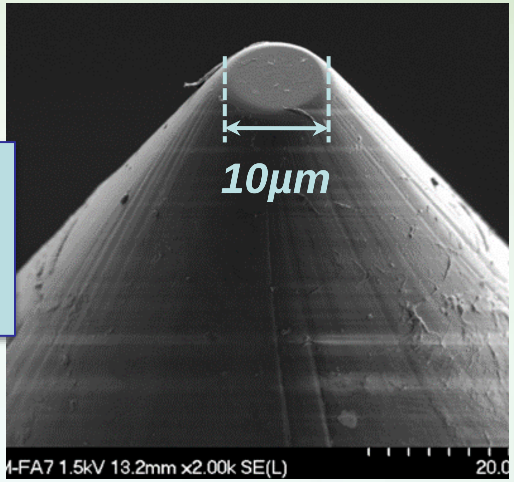
Comparison Probe vs. Indenter Tip and Probe Marks

Probe

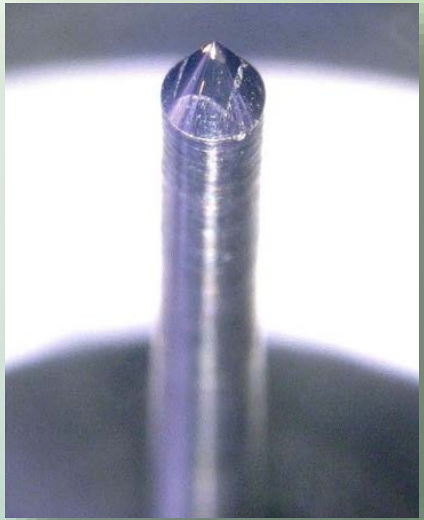


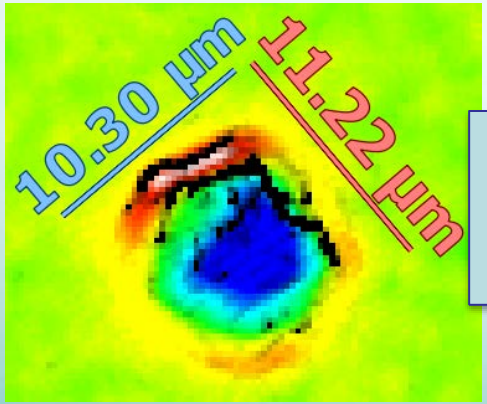


Similar Tip Shape and Size

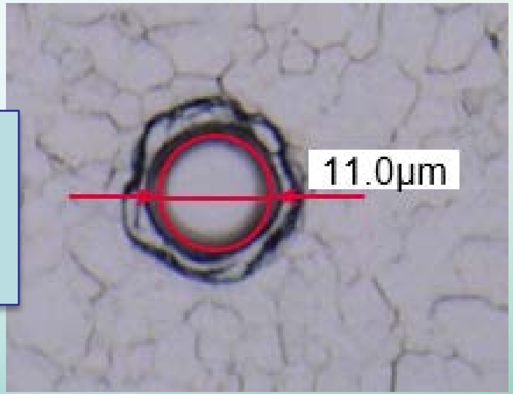


Indenter





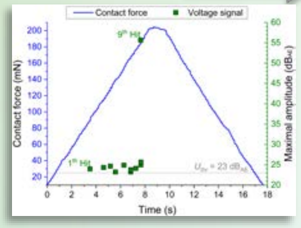
Similar Imprint Size and Depth



Crack Assessment Process Flow

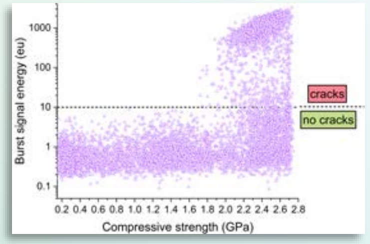
Step #1:

- Define probing-related contact parameters (tip shape, tip diameter, max. force)



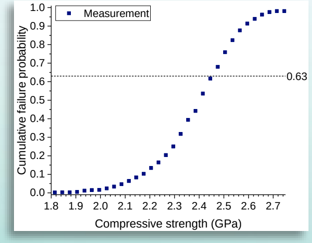
Step #2

- Repeat x-times contact cycle (sample size!) and record AE-data



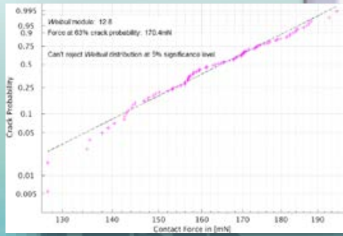
Step #3

- AE data processing (feature extraction and scatter plot)



Step #4

- Filter and cluster acoustic signal data for 1st cracks



Step #5

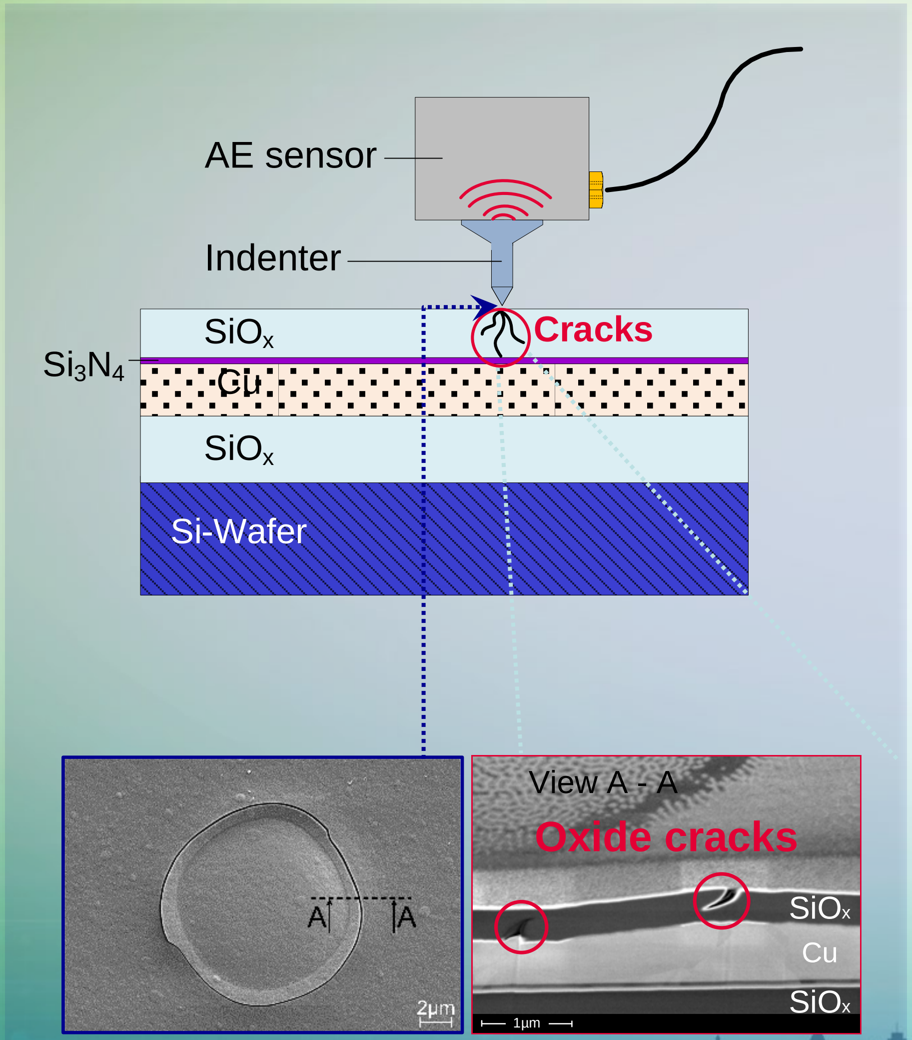
- Calculate and plot cumulative crack probability function

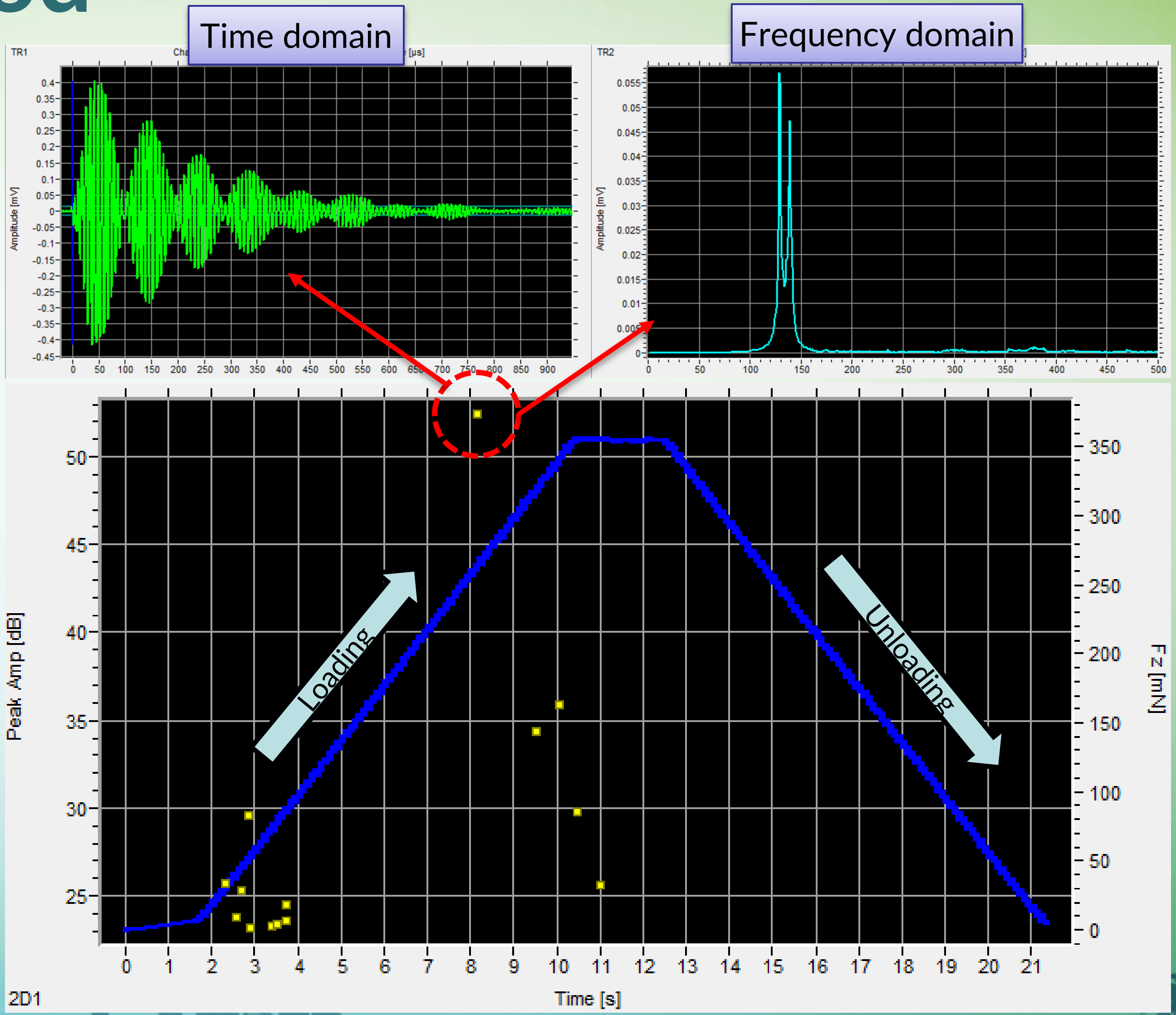
Step #6

- Extract characteristic Weibull parameters

F_0 = 233mN
m = 18.9

Thin Layer Crack Detection by AE-Test Method

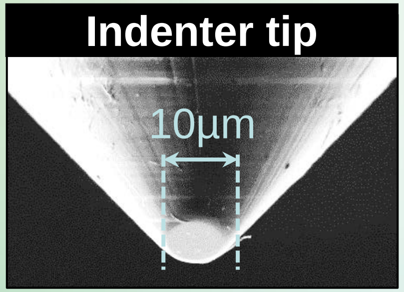


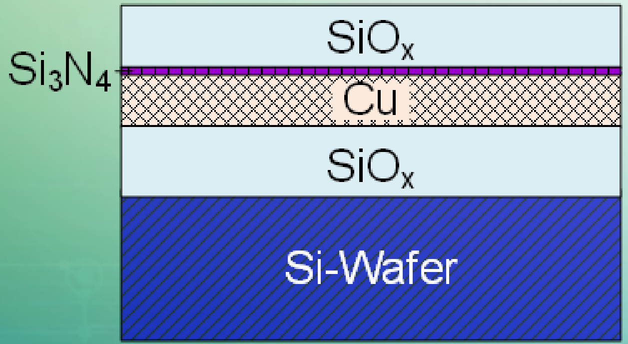


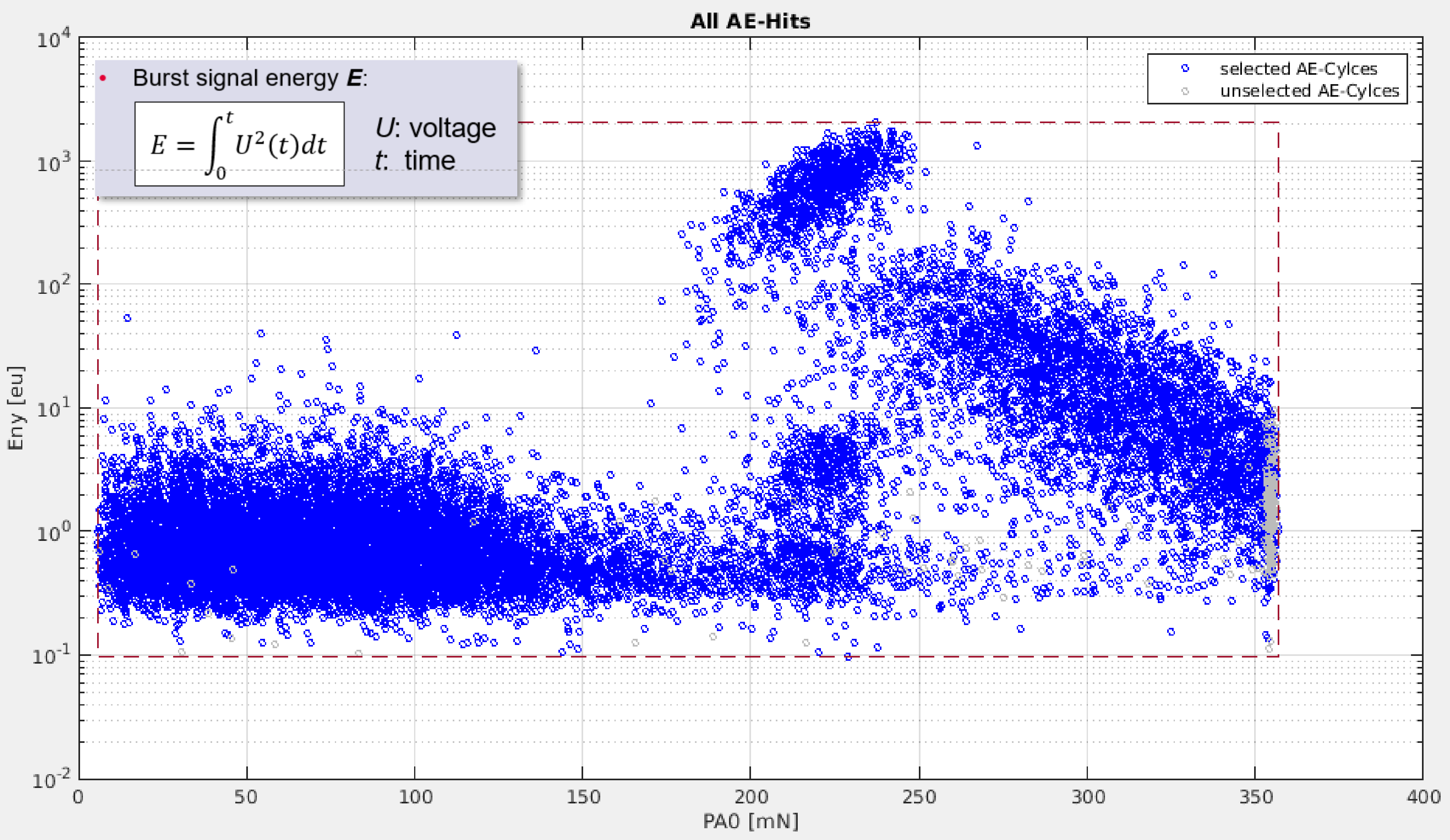
Scatter Plot of Multiple Contact Cycles

Experimental Settings:

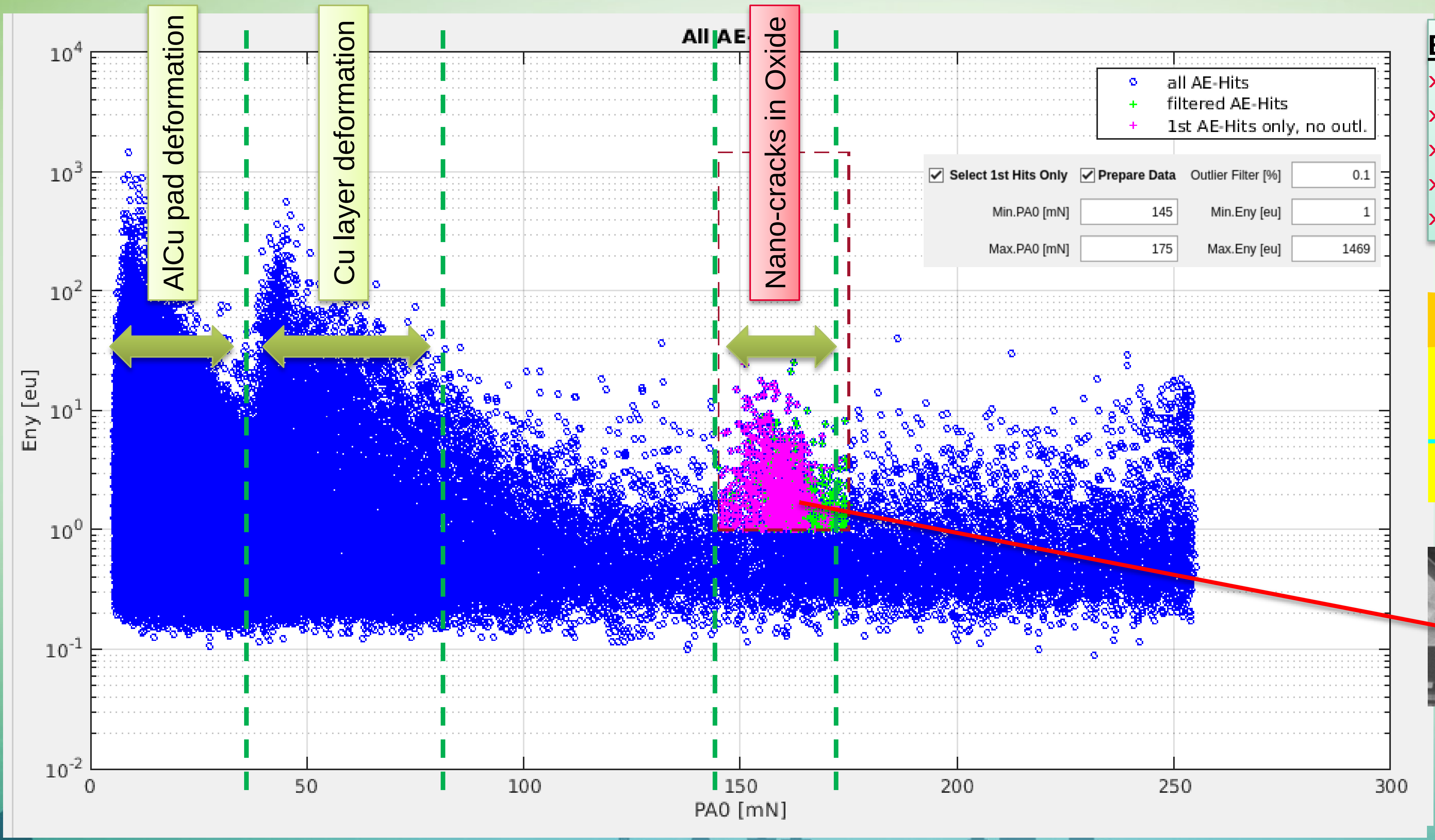
- Indenter tip: 10µm flat punch
- Unstructured test chip
- Sample Size: 1000 contact cycles
- Max. load: 350mN
- Chuck speed: 2µm/s





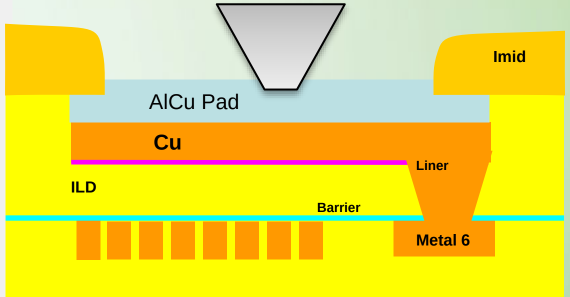


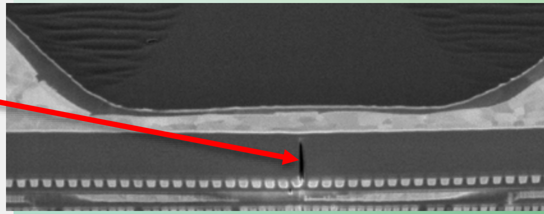
AE Data Filtering and Clustering



Experimental Settings:

- Indenter tip: 5µm flat punch
- 28nm CMOS technology
- Sample Size: 945 contact cycles
- Max. load: 250mN
- Chuck speed: 2µm/s





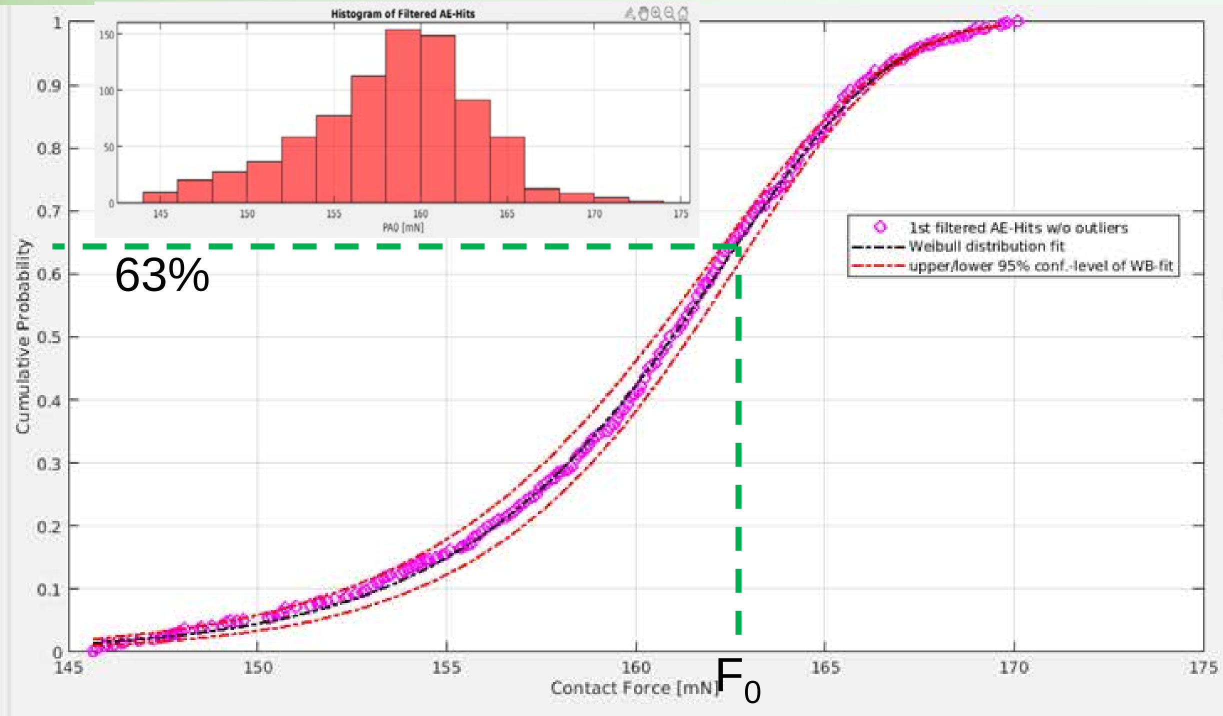
Optical crack correlation

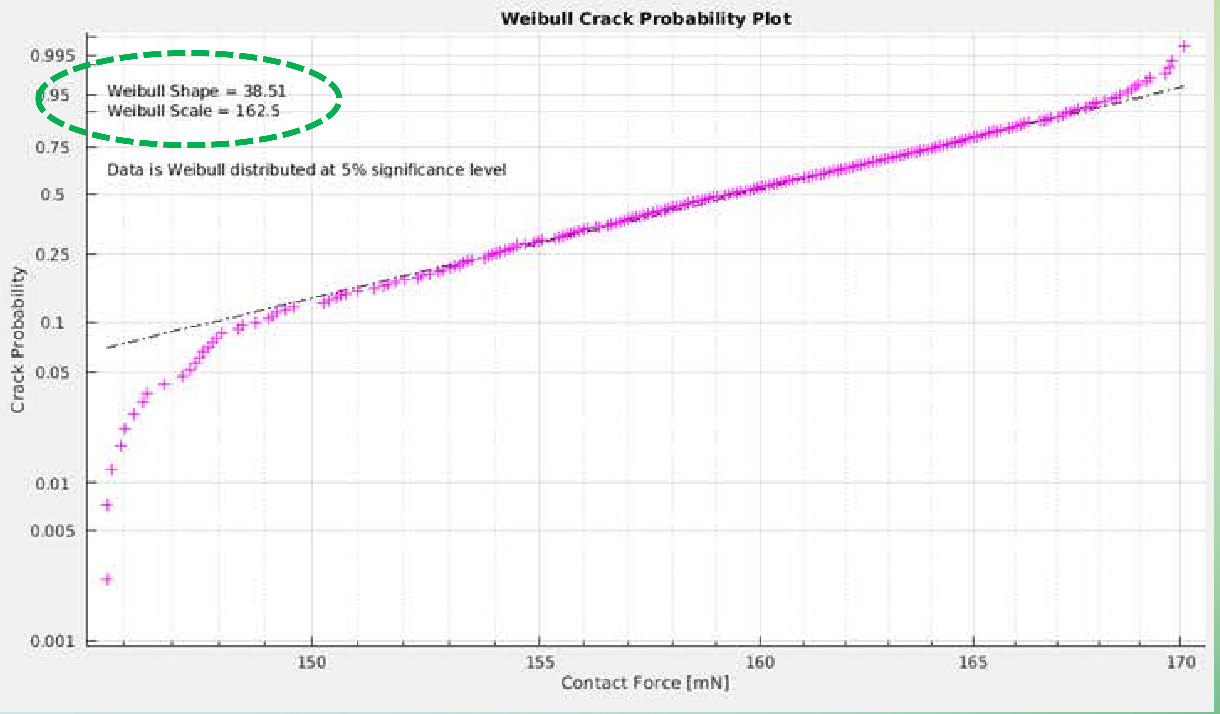
Crack Probability Plots

Cumulative crack probability

$$P_f(F) = 1 - e^{-\left(\frac{F}{F_0}\right)^m}$$

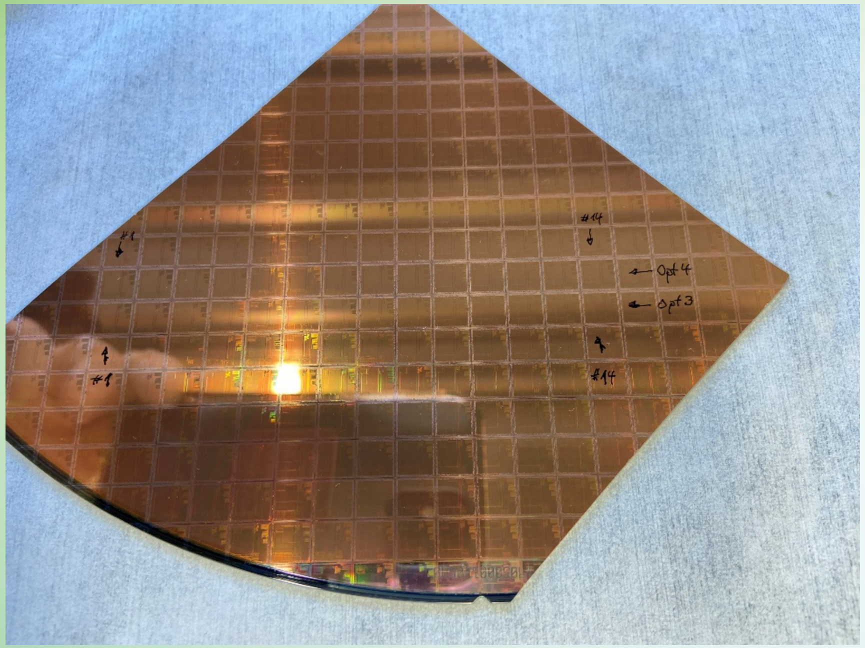
m: *Weibull* modulus
F_0: Characteristic contact force

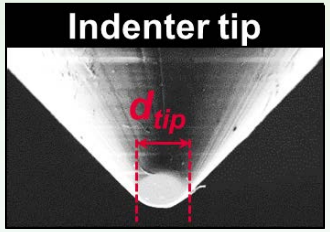




Weibull distribution function model is suitable to predict the crack probability of semiconductor layer stacks

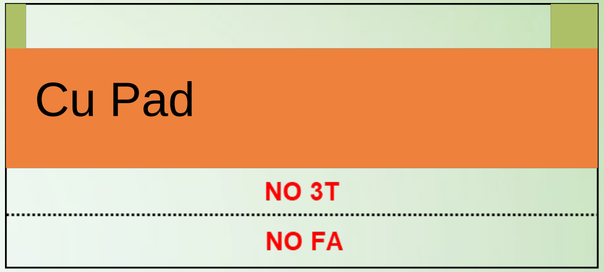
Application of AE-method for POAA-Qualification



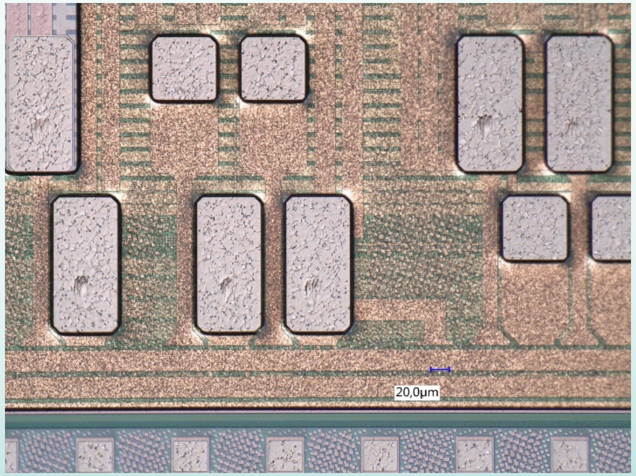


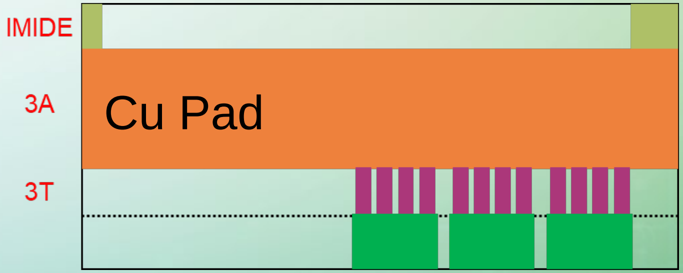
FP05: indenter with flat 5µm diameter diamond tip

FP10: indenter with flat 10µm diameter diamond tip



Pad Stack Option 4



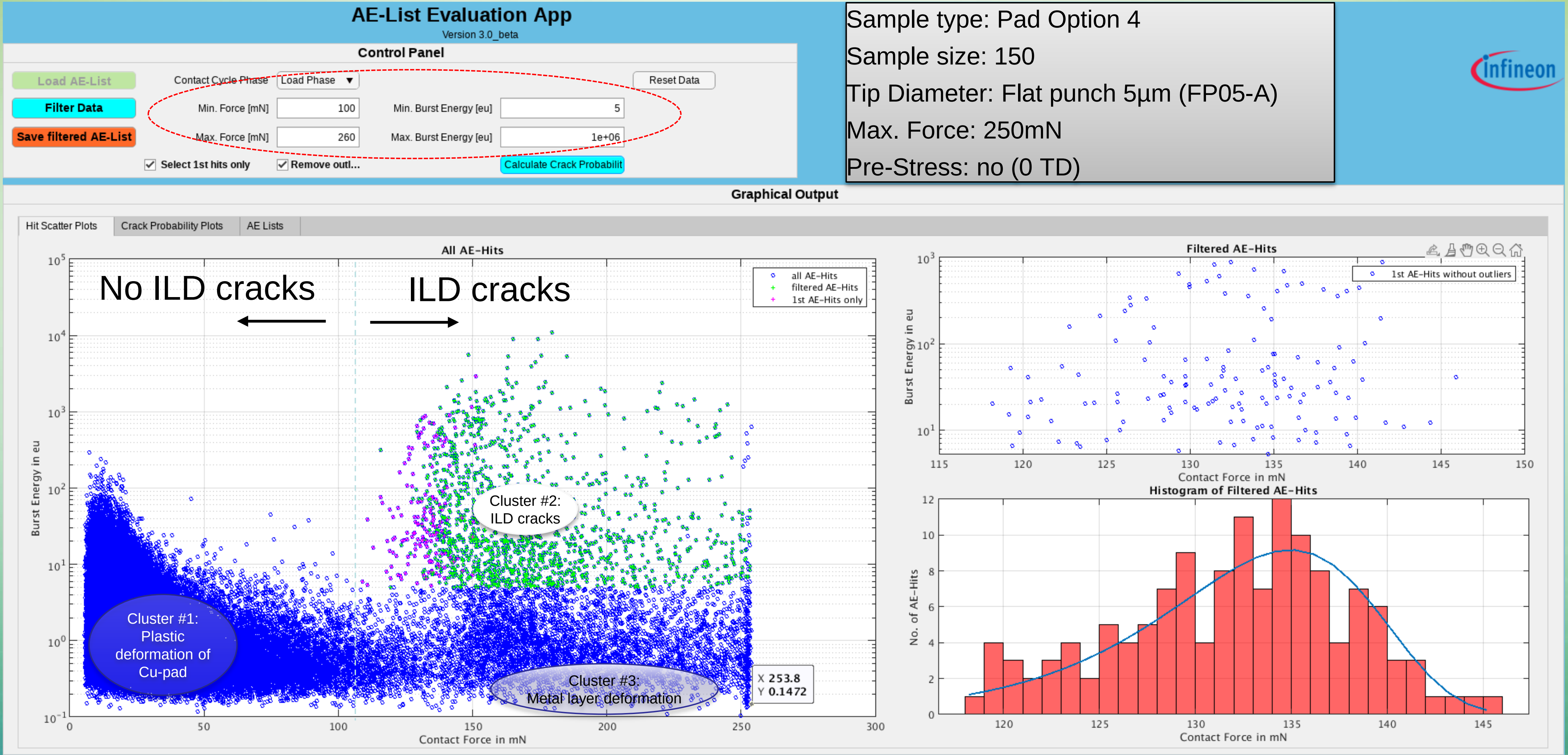


Pad Stack Option 3a

150x pads per option 3 and 4

15x contacted pads per chip
10 chips each per row

POAA-Qualification: AE-Data Analysis



Sample type: Pad Option 4

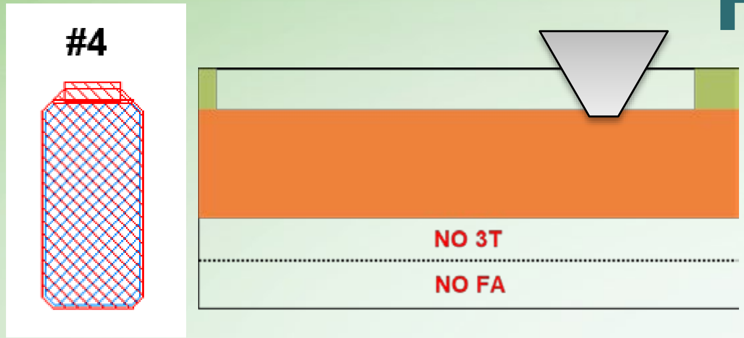
Sample size: 150

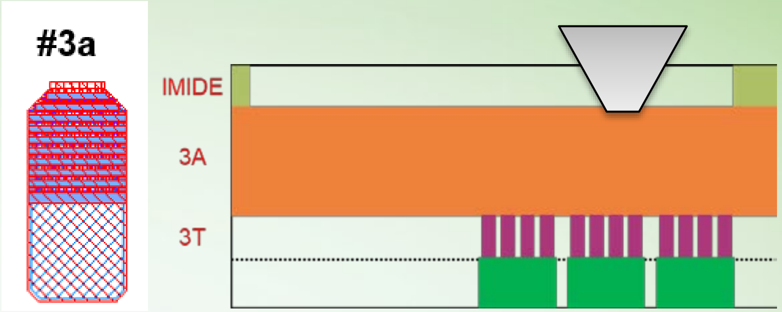
Tip Diameter: Flat punch 5µm (FP05-A)

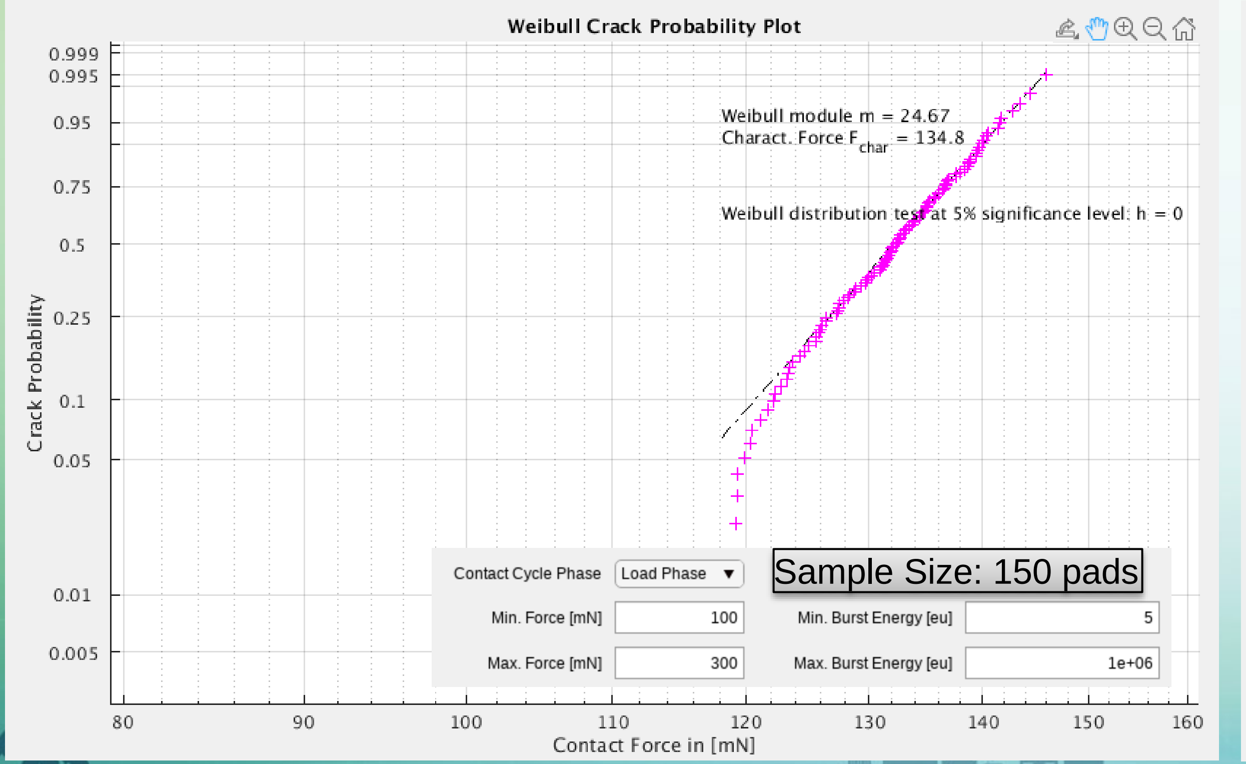
Max. Force: 250mN

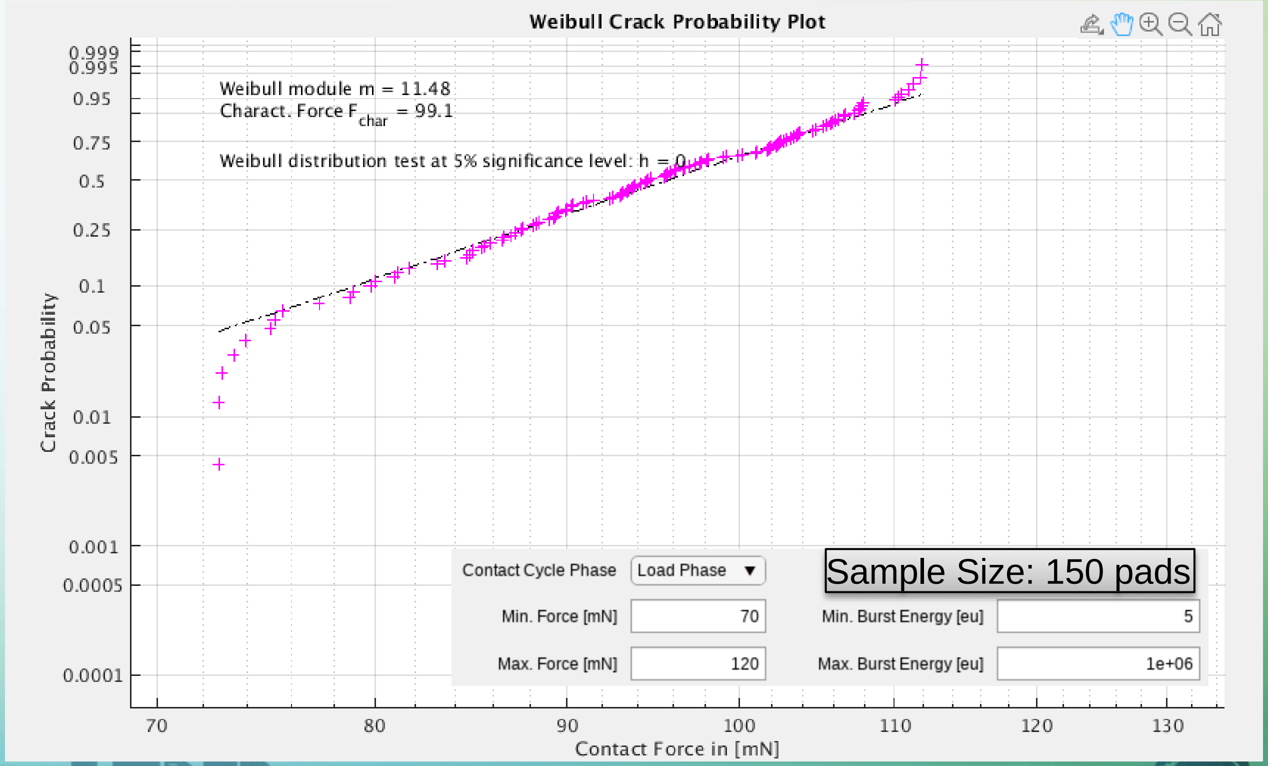
Pre-Stress: no (0 TD)

POAA-Qualification: Crack Probability Plots

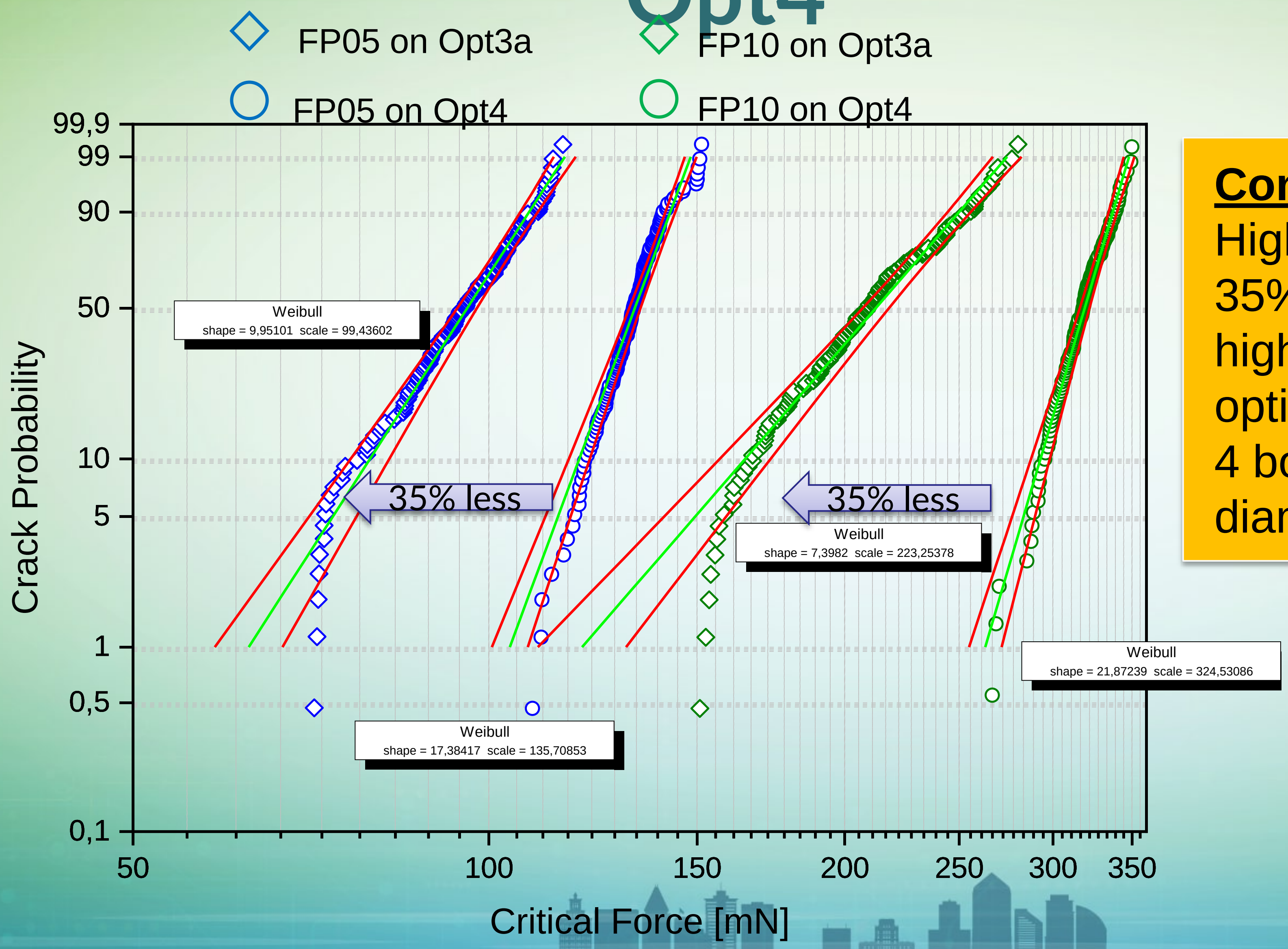








Crack Probability Pad Stack Opt3a vs. Opt4



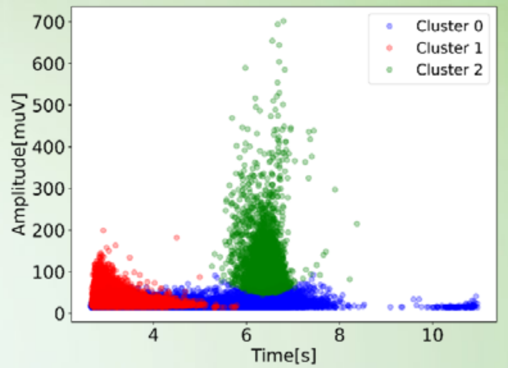
Conclusion:
Higher crack risk (approx. 35% lower critical force and higher variance) for pad stack option 3a compared to option 4 both for small and larger tip diameter

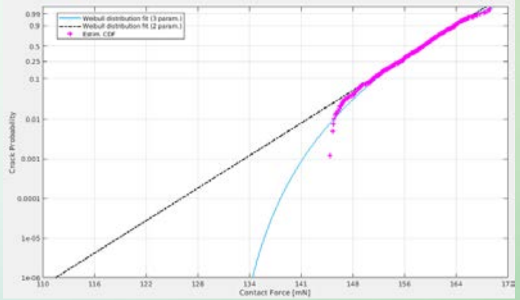
Summary

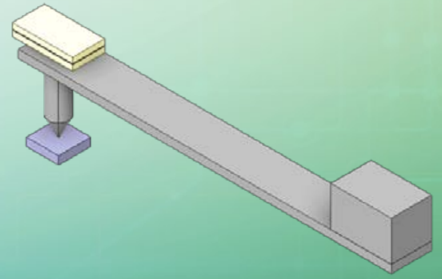
- Development of an innovative acoustic emission test method for thin layer crack detection
- Patented sensor-indenter system with high acoustic signal sensitivity and wide SNR
- Fast, reliable and accurate determination of POAA crack probability demonstrated
- New POAA qualification method introduced at Infineon for CMOS technologies to characterize BEOL stack robustness

Follow-On Work

- AE-Data Clustering by Machine Learning
- Improved statistical model (3-parametric Weibull model)
- Consider more probing parameters (multi-TD, lateral scrub, dynamics) for crack robustness
- Extension of AE-test method to power technologies
- Test bench feature upgrades (AE-signal triggering, hot/cold chuck)
- Integration of AE-sensor element with probe needle
- Industry standardization for POAA crack







Acknowledgment

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  - Dr. Eric Liau
  - Georg Georgakos
- **Stanford University**
  - Prof. Debbie Senesky
  - PhD-candidate Chen Liu

Publication List (extract)

- Unterreitmeier, M., et al. "An acoustic emission sensor system for thin layer crack detection." Microelectronics Reliability 88 (2018): 16-21.
- Unterreitmeier, M. “Contact related Failure Detection of Semiconductor Layer Stacks using an Acoustic Emission Test Method.” FAU Forschungen, Reihe B, Medizin, Naturwissenschaft, Technik Band 33. Erlangen: FAU University Press. DOI: 10.25593/978-3-96147-306-9.
- Liu, C., Nagler, O., Tremmel, F., Unterreitmeier, M., Frick, J. J., Patil, R. P., Gu, X.W., Senesky, D. G. “Cluster-based acoustic emission signal processing and loading rate effects study of nanoindentation on thin filmstack structures.” Mechanical Systems and Signal Processing, 165, 108301.
- Unterreitmeier, M., Nagler, O. “Determination of Indenter crack probability on Multilayer Stacks Using an Acoustic Emission Test Method." Electronic Device Failure Analysis (2022), Volume 24
- Liu, C., Nagler, O., Tremmel, F., Unterreitmeier, M., Frick, J.J., Gu, X.W., Senesky, D. G. “Thin Film Stack Structures Nanoindentation Characterization by Finite Element Analysis (FEA) and Experiments using Acoustic Emission Testing.” Materials Science in Semiconductor Processing. (Under review)