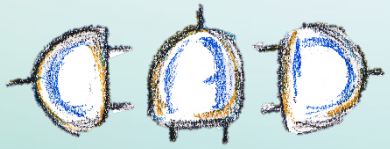
SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

Reducing test time by exploiting scan ATPG-based patterns targeting high density area in large Automotive Systems-on-Chip

Politecnico di Torino



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Outline

- Introduction.
- Goals.
- Background.
- Proposed approach.
- Experimental Results.
- Conclusions.
- Future works.

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Introduction

- Complexity of Automotive System-on-Chips is dramatically rising due to the demand for new efficient features in next-generation vehicles.
- The rising complexity leads to an abnormous increase in scan chain length and pattern test set, the primary sources of test duration.
- Growing Functional Safety requirements for safety-critical applications (i.e., ISO26262).
- Manufacturing test flow enhanced with additional steps, such as Burn-In stage and Final Test.
- Early found faults can reduce the manufacturing costs.

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Goals

- Our goal is to **explore possible solutions** for **reducing test time** with a minimal loss on the coverage but still maximize the yield expectation at the wafer level to avoid costly penalties in later test phases.

- Provide an automated framework for **fault criticality classification** according to **topology-related** information.

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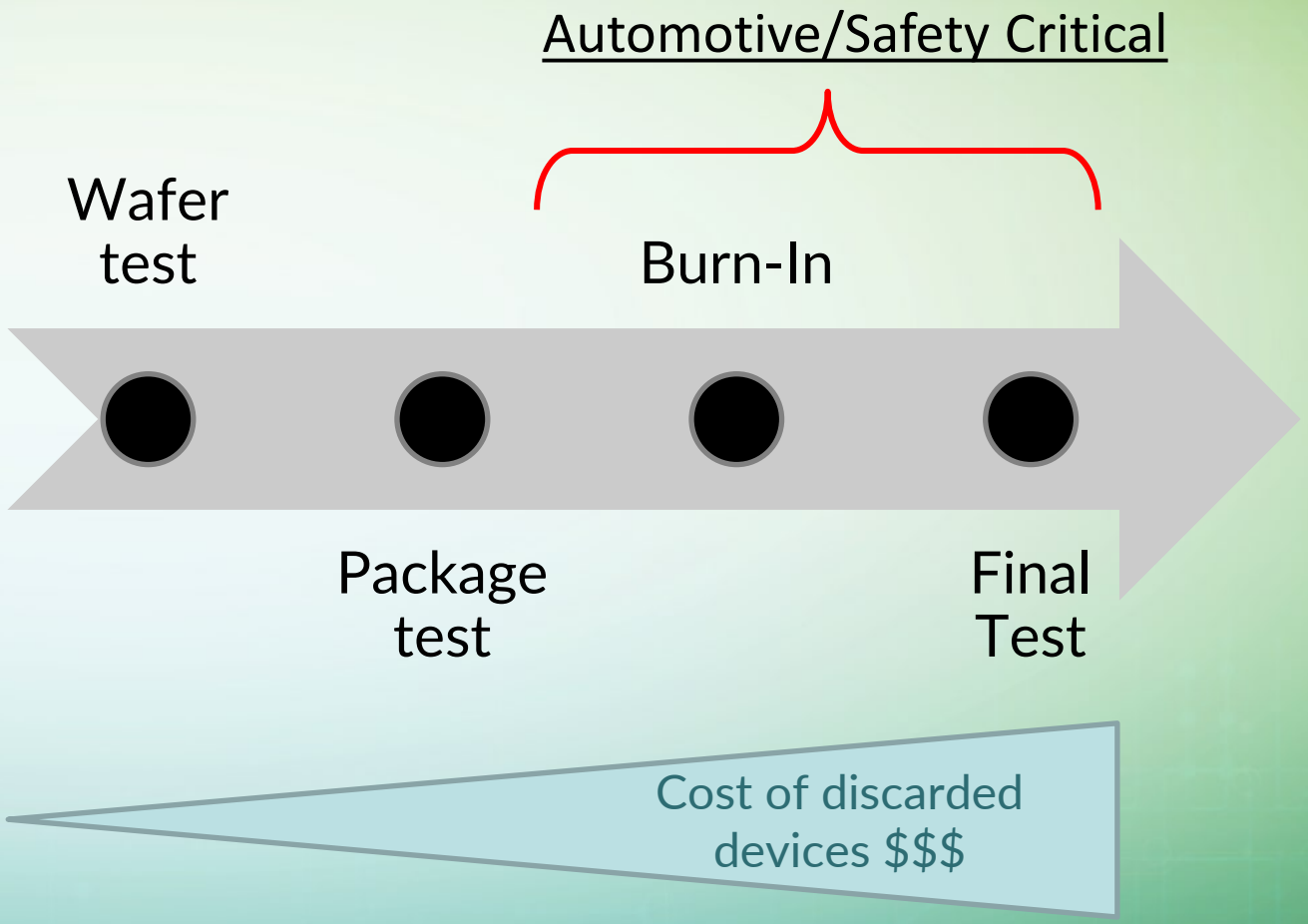
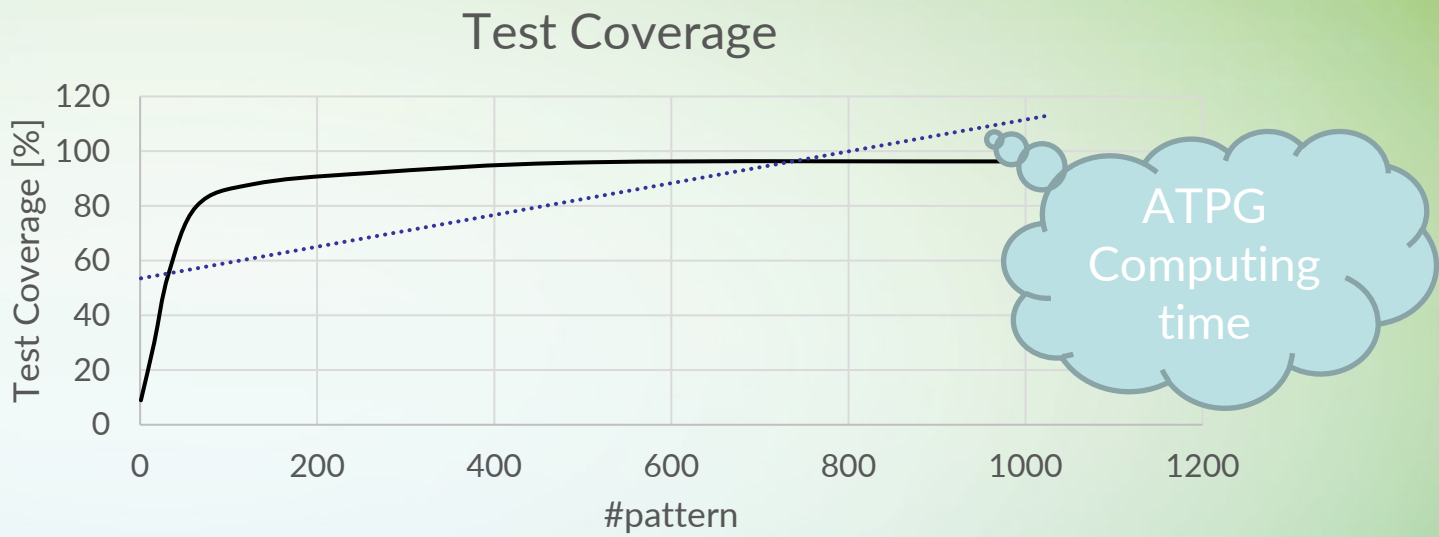
Background – Manufacturing Test Flow

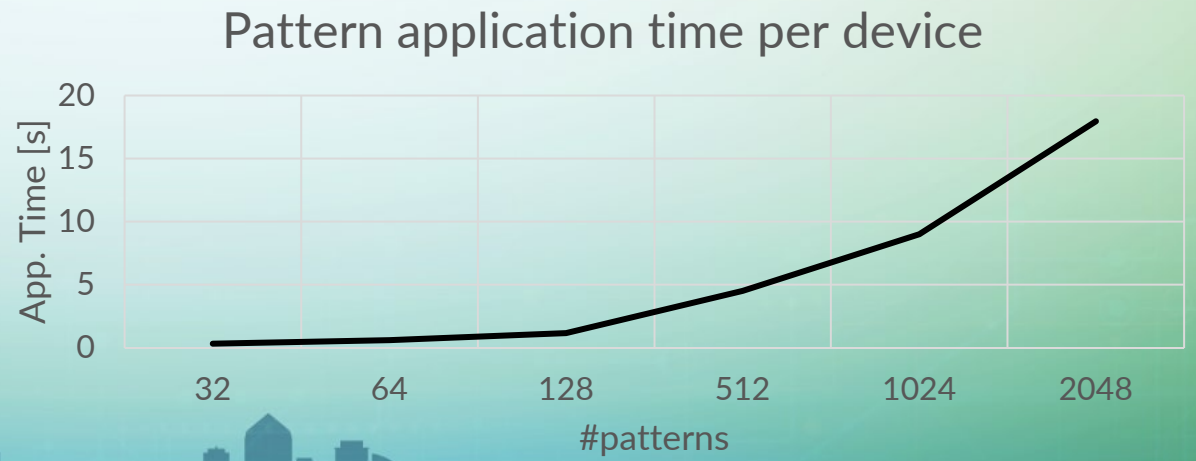
- Wafer test, it checks the primary functionality of the chip.
- Package test, it measures and tests the essential electrical characteristics of pins.
- Burn-In, for automotive applications, applies stress in order to exacerbate potential latent defects.
- Final Test, it applies a mix of structural and functional tests.



Background – ATPG

- Automatic Test Pattern Generator (ATPG) oversees identifying test vectors for devices.
- Computing time is directly proportional to complexity in terms of logic gates.
- Complexity impacts the scan chain length and number of generated patterns.





Background – Circuit topology

- Topology, including cell placement and routing, plays a crucial role in investigating new types of defects and their correlation.
- It influences electromagnetic interference and other defects.
- High-density areas in the layout are areas in which many cells are placed.

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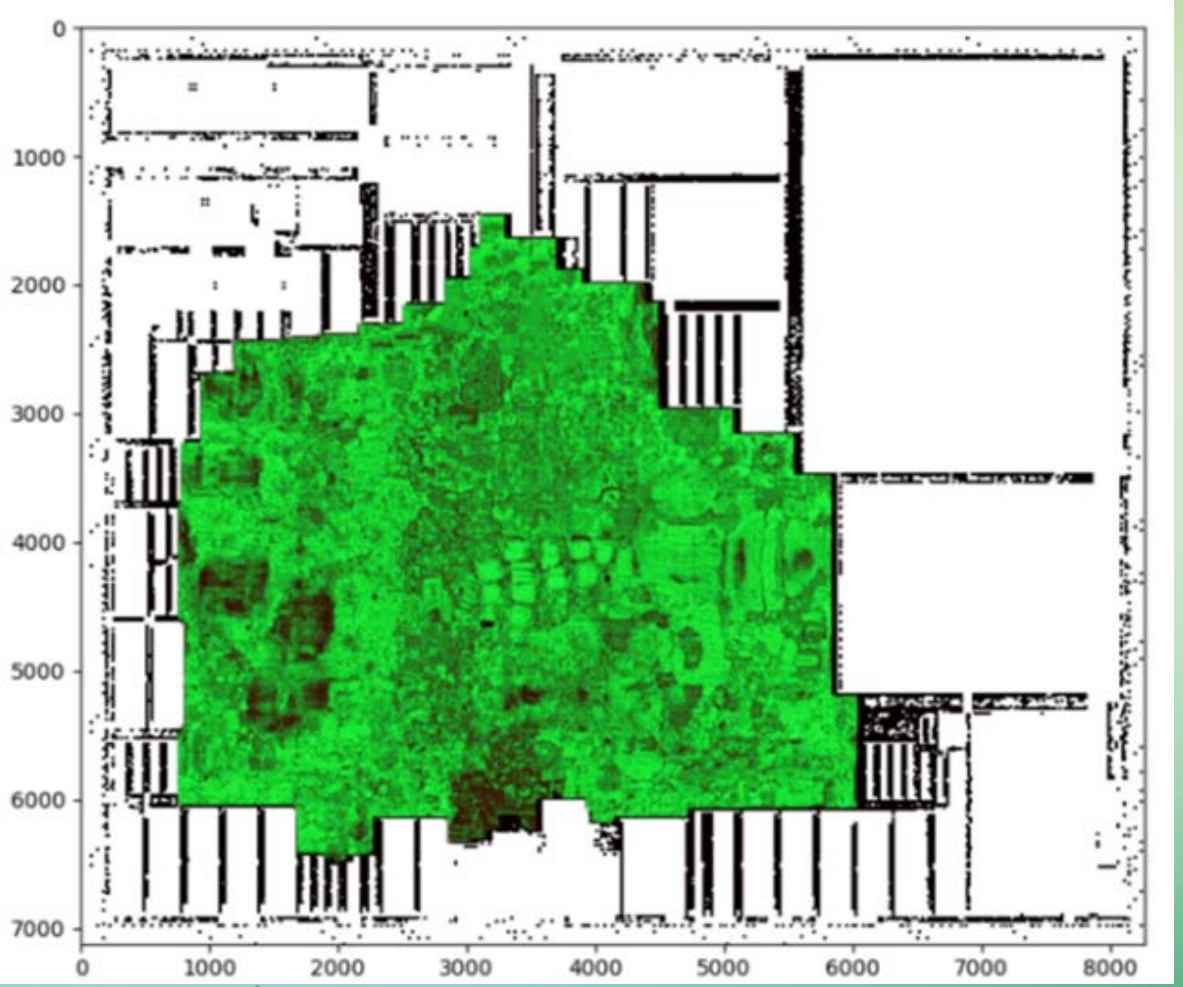
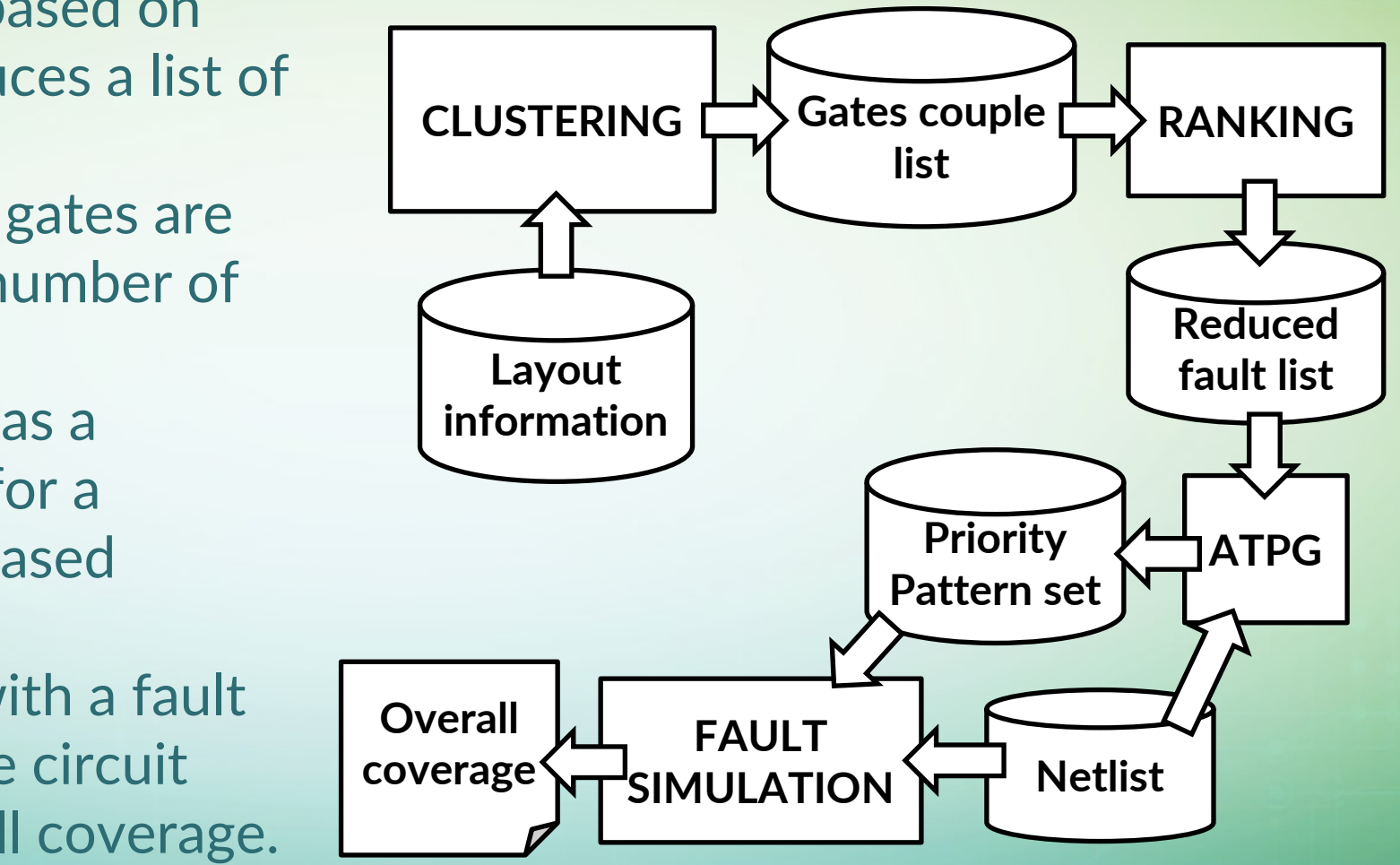
Proposed methodology

- Our proposed workflow for reducing test time in large Automotive System-on-Chips is based on the experimental observation of the physical layout of the device.
- It depicts a non-uniform distribution of gates in the front end.



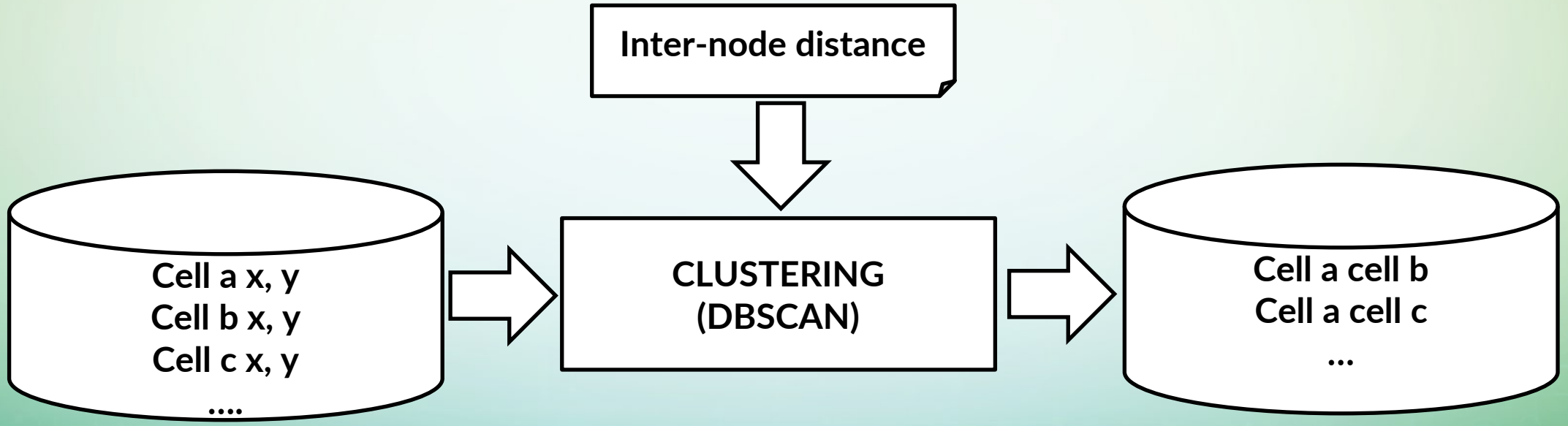
Proposed methodology

- Machine learning phase based on clustering methods produces a list of closed couples of gates.
- The produced couples of gates are ranked according to the number of couples they belong to.
- A subset of gates is used as a reduced fault list source for a priority-oriented ATPG-based pattern generation.
- The strategy concludes with a fault simulation over the whole circuit gates to obtain the overall coverage.



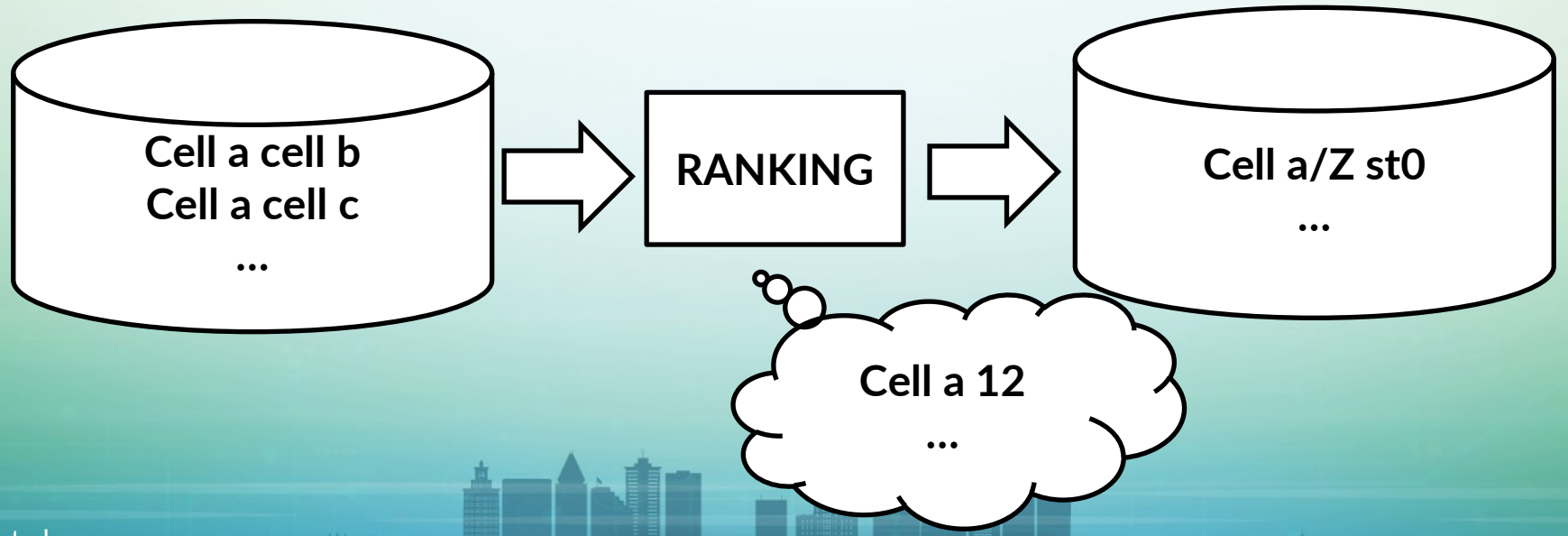
Proposed methodology – Clustering

- Using clustering-based Machine Learning to reduce the analysis time.
- The clustering algorithm can generate a list of couples of gates with a fixed inter-node distance.



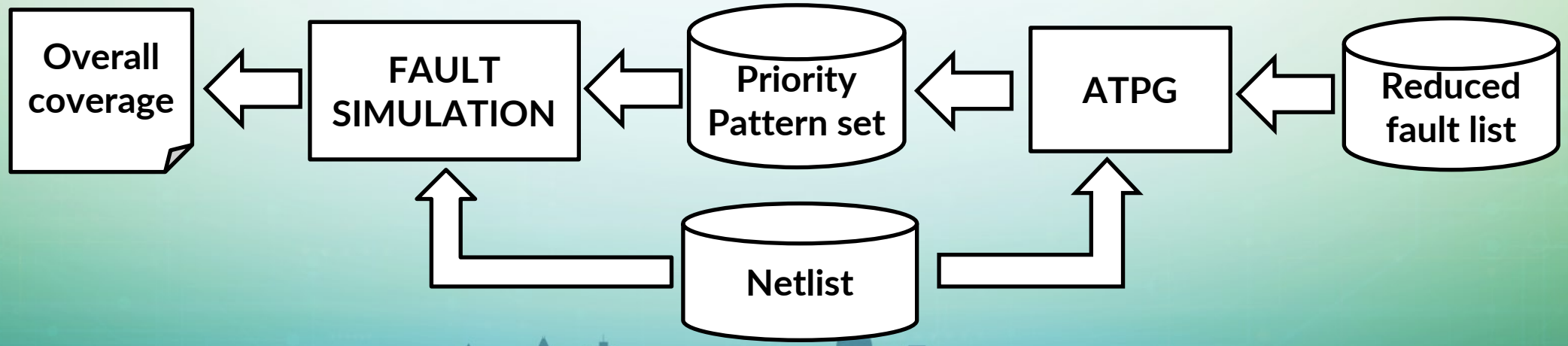
Proposed methodology – Ranking

- Ranking based on planar density (front-end information).
- Based on the assumption that cells with more neighbours' are more prone to errors.
- The ranking phase computes the number of neighbors for each cell and creates a fault list.



Proposed methodology – ATPG

- Priority scan pattern generation based on the reduced fault list, targeting high-density areas.
- Fault simulation to validate the generated patterns and obtain the overall test coverage over the complete Fault List.
- Priority pattern set can be applied with a tester.



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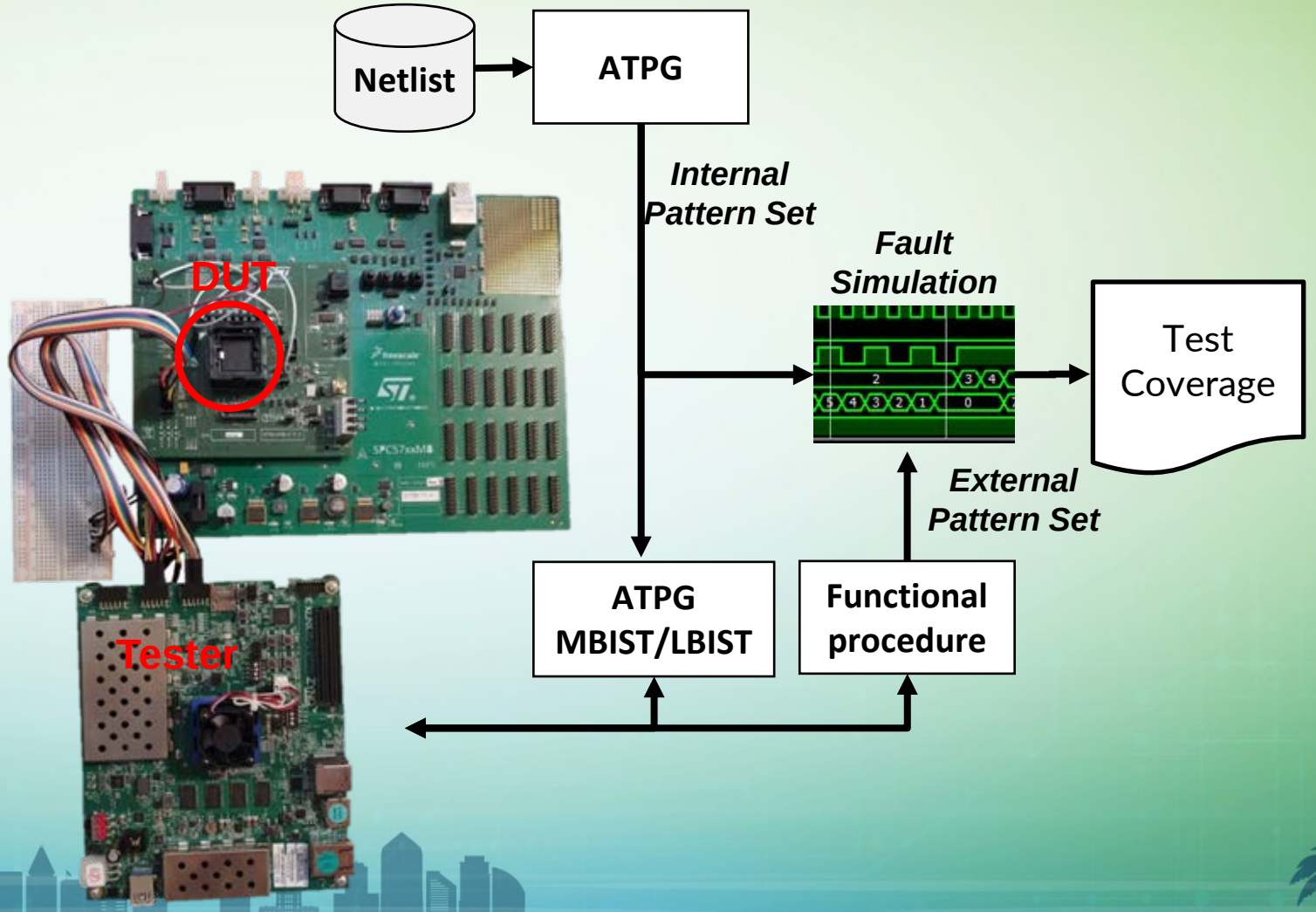
Experimental Setup

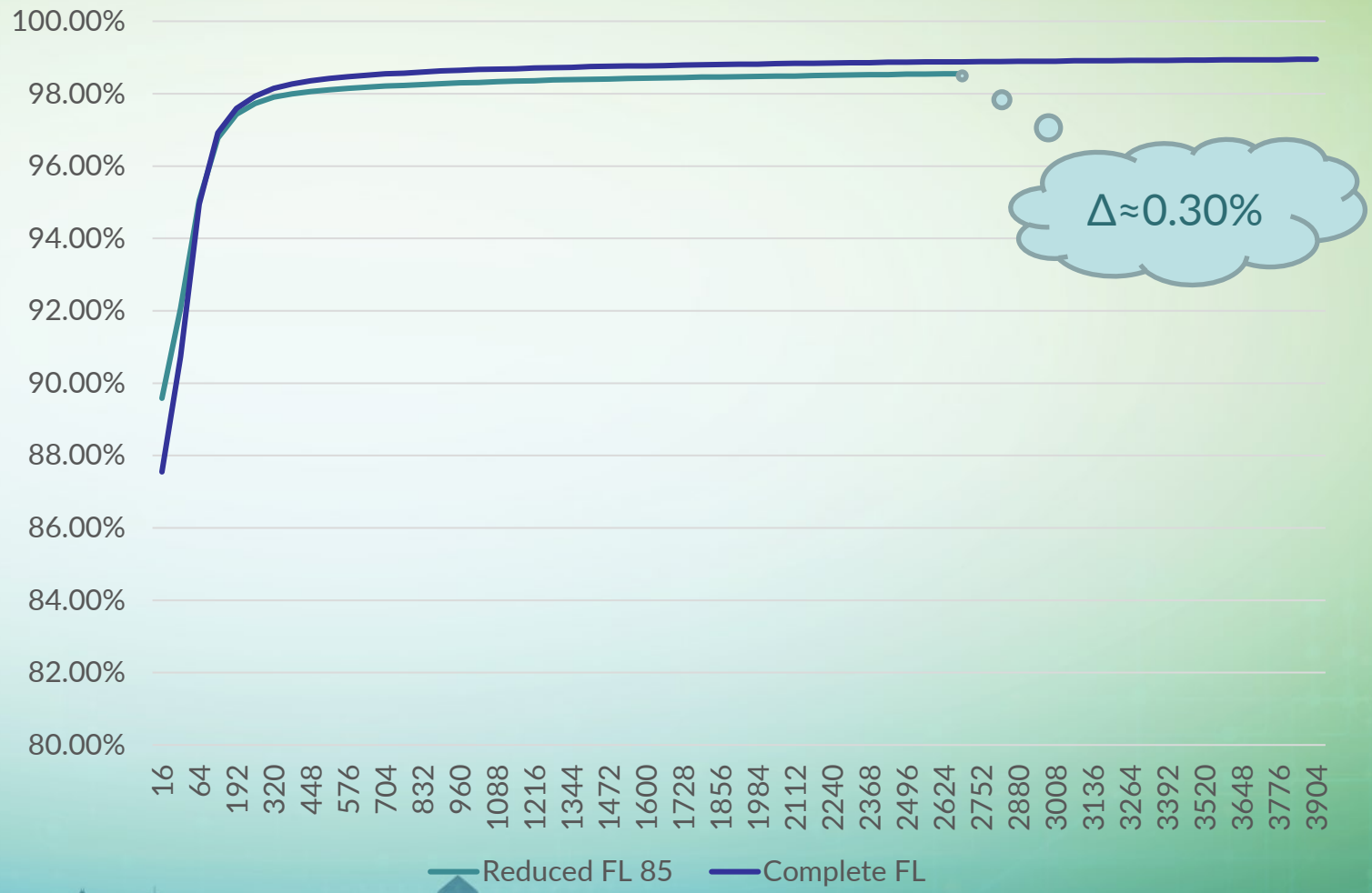
The case study is an Automotive SoC belonging to the SPC58 family produced by STMicroelectronics:

- 20 million gates.
- ~700K Flip flops.
- Multi-core architecture.
- ASIL-D compliant.
- Multiple test mode entry.



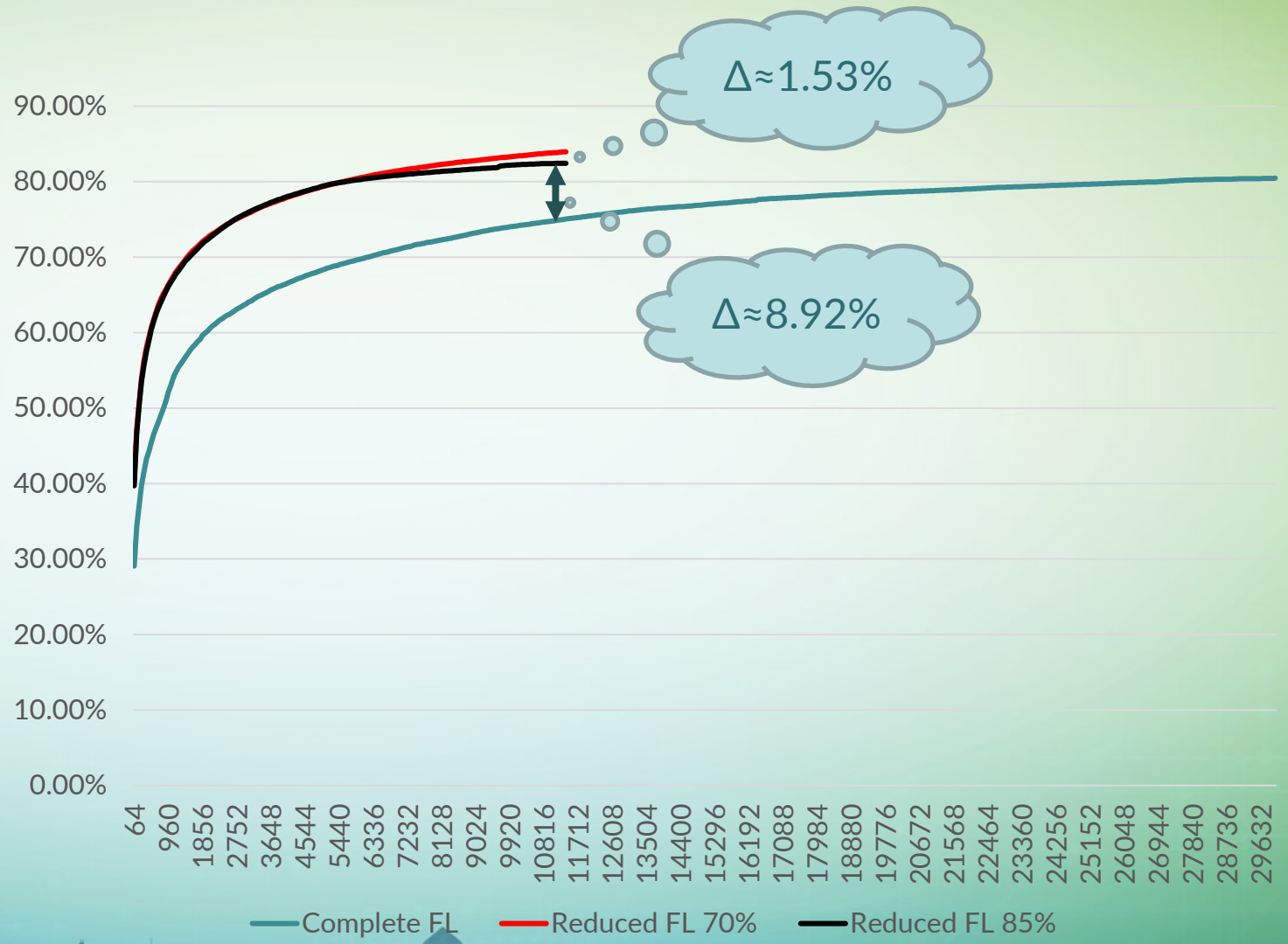
Experimental Results – Toggle Patterns

- Pattern generated targeting toggle metric for reduced Fault List.
- Pattern set size reduced by 1.45x.
- The pattern set generated from the reduced Fault List, targeting a high-density area, almost reaches the same as the complete pattern set.



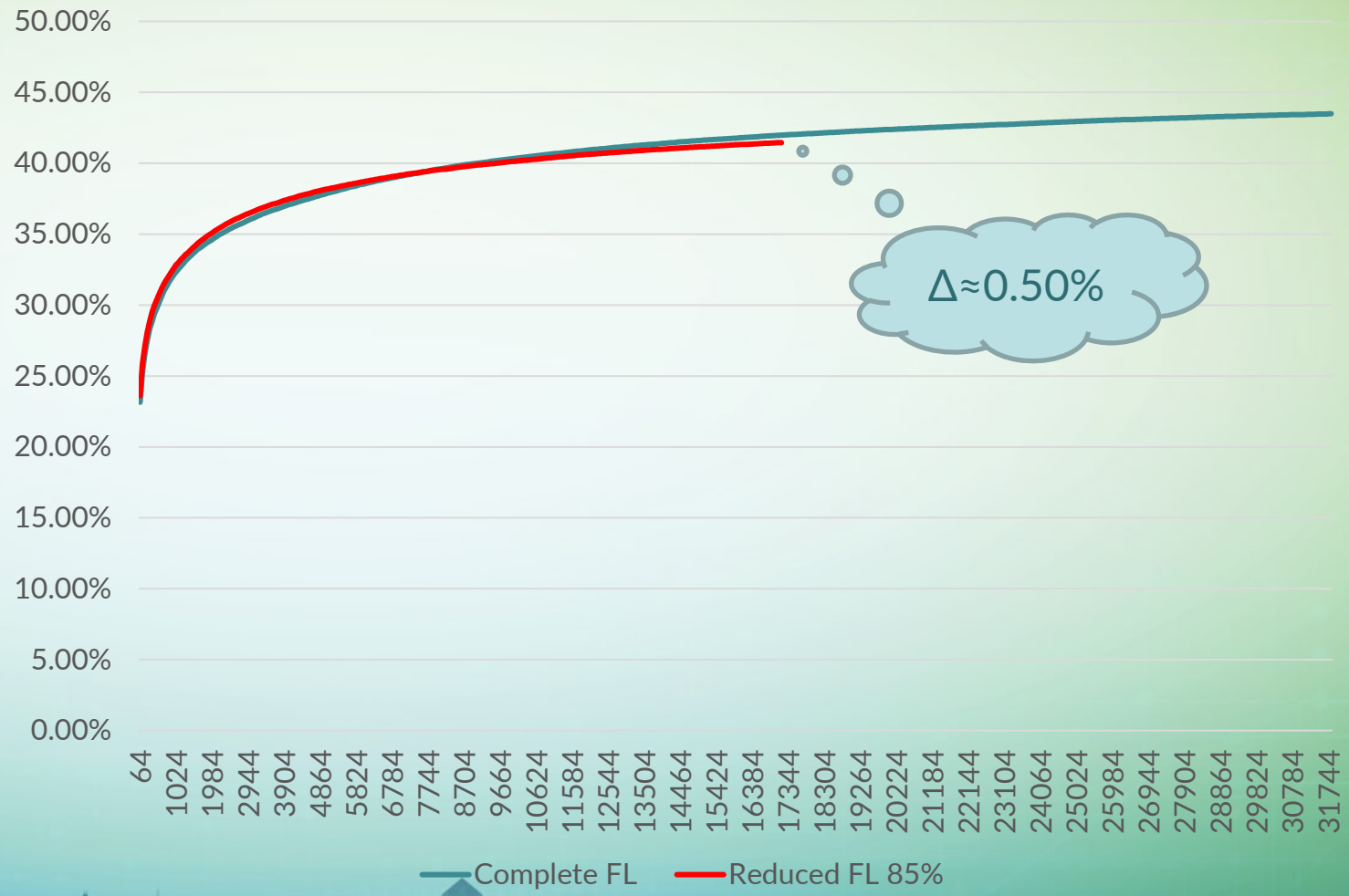
Experimental Results – Stuck at Patterns

- Pattern generated targeting fault metric for reduced Fault List.
- Pattern set size reduced by 2.63x.
- The pattern set generated from the reduced Fault List, targeting high-density areas, reaches higher coverages than the complete pattern set.



Experimental Results – Transition Delay Patterns

- Pattern generated targeting transition metric for reduced Fault List.
- Pattern set size reduced by 1.85x.
- The pattern set generated from the reduced Fault List, targeting high-density areas, almost reaches the same as the complete pattern set.



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Conclusions

- In safety-critical sectors, it is essential to guarantee high reliability, and due to the complexity of modern electronics systems, the testing process must be optimized in terms of time.
- Our methodology proposes a **possible solution to reduce the overall test time** in early manufacturing test steps **without drastically impacting the test metrics**.
- The **reduced Test set** targeting High-density areas **could screen faulty devices early in the manufacturing test**.
- The reduced test time leads at the wafer test level to increase the number of tested devices in the same amount of time.

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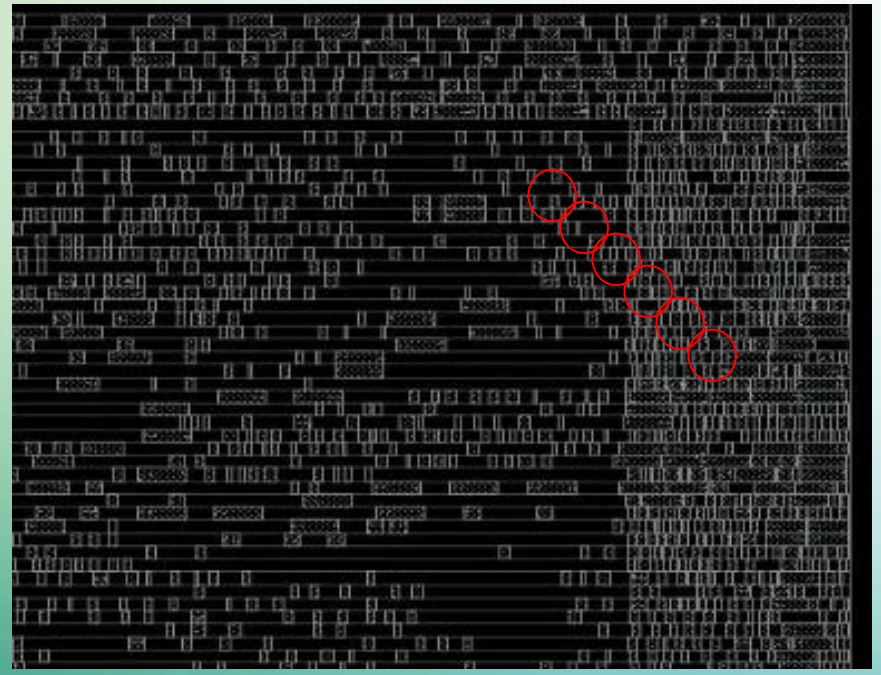
Future works

- Avail of 3-dimension density analysis.
- Analysis of critical interconnections.
- Cost analysis and impact on manufacturing test flow.

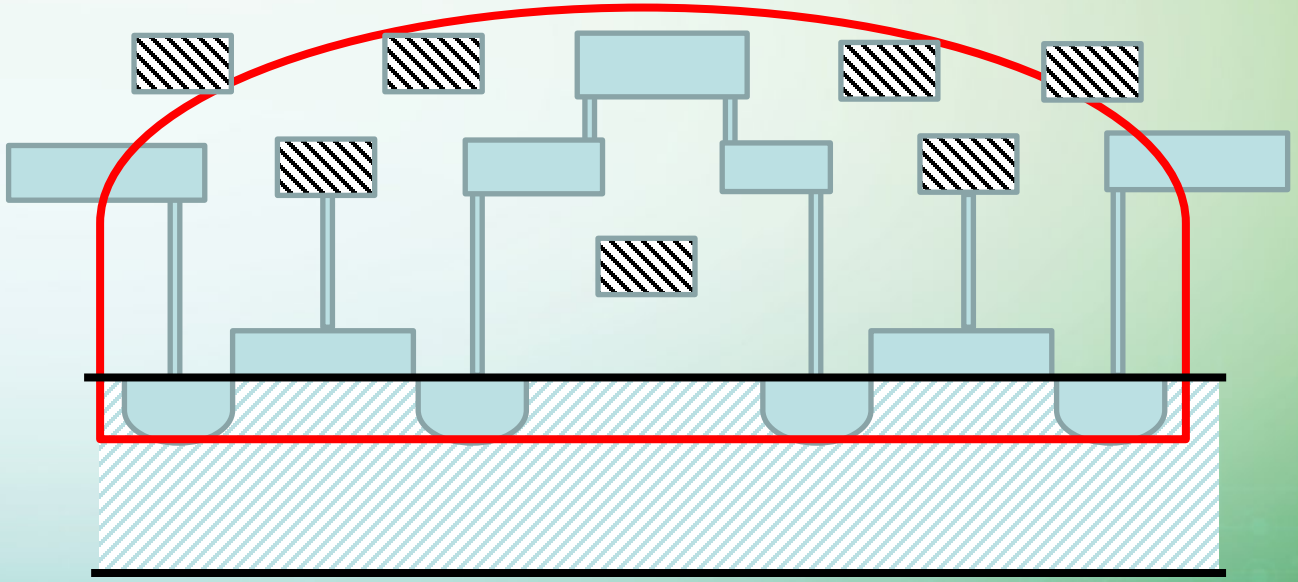
Future works – 3D density

- Inclusion of 3-dimension density analysis.
- Integrating the planar density based on the frontend with backend information.

Top view

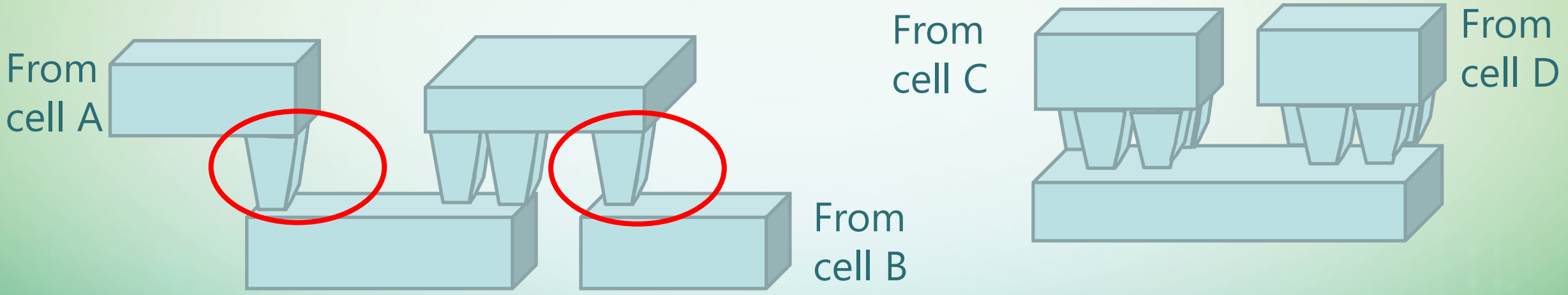


Section view



Future works – Analysis of Critical interconnections

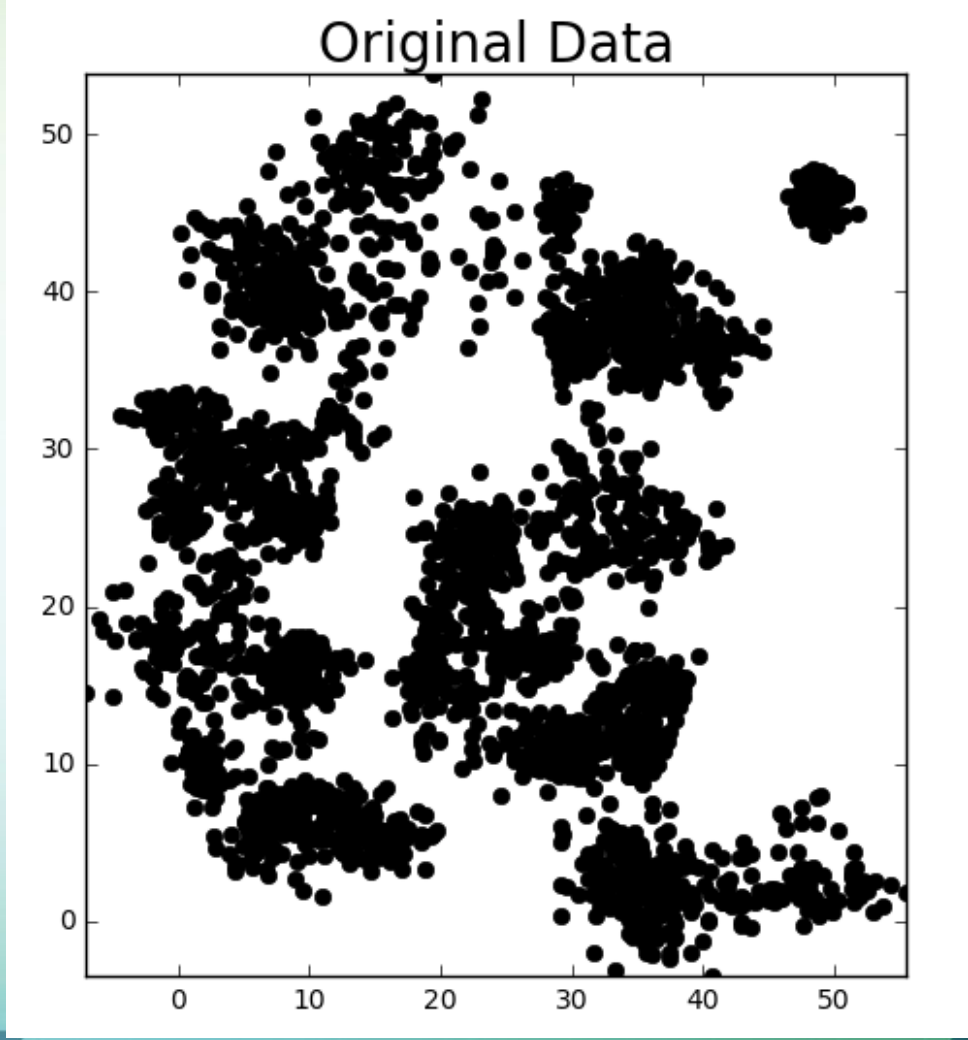
- Analysis of critical interconnections and related cells.
- Critical index is the presence of a single via vs. redundancy vias.



Thank you for your attention.

Background - Clustering

- Machine Learning algorithm of clustering is the action of grouping objects (or data) in the same group, called a cluster.
- Objects (or data) in the same group are more similar to each other compared to other clusters.
- Focus on DBSCAN, Density-Based spatial clustering of application with noise.
- It is a density-based clustering algorithm. Given a set of points, it groups together closely packed points (points with many nearby neighbours), highlighting outliers in the low-density region.



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