SWTEST

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2022 CONFERENCE

Novel reverse engineering way of fine pitch pre-bump probe head development

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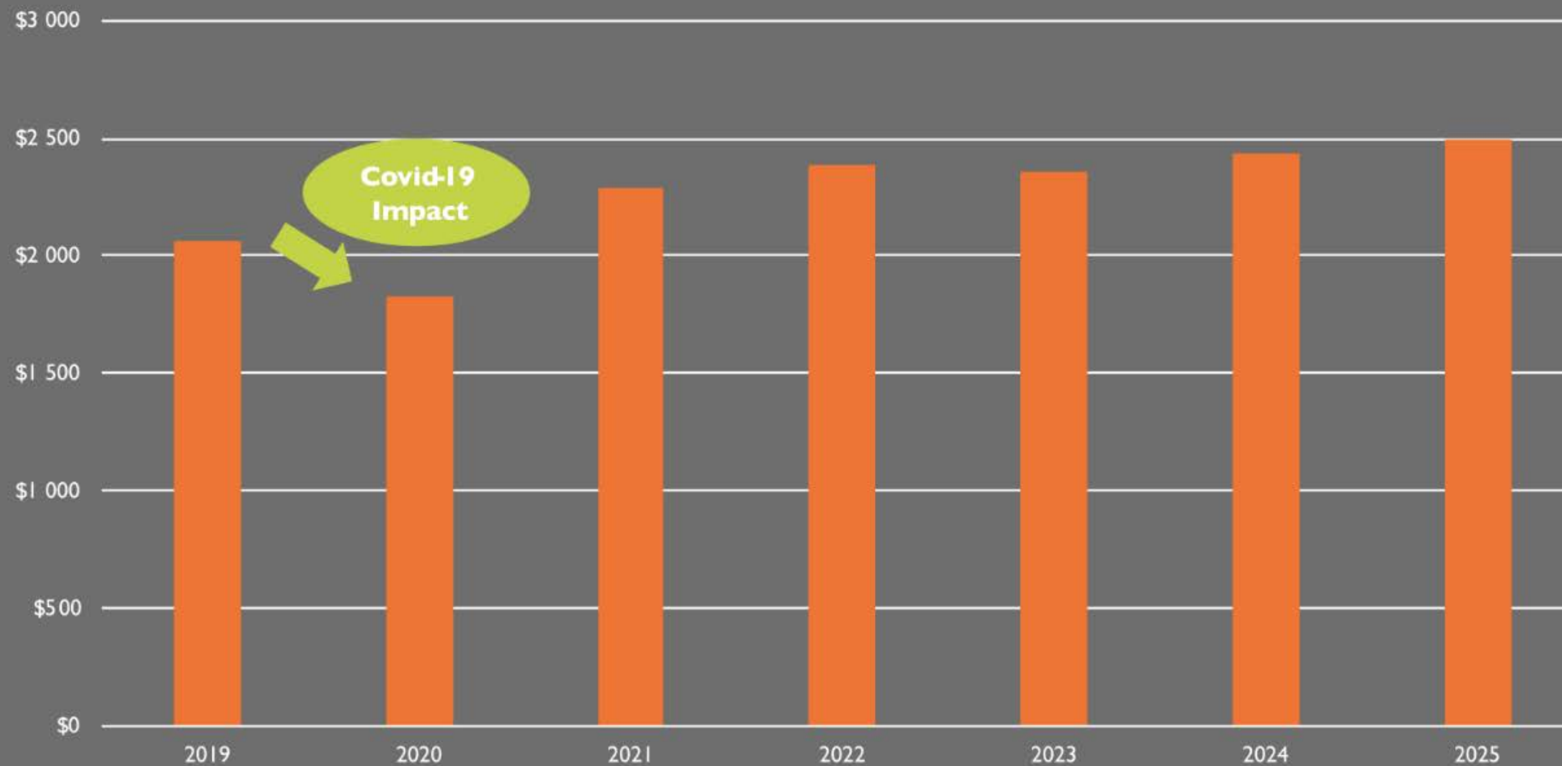
Overview

- Introduction
- Background
- Expected outcome and goals
- Proposed solution
- Design Consideration
- Challenges
- Experimental data in GLOBALFOUNDRIES
- Conclusion and further works

What’s WLP

- **WLP = Wafer Level packaging**
- **Fan-In WLP** are formed on the dies while they are still on the uncut wafer. The final packaged device is the same size as the die itself. singulation of the device occurs after the device is fully packaged.
- Fan-Out WLP starts with the reconstitution of individual dies to an artificial molded wafer. The molded reconstituted wafer forms a new base to apply a batch process that features build-up and metallization constructions

Trend of WLCSP/Fan-in WLP

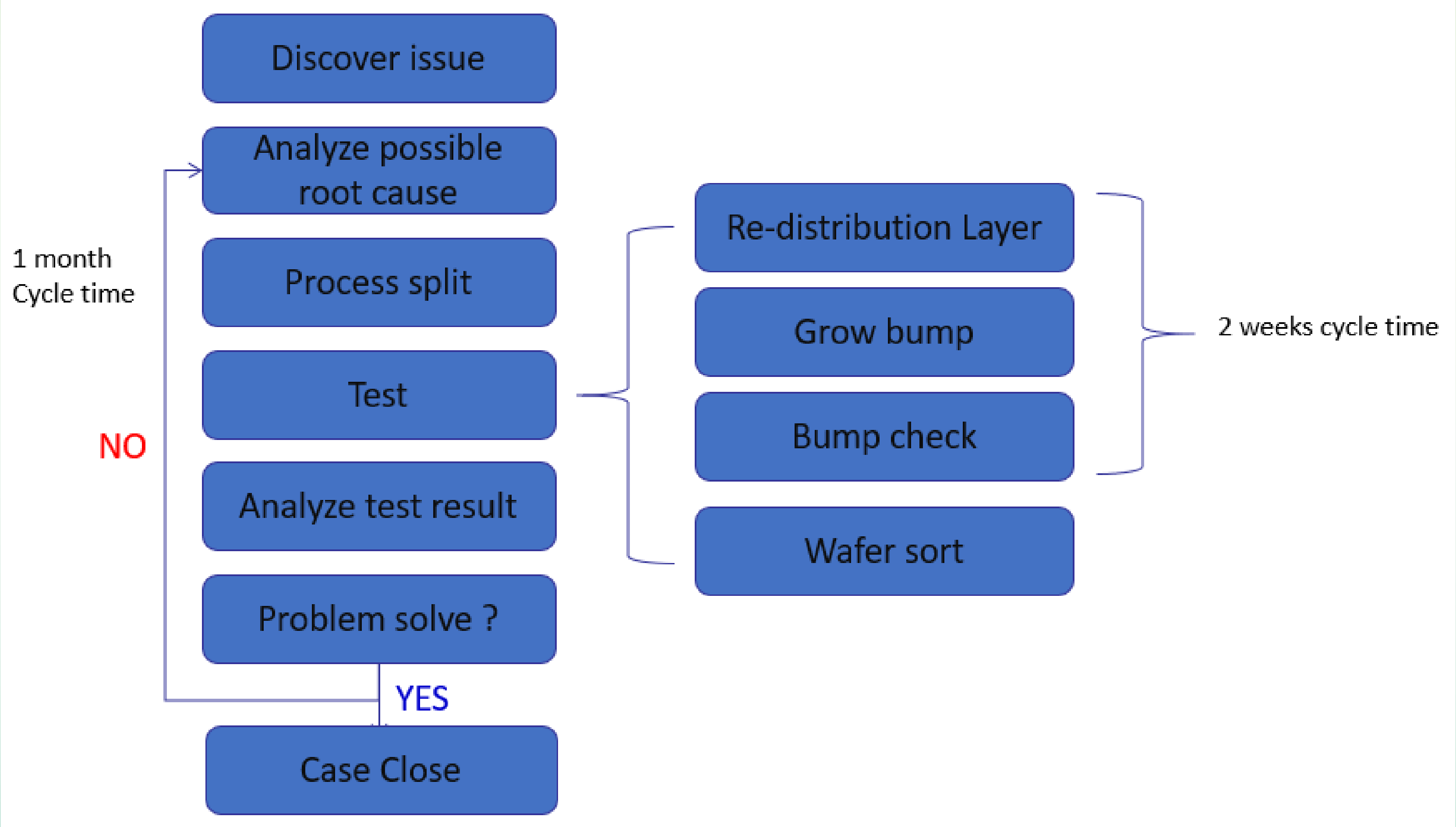


Pros and Cons for WLP

- Pros
  - Smaller chip size
  - Shorter electrical path
  - Lower cost

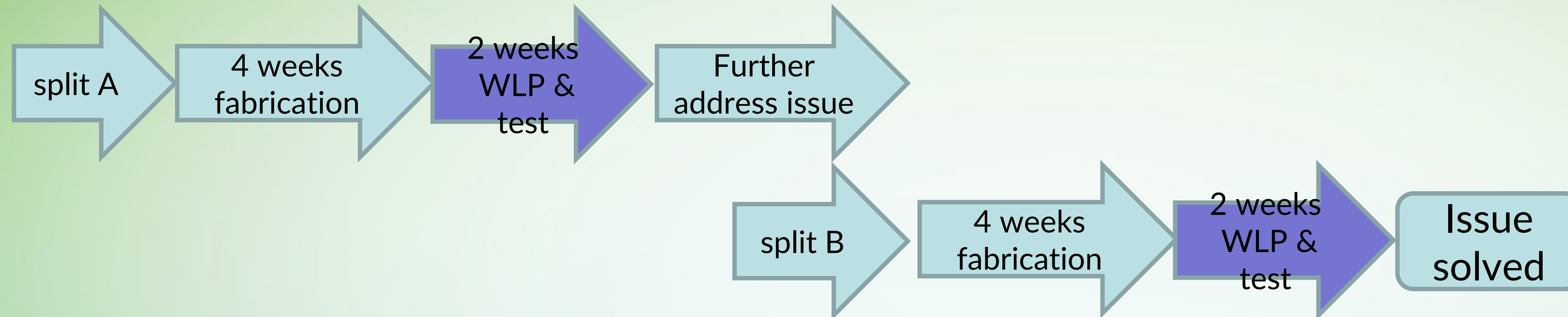
- Cons
  - Prolong process learning cycle
  - Extra cost for process monitoring

Role of test in process learning cycle



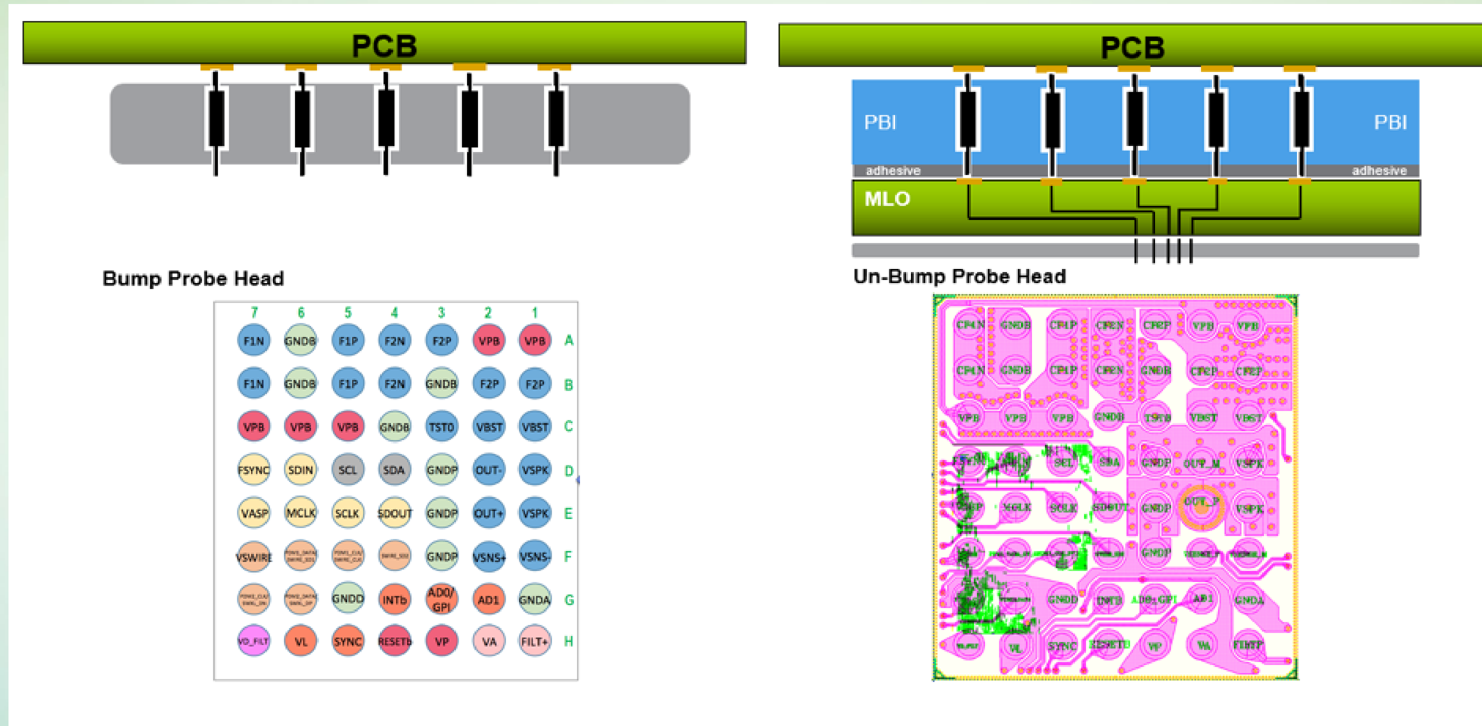
- Impact of cycle time for bumping and packaging route in yield learning workflow can be as much as 50% of fabrication time

Role of test in process learning cycle



- **In cases of multiple learning cycle is needed to resolve 1 process issue, the impact of cycle time induced by packaging and testing is accumulative.**
- **In above example, there are 4 weeks spend in WLP which is 50% of wafer fabrication time.**

Proposed solution



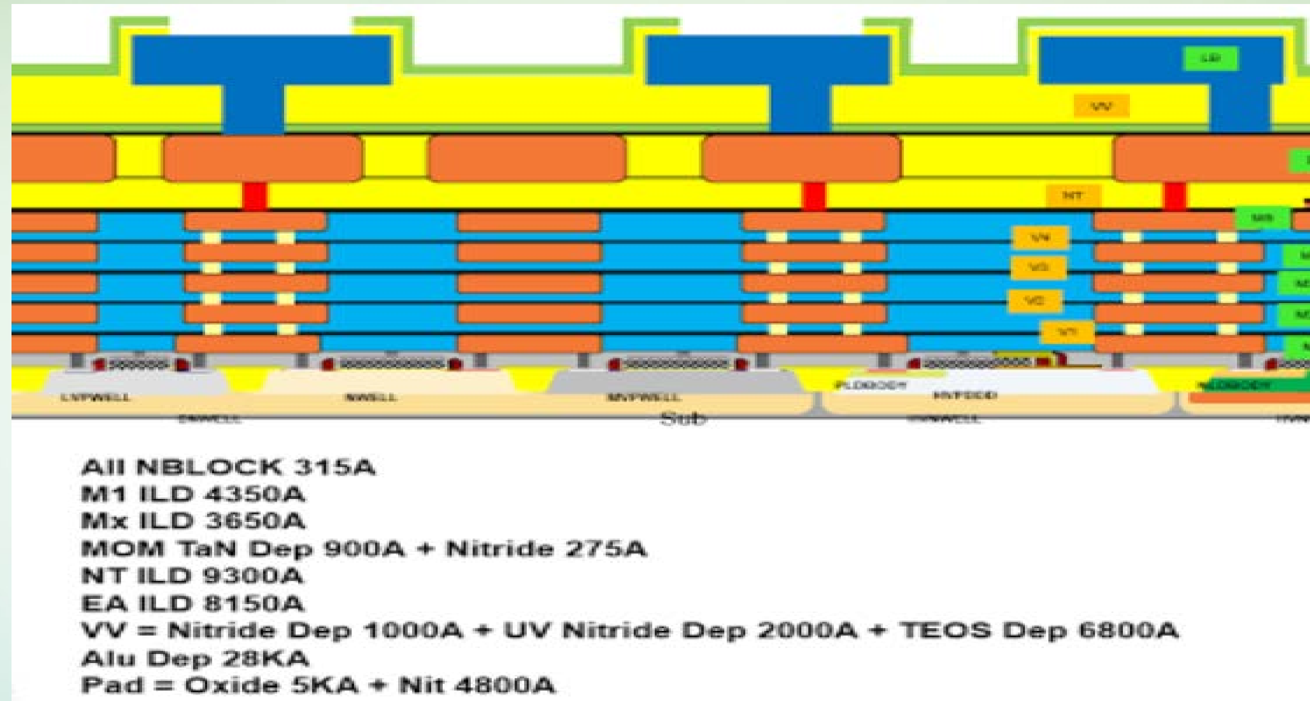
- Share same probe card PCB with production probe card
- Use same test program as production wafer sort

Design Consideration

	Bump	Pad
Number of Ball/pad	56	219
Pitch of Ball/pad	350um	50um
Pad Size	Solder Ball	35um round pad

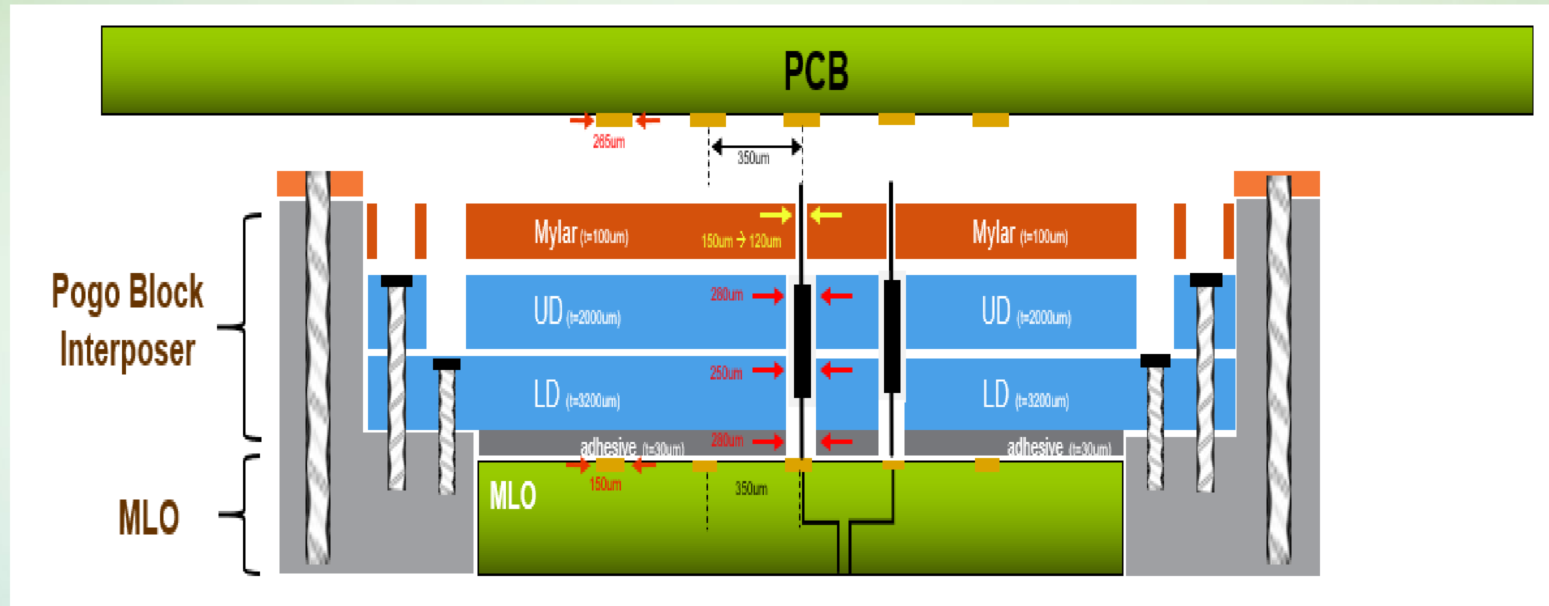
- **Remap of pins location**
  - Extract from Synopsys Avalon software with no change in tester channel assignment to ensure production test program is compatible
  - avoid sensitive underlying structure
  - Traditional Cobra VPC will not be able to meet this very small pitch requirement and special made MEMS 2mil probe pins. was used to replace original bump pin while ensuring the current carrying capability and gram force are still within required specification to avoid damage to wafer contact point and underlying device layers.

Design Consideration



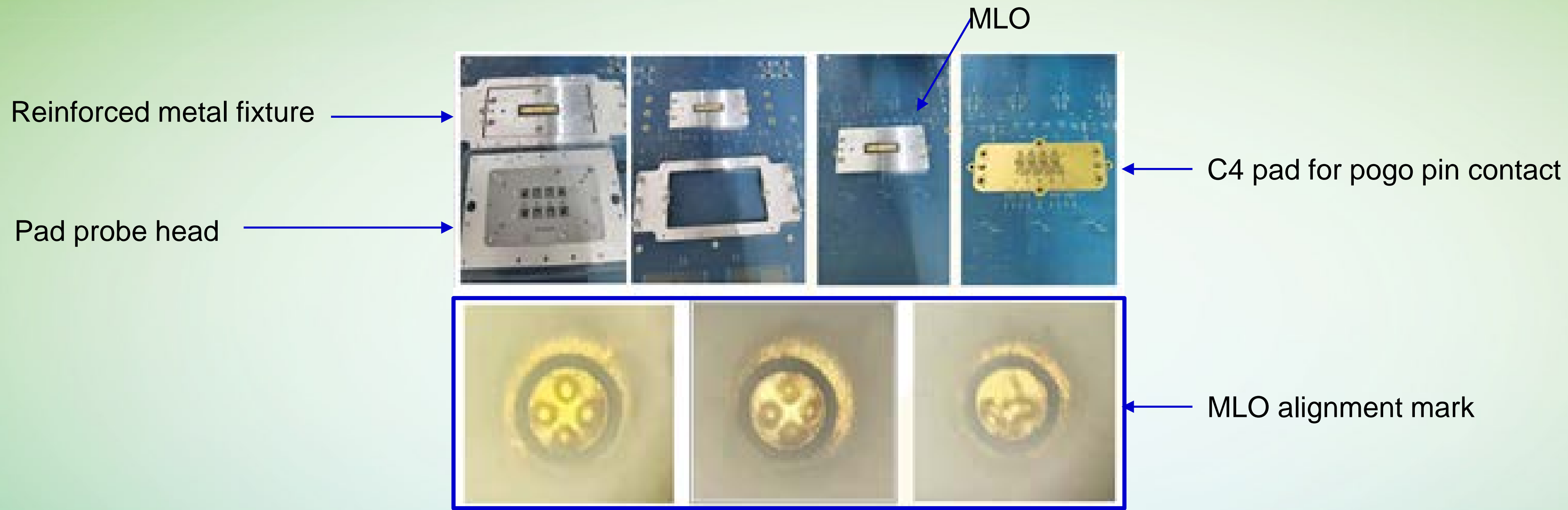
- **Foundry process information was studied for optimal probe settings**
  - Process illustration shows minimal risk of damaging sensitive electrical structure under the contact points.
  - Double touch down strategy with ~35um OD shows robust contact with minimal continuity test failure.

Design Consideration



- **PBI redistribution layer for rerouting PCB contact points to new locations**
  - MLO Layer to to reroute electrical signal overcome challenges that bump, and pre-bump wafer testing requires different number and position of contact points while keeping the pre-bump probe head compatible to existing probe card PCB.
  - Reinforced metal fixture designed to hold the multi-layer probe head.
  - Openings in Mylar/UD/LD/Adhesive layer optimized in width and shape to give a reliable housing of the pogo pins.

Design Consideration



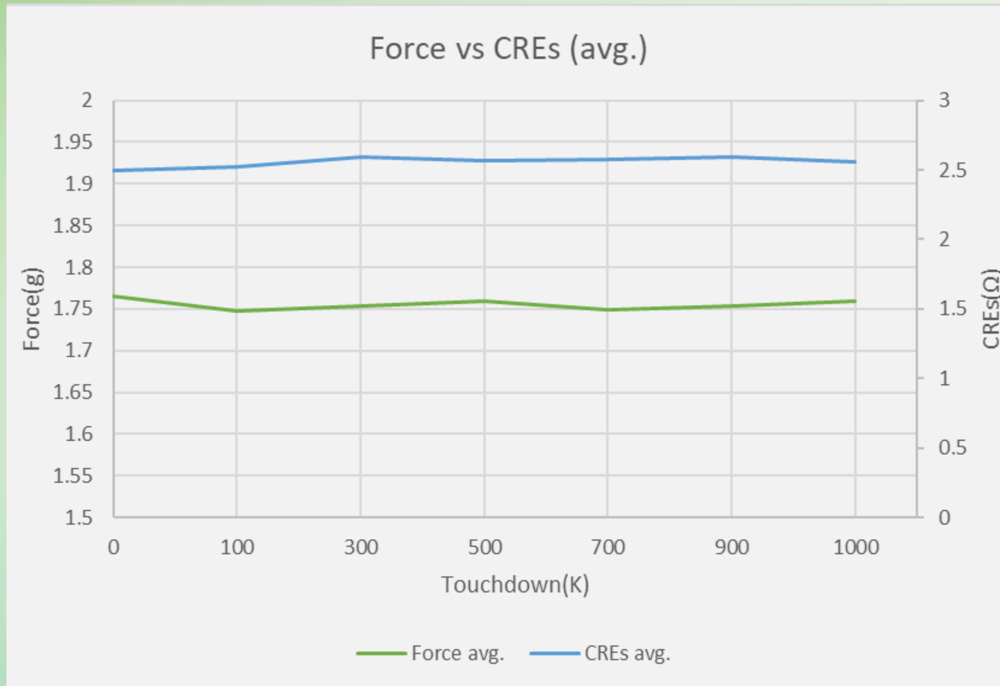
- **User friendly housing mechanism and specially placed visual guide holes to facilitate easy probe head swap**
  - Reinforced metal housing to hold the multi layer probe head.
  - Balanced and symmetrical screws with optimal torque force to ensure planarity and good contact between probe card PCB and pogo pins.
  - Visual guide holes at critical position allow user to check and confirm alignment and avoid contact issue due to mechanical allowance.
  - User can swap test head flexibility with minimal training to test both bump and un-bump wafer with a single probe card.

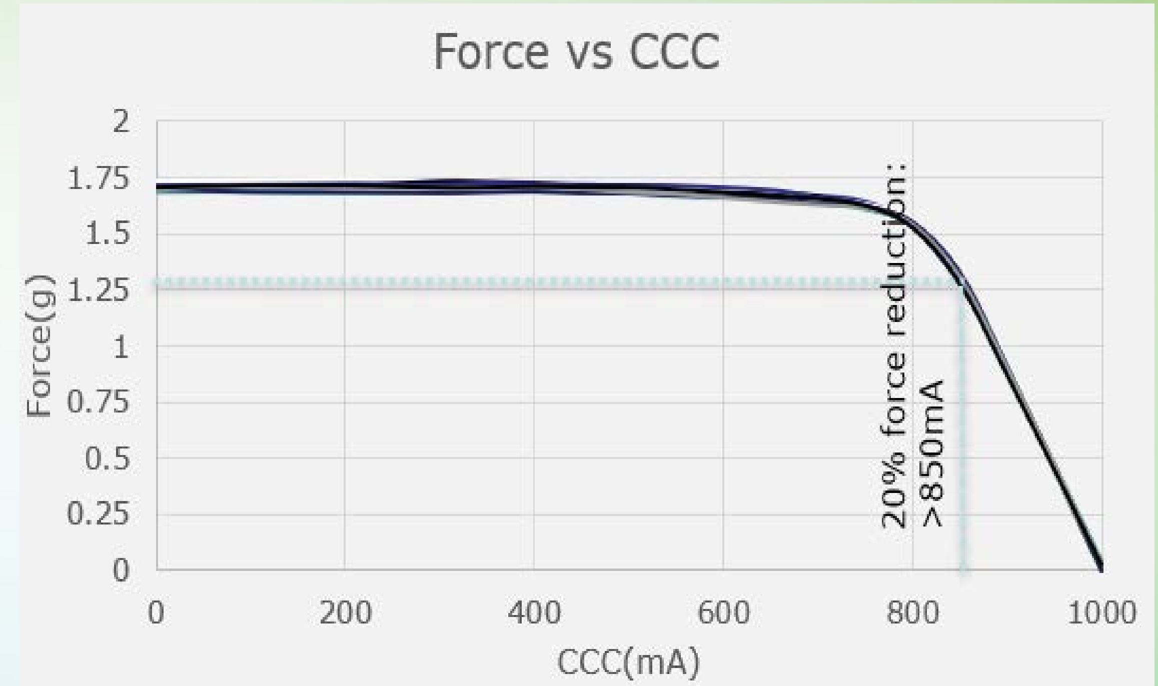
MEMS Pin Used

- **STAr-Prima SP65 & SP45**

Item No.	Needle Type	Spec	
		SP45	SP65
1	Needle Physical Length(um)	<5000um	<6000um
2	RDC(Total, mohm) @ 1MHz GS type (Simu.)	<350mohm	<300mohm
3	Pitch	≧45um	≧65um
4	CRs(mohm, CRs vs. OD 1~5mils)	<100mohm	<100mohm
5	Lifetime(Touchdown)	>1,500,000 (ref.)	>2,000,000 (ref.)
6	BCF(Balance Contact Force, g/mil, 1~5mils)	<1.35g(Customize)	<1.85g(Customize)
7	BCF Deviation	<2.5%	<1.5%
8	CCC	≦550mA	≦850mA
9	Operating Temp.(C)	-40~105 (opt. 125)	-40~125 (opt. 150)
10	Probe Needle Insulation Coating	Yes	Yes
11	Probe Needle Tail Au Coating Thickness	0.25um(opt.)	0.25um(opt.)
12	Alignment accuracy(X/Y)	<+/- 5um	<+/- 5um
13	Probe Tip Diameter	≦ 8um	≦ 10um
14	Usable Probe Length(mils)	250~325um(by case)	300~375um(by case)
15	Probe Type	Flat > Bump , Point > Pad	

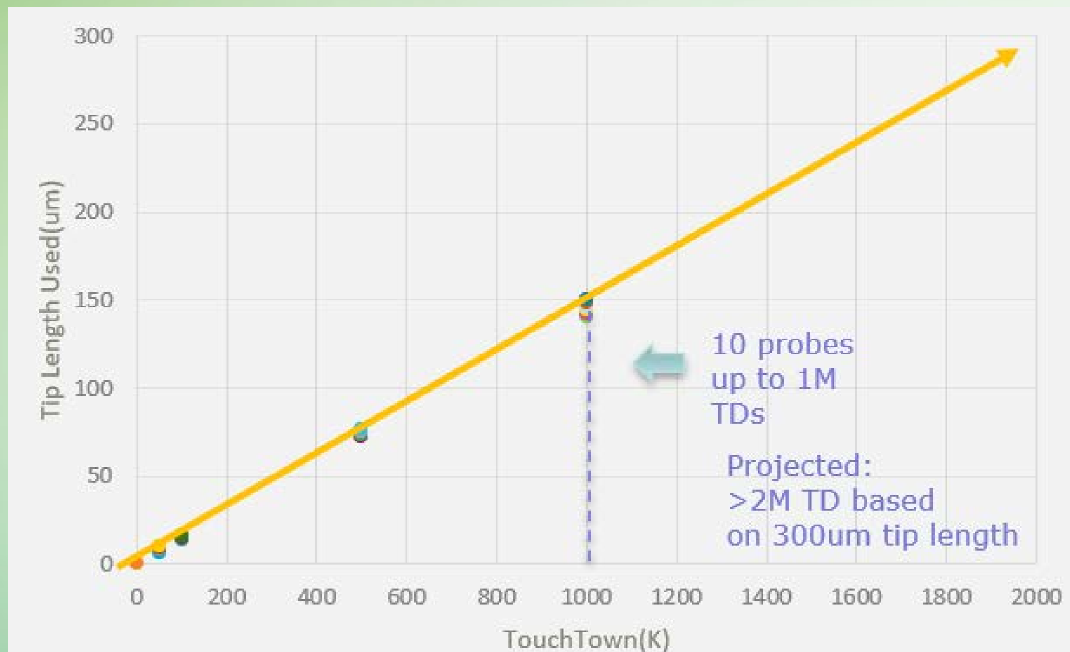
MEMS Pin Specification

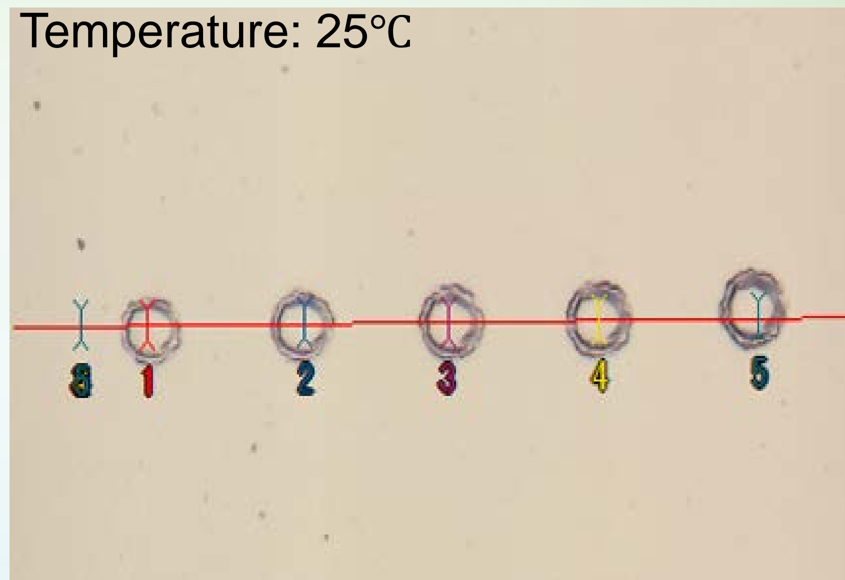




- **SP65 specification highlights**
  - Reliable contact force against # of TD
  - Consistence CRES against # of TD
  - CCC up to 850mA

MEMS Pin Specification

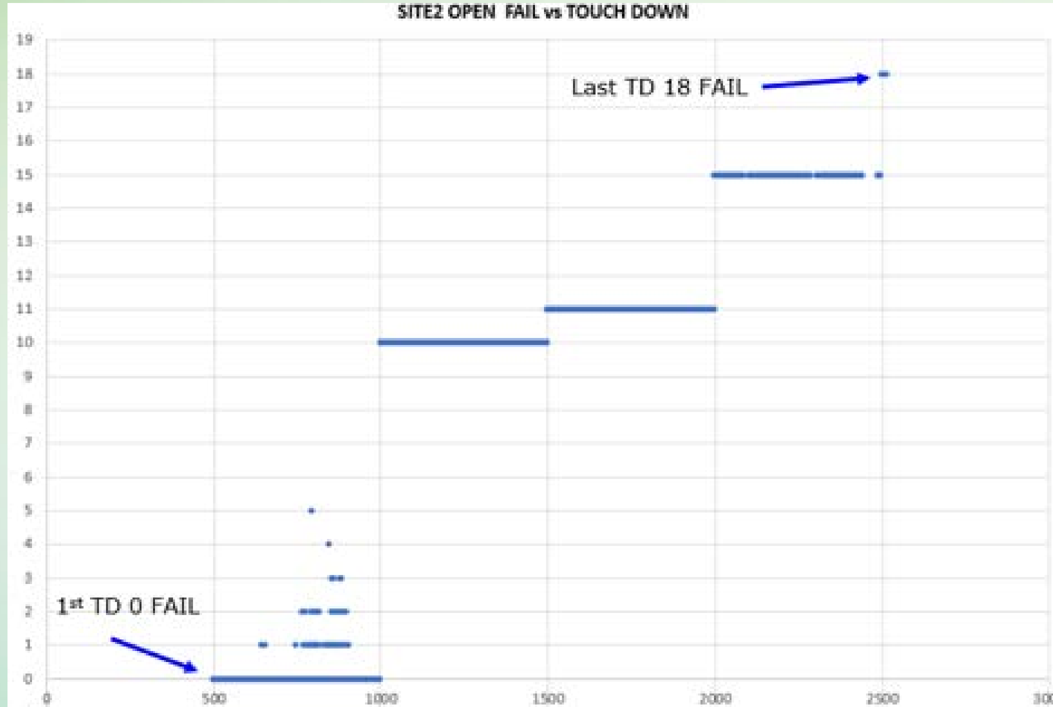


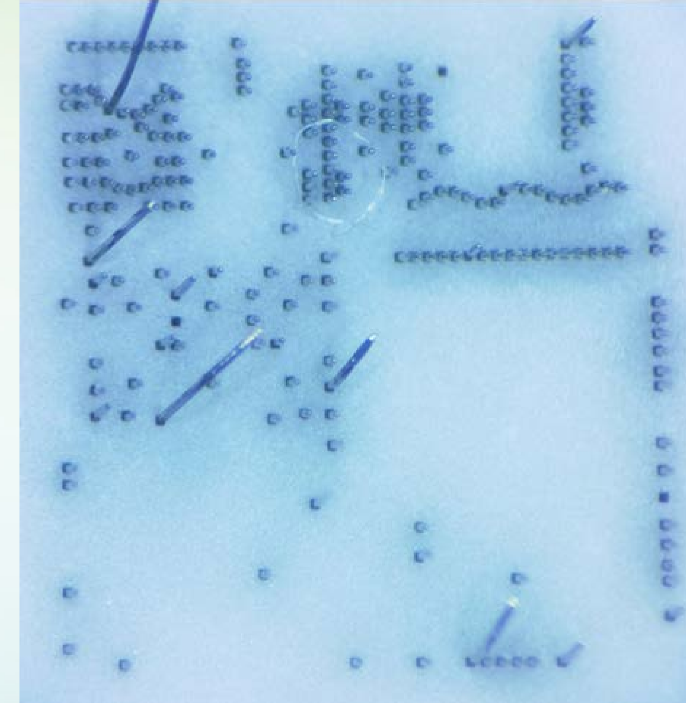


	OD (um)	Depth (um)
1	0	0.210
2	25	0.268
3	50	0.288
4	75	0.320
5	100	0.328

- **SP65 specification highlights**
  - Lifetime up to 2mil
  - Small probe mark with min probe depth

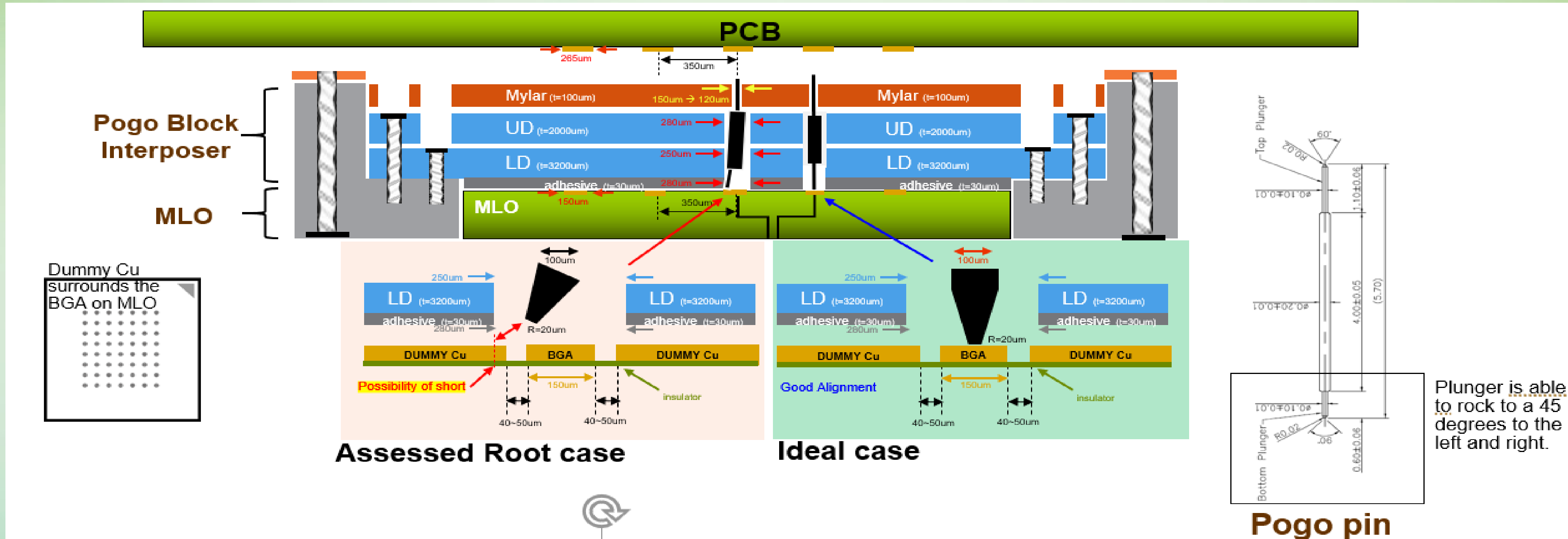
Challenges & reliability enhancement





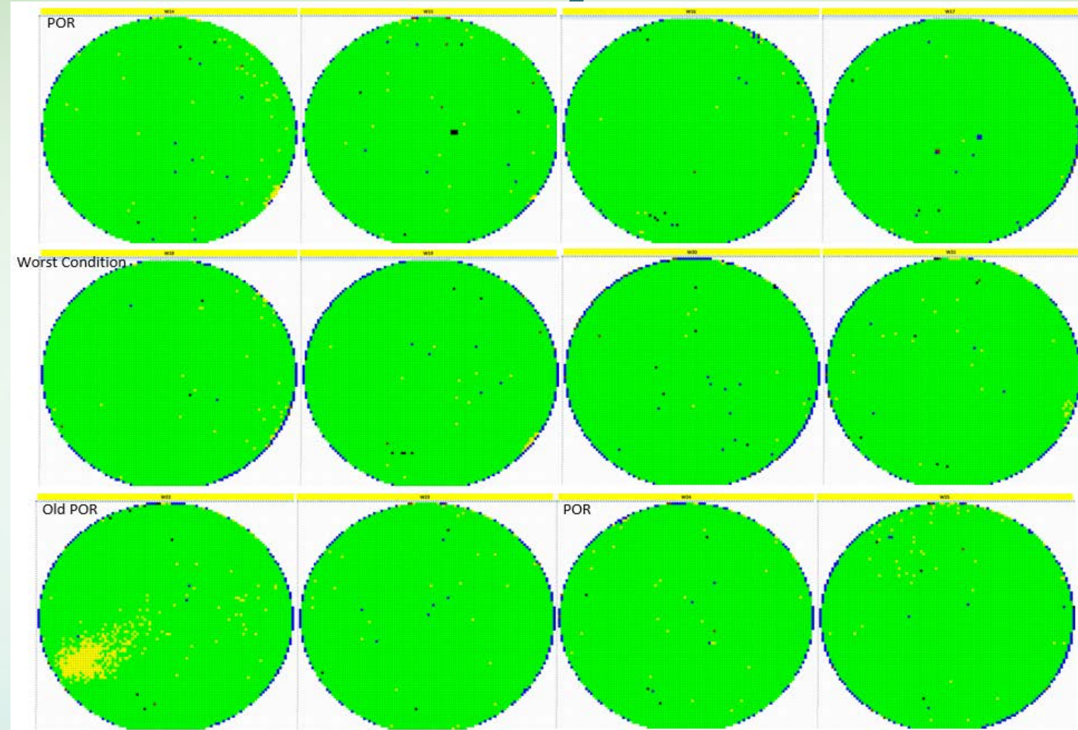
- **Reliability Issue Background**
  - To assess the reliability of the probe head, a wafer with 7800 dies was set to run in auto sort In the middle of sort testing, it was observed that multiple pins start to fail continuity open and short test. While visual inspection using prober microscope confirmed some pins were deformed after repeated touch down

Challenges & reliability enhancement



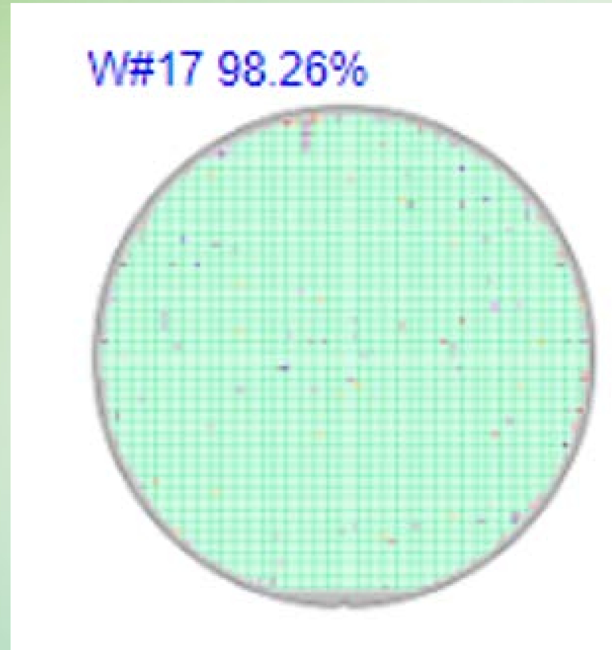
- **Root Cause Isolation**
  - To isolate the root cause as well as to scope for potential area of optimization in design the probe head was dismantled layers by layers.
  - It was found that the main reason for open is due to UD/LD layer not holding the pin securely and main reason for short is plunger of pogo bending to touch the CU layer after repeated touch down.
  - To address these issues a re-build of the probe head using tighter opening in mylar/UD and LD layer as well as additional protective etch to widen the gap between CU and BGA layer

Challenges & reliability enhancement

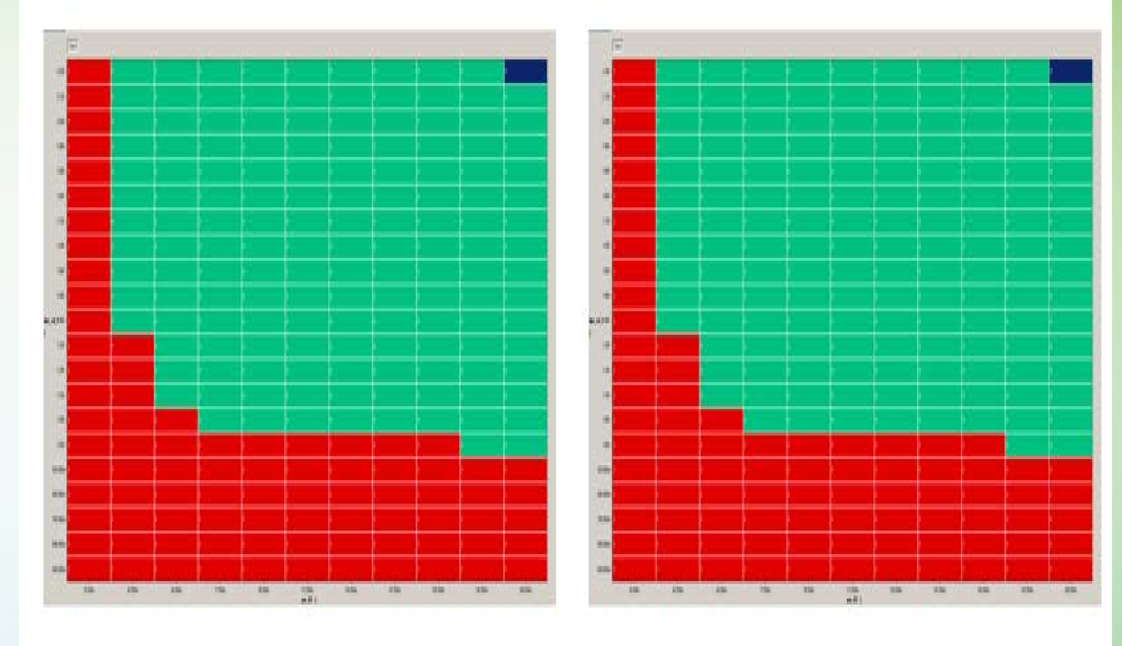


- **Test Result After Rectification**
  - The optimized probe head was subjected to 25 wafers testing totalling > fifty thousand touchdowns in an attempt of reliability and functionality assessment. The yield result is inline with expectation with no more open and short failure observed.
  - Yield is comparable to bump wafer. Probe head endure all wafers testing with no issue observed after the design enhancement

Success story – In Fab test enablement

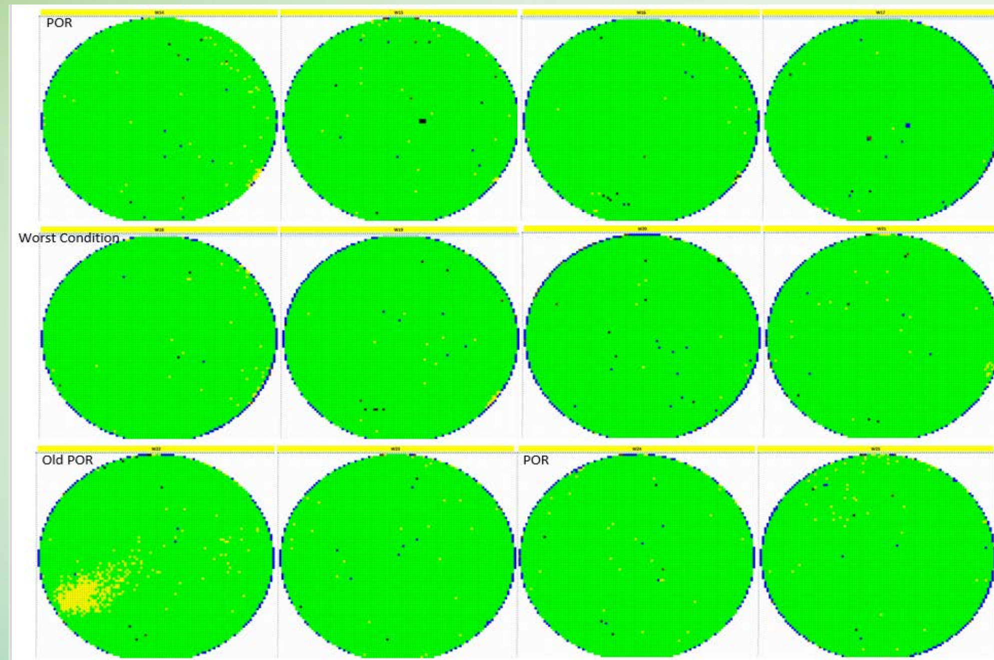


Show	Bin Group	Color
✔	ADC/MON	
✔	Amp	
✔	Boost	
✔	Conti	
✔	DVS	
✔	Digital	
✔	Leakage	
✔	OTP/Trim	
✔	Others	
✔	Pass	
✔	Power	
✔	PowerUp	
✔	Scan	



- **In Fab unbump test enablement**
  - Unbump probe head validated to have comparable yield and bin distribution against bump wafer production sort result.
  - Shmoo on speed critical test show identical performance and passing window.
  - Fab can perform in-house test and device characterization without going through the costly and time-consuming bumping+test house route

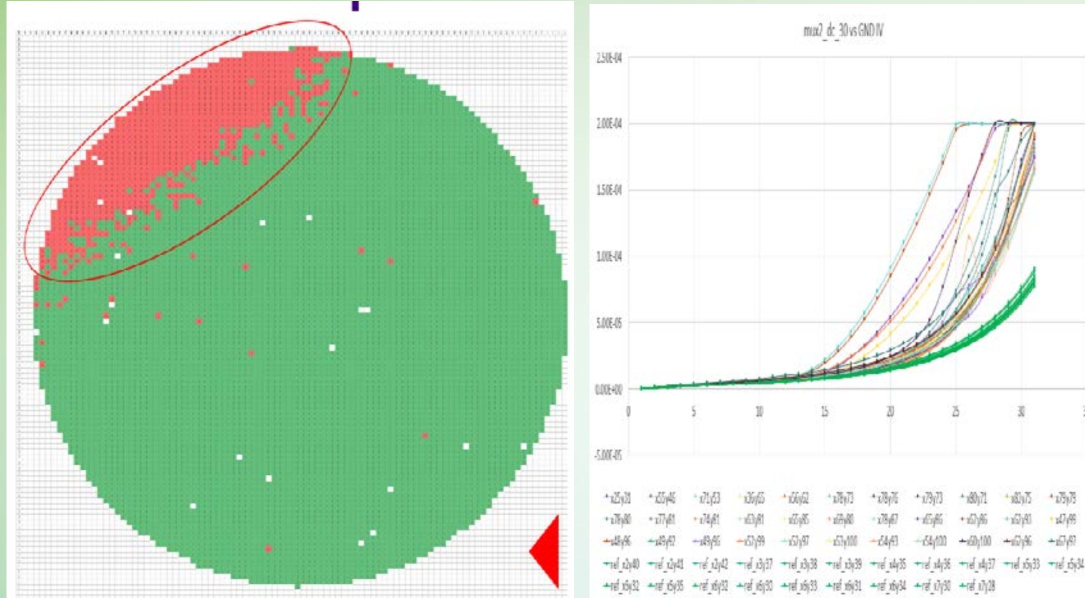
Success story – Fab process optimization support

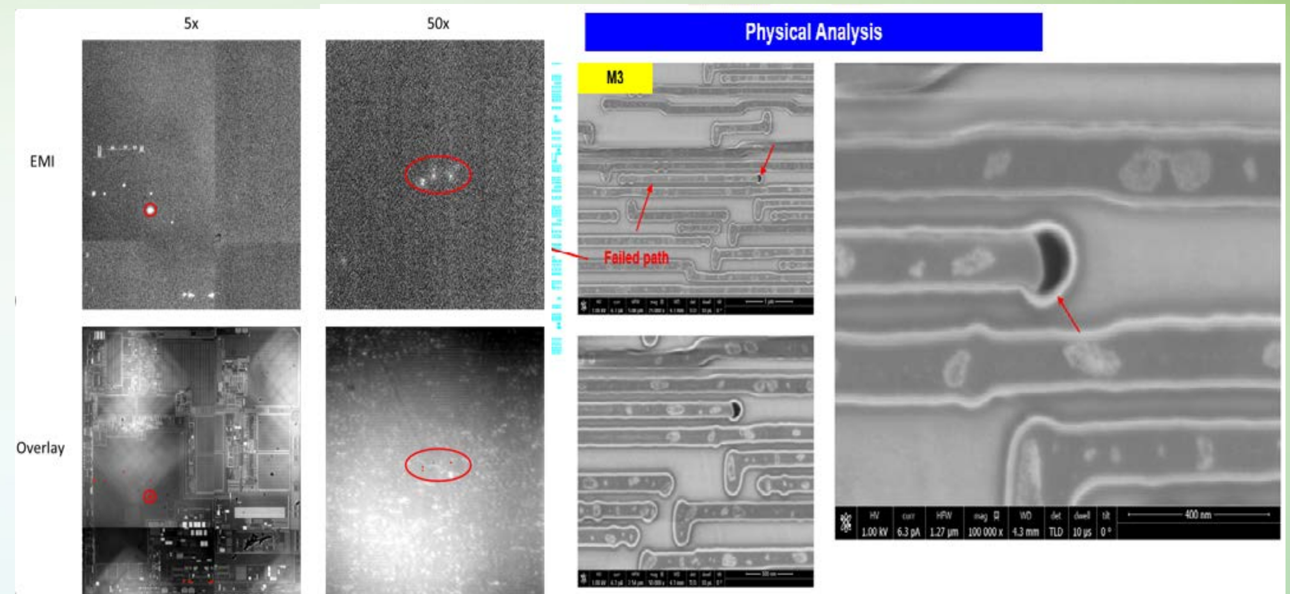


Split stage:M3 & M4: Liner & ECP	Module B Exposure vs Process Split	6 hours Foup open & 48 hrs Qtime from Liner to ECP									POR Envt Condition		
		14	15	16	17	18	19	20	21	22	23	24	25
Cu seed thk (ModuleB)	500 A (Old POR)							X	X	X			
	600 A (POR)	X	X	X	X	X	X				X	X	X
Environment & Q time	**(6hours exposure ModuleB at night): Foup open**	X	X	X	X	X	X	X	X	X			
	POR										X	X	X
	Q time 48 hrs (Liner to ECP)	X	X	X	X	X	X	X	X	X			
ECP intinal step (FECP707)	0.65V/0.5sec			X			X	X			X		
	1.00V/0.5sec(POR)	X	X									X	
	1.20V/0.5sec (Old POR)				X	X			X	X			X
ECP 1'st step	4.5A (Old POR)		X	X		X				X			
	6.75A(POR)	X			X		X	X	X		X	X	X
Comment		**POR**				**Worst Condition**				Old POR		POR	
Yield		98.04	98.18	97.73	97.85	97.47	97.45	97.31	97.69	93.35	97.95	97.92	97.07
14213_Power		0.94	1.02	1.28	1.33	1.68	1.74	2.09	1.30	1.29	1.38	1.42	1.97
5000_Scan		0.49	0.19	0.26	0.08	0.32	0.26	0.12	0.34	3.05	0.22	0.24	0.31
5005_Scan		0.22	0.18	0.10	0.03	0.21	0.09	0.03	0.14	1.46	0.21	0.15	0.37
14211_Power		0.03	0.12	0.22	0.31	0.18	0.21	0.06	0.27	0.24	0.09	0.01	0.04
14020_Power		0.08	0.08	0.13	0.15	0.03	0.06	0.05	0.05	0.04	0.06	0.08	0.05
2017_CONT		0.04	0.06	0.08	0.03	0.01	0.09	0.03	0.05	0.05	0.04	0.04	0.03
3299_Leakage		0.05	0.06	0.03	0.06	0.01	0.06	0.01	0.03	0.01	0.05	0.05	0.03
3021_Leakage		0.00	0.00	0.00	0.06	0.04	0.01	0.12	0.04	0.03	0.00	0.01	0.01
2015_CONT		0.00	0.00	0.13	0.03	0.01	0.00	0.05	0.03	0.05	0.00	0.00	0.00
5010_Scan		0.06	0.01	0.00	0.01	0.00	0.00	0.00	0.01	0.15	0.00	0.01	0.00

- **In Fab process optimization**
  - Optimal CU seed thickness and ECP initial step voltage identified via DOE. Yield gain of ~4.5% using new recipe against original POR recipe.
  - Significant time and cost impact as study can now proceed in Fab at pad level avoiding additional step of bumping and sending wafer to test house.

Success story – Enablement of in Fab EFA





- **Root cause finding for high scan yield loss**
  - In-house sorting on un-bump wafer successfully reproduce the scan failure reported.
  - Characterization sort shows failure is related to high leakage on one of the device power pad.
  - EFA and PFA confirmed root cause due to M3/V3 void.
  - Fast turn around time and significant cost saving as Fab can do one stage analysis now (Test+Charz+EFA+PFA) without bumping and sending wafer to test house.

Conclusion & Future improvements

- **Conclusion**
  - This paper has demonstrated the design and validation of a user interchangeable probe head solution that will enable earlier stage pre-bump wafer testing while using existing production bump wafer test hardware and program
  - Such method will enable pure play foundries to enable in-house test solution for process improvement without support from customer and with minimal lead time and cost.
  - Volume wafers sorting confirm that un-bump probe head is production ready and is comparable to original bump probe head in terms of functionality and reliability.

- **Future improvements**
  - New technology future stack layer probe head will be copper layer free while maintaining the same rigidity.

Acknowledgment

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  - Yuan-Dong Huang
  - Wei Leong Toh

Thank you !