SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

ADVANCES IN VERTICAL PROBING FOR HIGH-SPEED DIGITAL TEST AT WAFER SORT

FormFactor™

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FormFactor

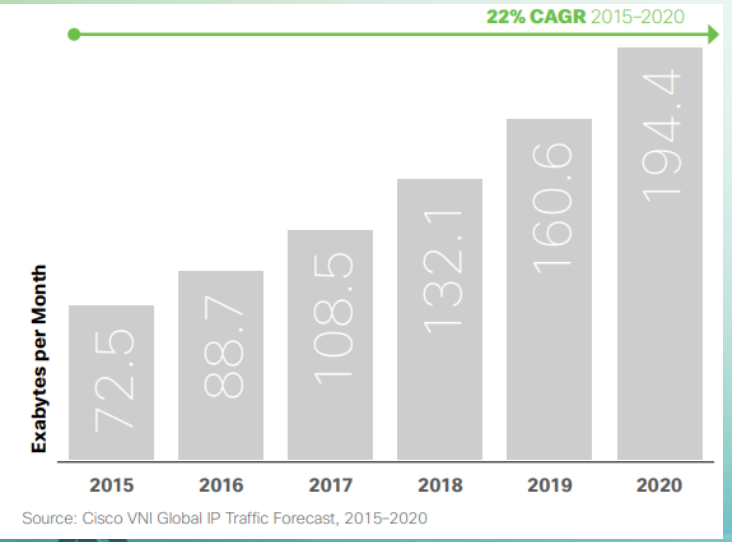
June 5 - 8, 2022

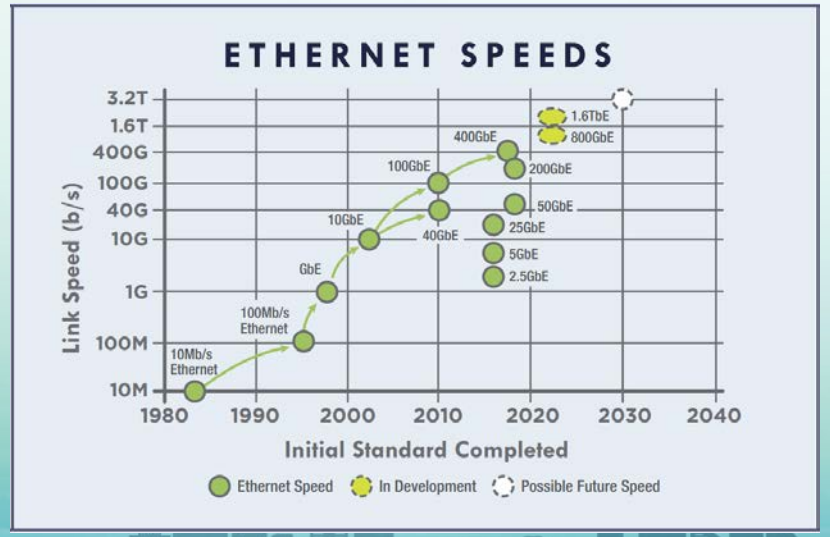
Agenda

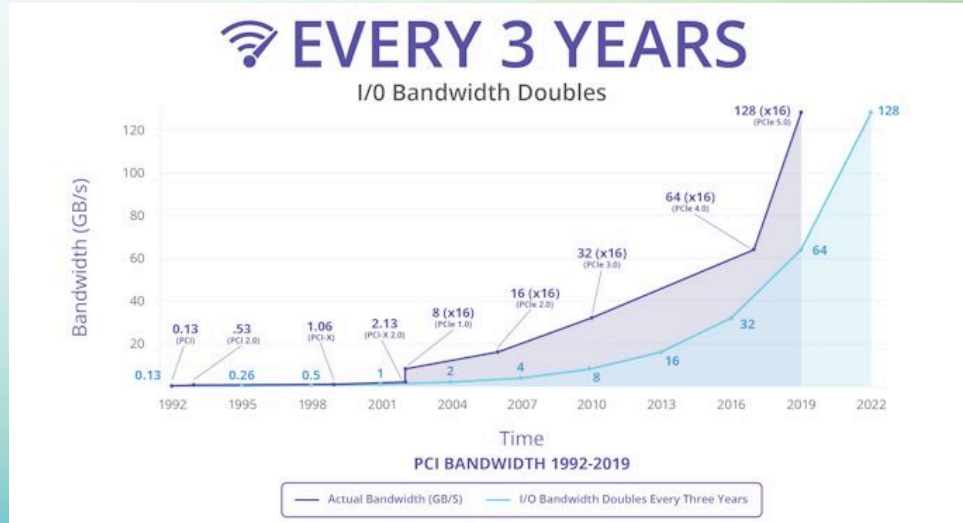
- Digital Trends and Status Quo of Wafer Test
- New High-Speed Digital Test Requirements
- New FFI High-Speed Wafer Test Solutions
- Conclusion

Digital Speeds Following Moore's Law

- **Global data usage growing exponentially with a 22% CAGR**
- **To manage this data, the speed at which data can be moved must increase at a similar rate.**
  - Data rates must double every 2-3 years to keep up with usage

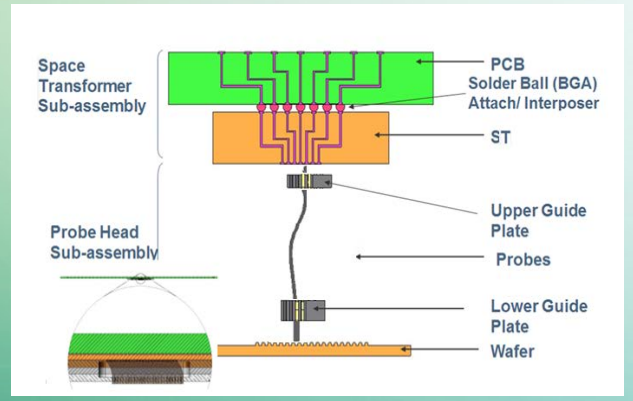


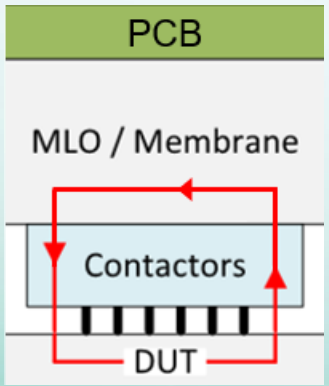




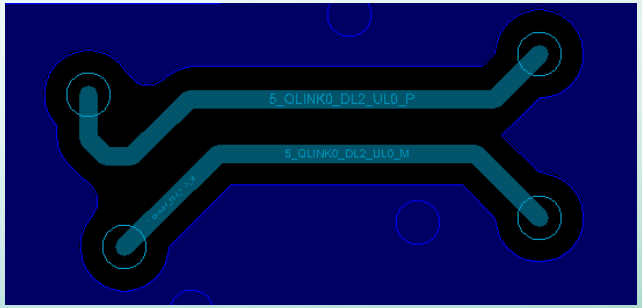
How is Digital Test Managed Today?

- **Digital Test traditionally consists of external loopbacks connecting the TX of a die to the RX of a die**
  - Essentially a form of self-test
  - Typical loopback length <15mm
- **Goal is to minimize loss**

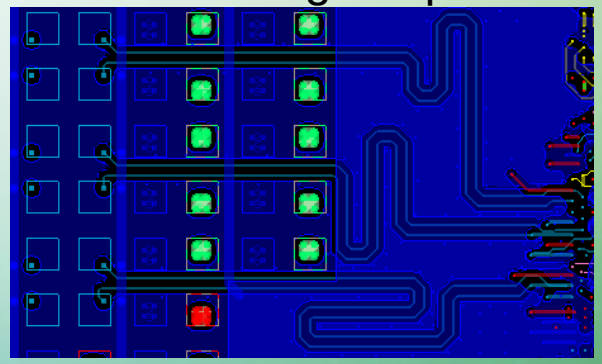




DC Loopback



DC-Blocking Loopback



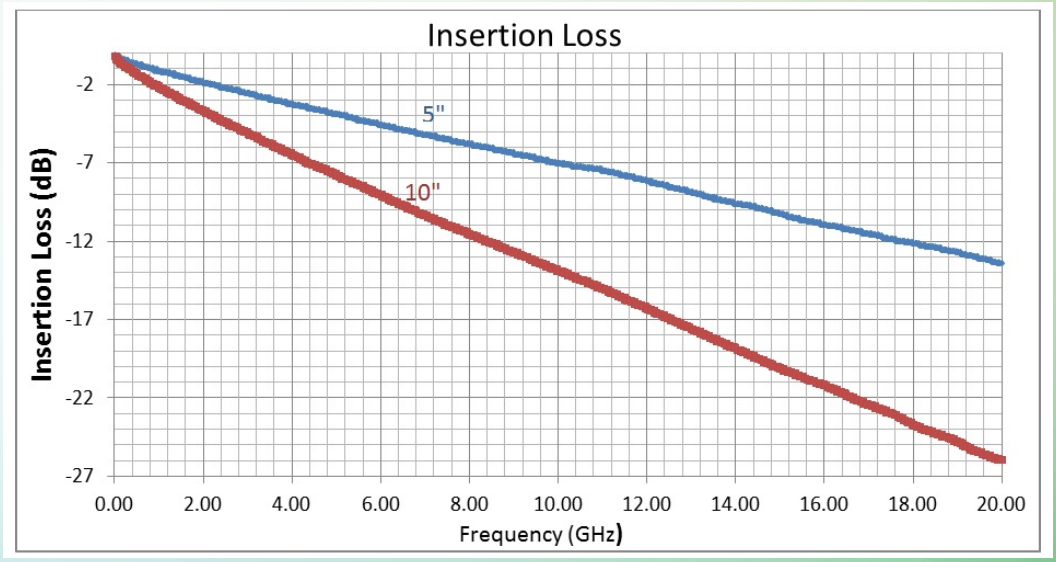
- **Will this test strategy continue to work as speeds increase?**

Impact of Data Rate Increase on Semiconductors

- Loss increases as speed increases
- Loss increases with path length

- How do we solve the challenge of increasing data rate without increasing loss?

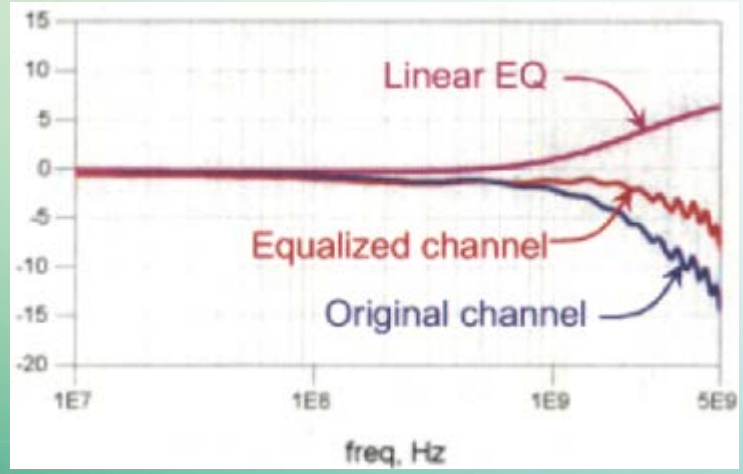
Microstrip Insertion Loss Comparison



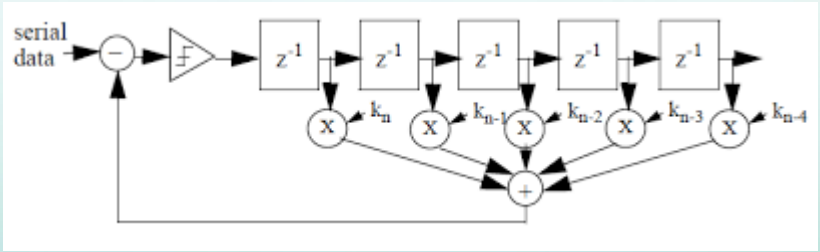
Countering Loss with Equalization

- Loss is countered using equalization and digital signal processing techniques
- Common Types of Equalization:

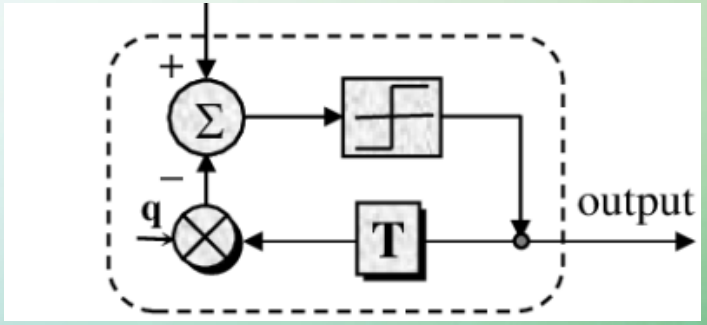
Continuous Time Linear Equalization (CTLE)



Feed-Forward Equalization (FFE)

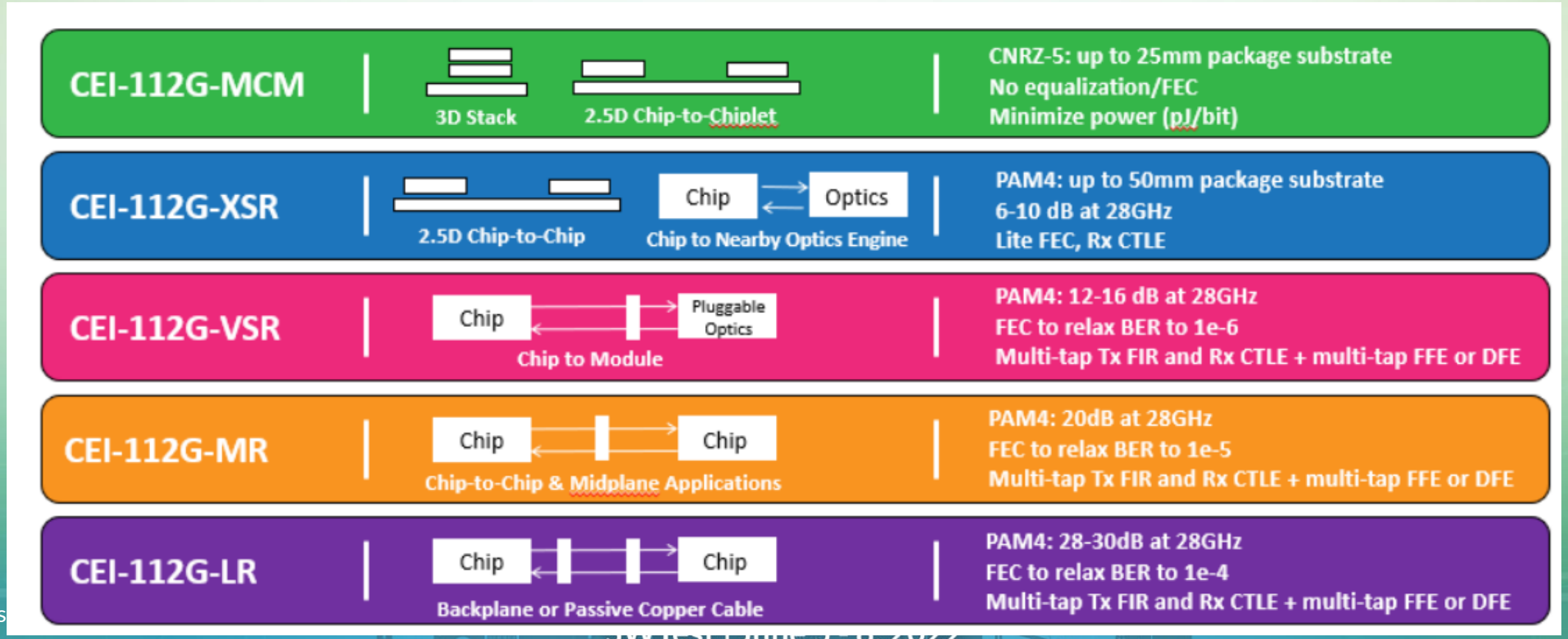


Decision Feedback Equalization (DFE)



How the End Module Impacts Loss

- Different module types lead to different loss budgets and require different equalization techniques



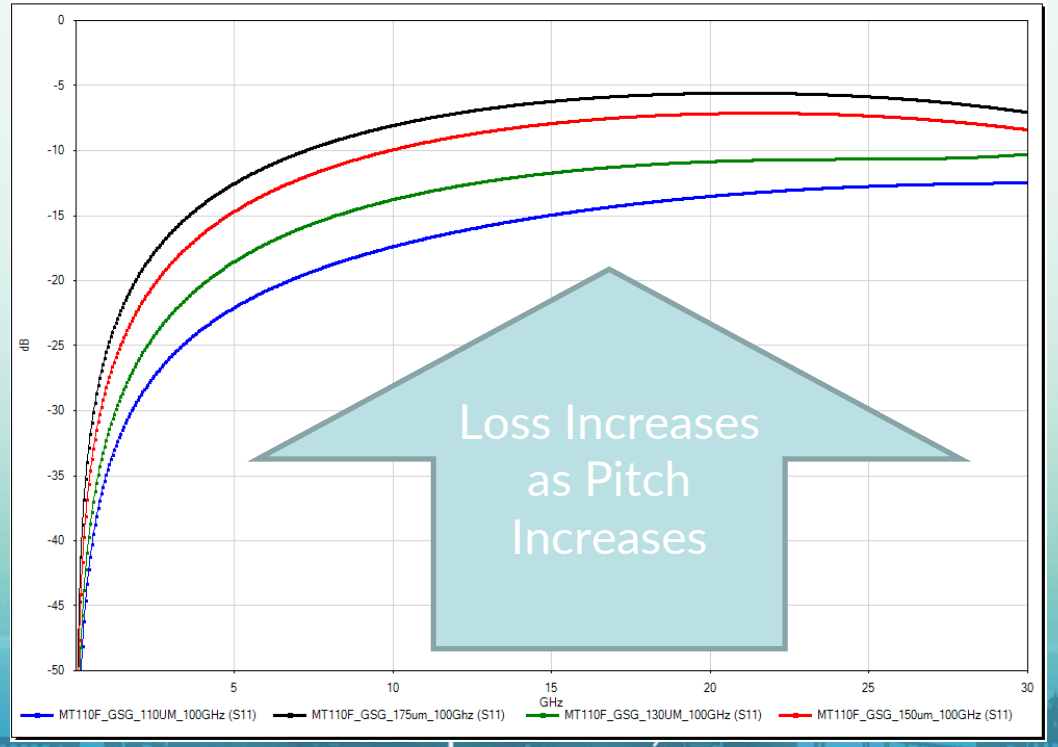
How Does Equalization Impact Wafer Test?

- **Challenges with Testing the Equalization and Digital Signal Processing:**
  - Challenge 1: Matching Impedance in the PH or contactor
  - Challenge 2: Matching Module Performance
  - Challenge 3: Verifying that Full Functional Test will Work

Challenge 1: Improving Return Loss

- Impedance is set by pitch and layout
- Wafer test needs to develop a robust, pitch independent solution

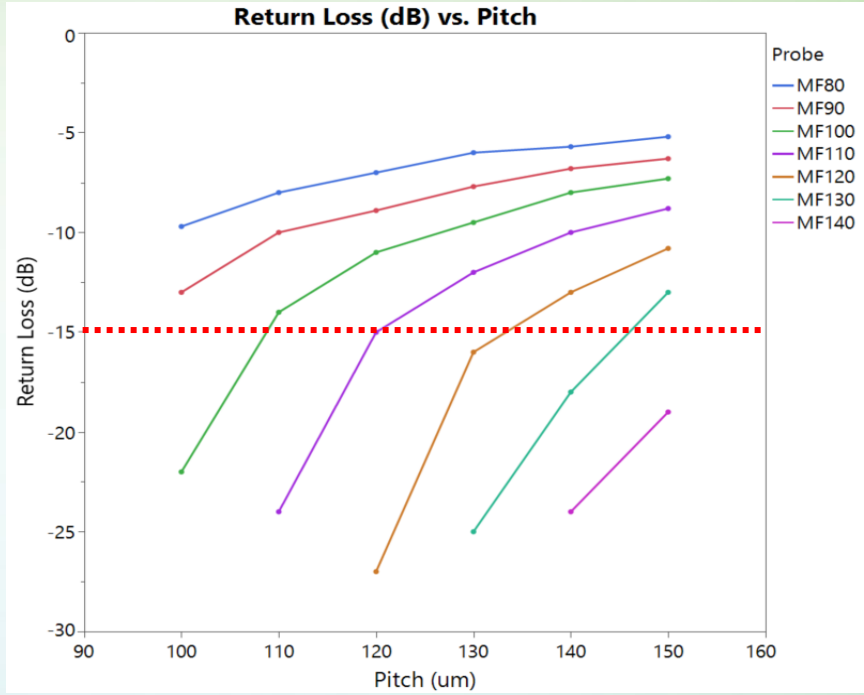
Return Loss Performance of MEMS Probes by Pitch



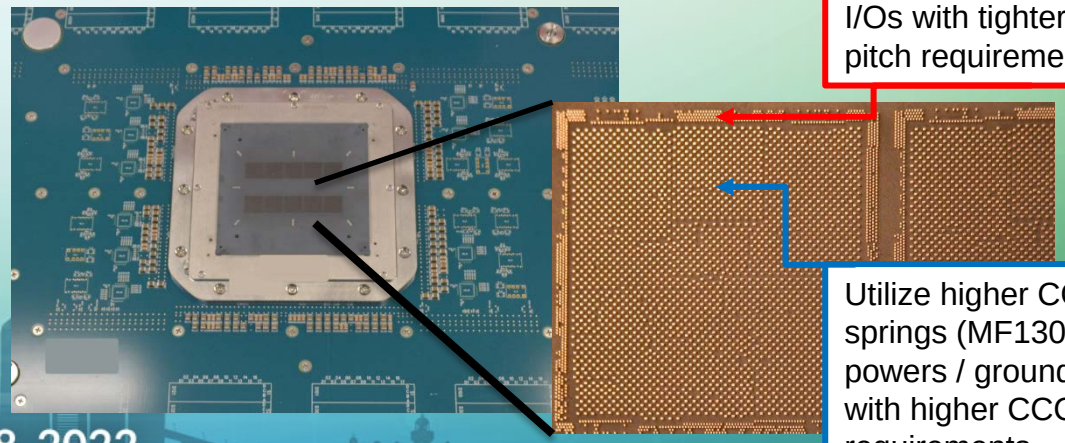
175um Pitch
150um Pitch
130um Pitch
110um Pitch

FFI Hybrid Probes for Optimized Return Loss

- **FFI Hybrid probes enables multiple probe types in the same probe head**
  - Traditionally used to maximize effective CCC
  - Now FFI supports hybrid probes that are tuned to match impedance at a particular pitch
  - Automated design and assembly processes ensures >99% First Pass Yield
- **FFI Hybrid Probes Shipping in HVM for several years**



FFI Hybrid enables <-15 dB Return Loss from <100um pitch to 150um pitch



Utilize tight pitch springs (MF80) for I/Os with tighter pitch requirements

Utilize higher CCC springs (MF130) for powers / grounds with higher CCC requirements

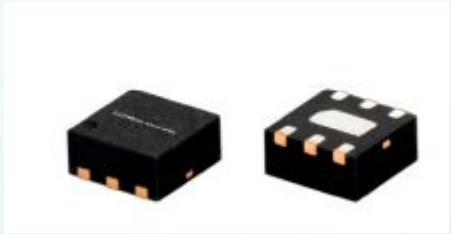
How Does Equalization Impact Wafer Test?

- **Testing the Equalization and Digital Signal Processing**
  - Challenge 1: Matching Impedance in the PH or contactor
    - Solution 1: Hybrid Probes for Matching Impedance
  - Challenge 2: Matching Module Performance
  - Challenge 3: Verifying that Full Functional Test will Work

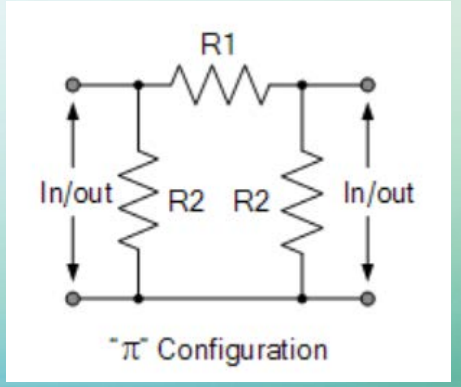
Challenge 2: Matching Module Loss

- **How can loss be added to a Probe Card?**
  - **Connectorized attenuators** ✗
    - Only matched to 50 ohms
    - Too large to fit more than a few on the PCB
    - Requires complex routing to get signals out of the MLO

  - **SMT Attenuators** ✗
    - Only matched to 50 ohms
    - Single-Ended format only
    - Long Lead Times

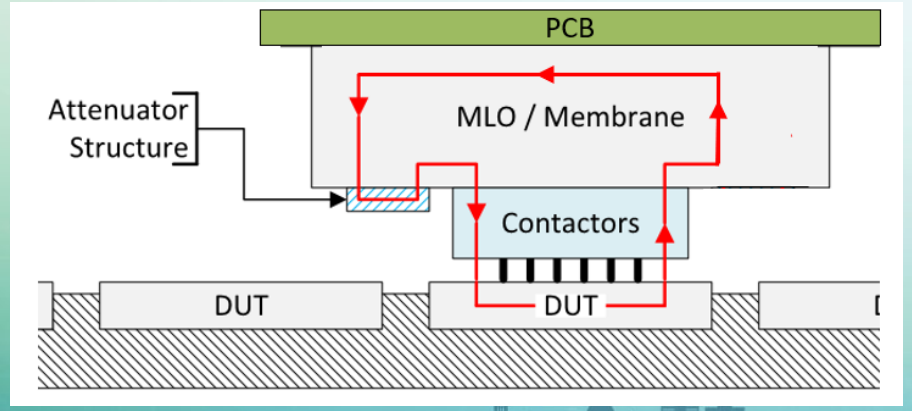


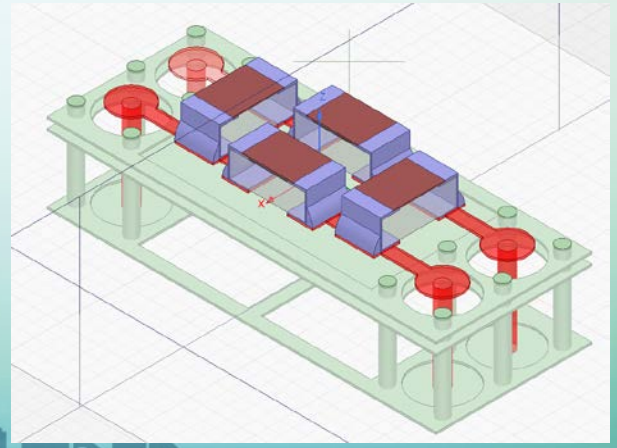
  - **Custom Attenuation Network** ✓
    - Can match any impedance
    - Can be design for differential mode
    - Short Lead Times for off-the-shelf components



Designing a Custom Attenuation Network

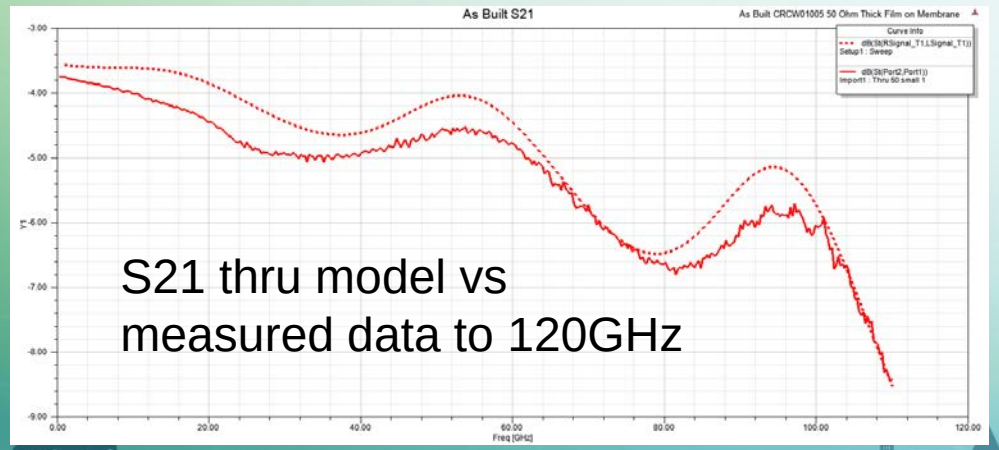
- **To match module loss, attenuation needs to be added to the probe card**
  - This can be achieved using an O-attenuator circuit and SMT resistors on the MLO
  - Requires superb 3D modeling to accurately match module

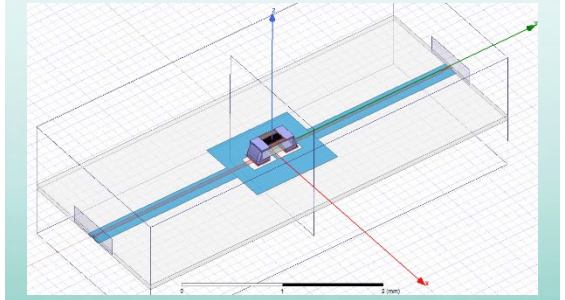


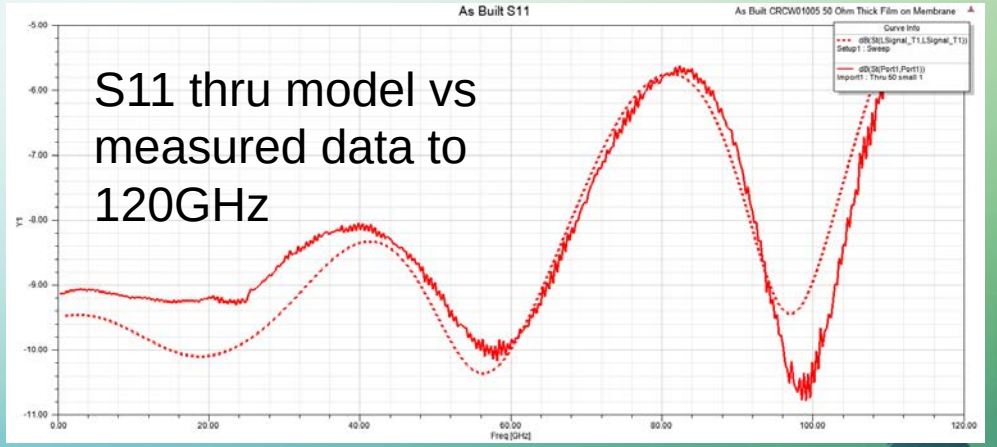


Creating a 3D Resistor Model

- With the Nyquist frequency approaching mmWave, accurate 3D modeling of the attenuation network is needed
- FFI created a 3D resistor model that can be tuned to match a variety of package types and resistance values

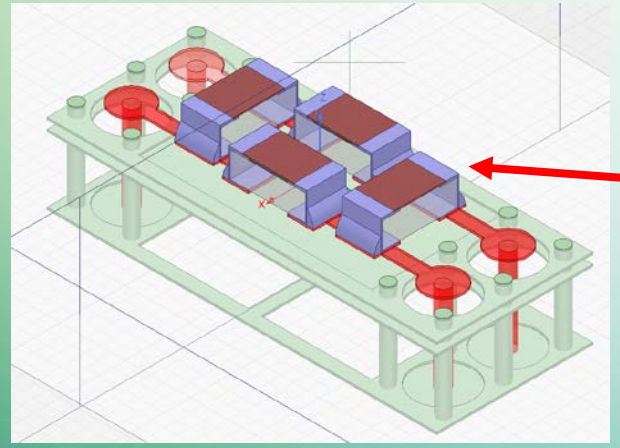






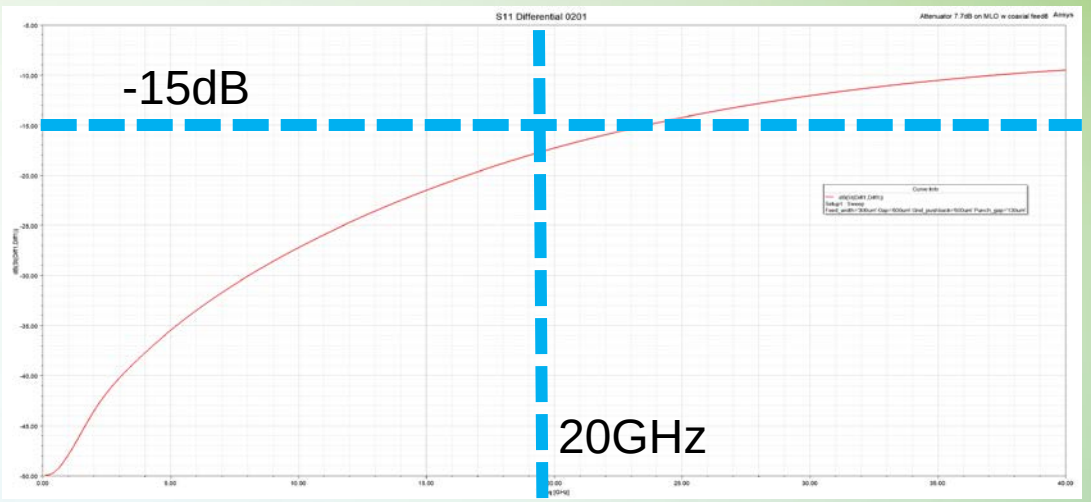
Optimizing Attenuation in the MLO

- **With Accurate resistor models, attenuation in the MLO can be fully optimized through simulation**

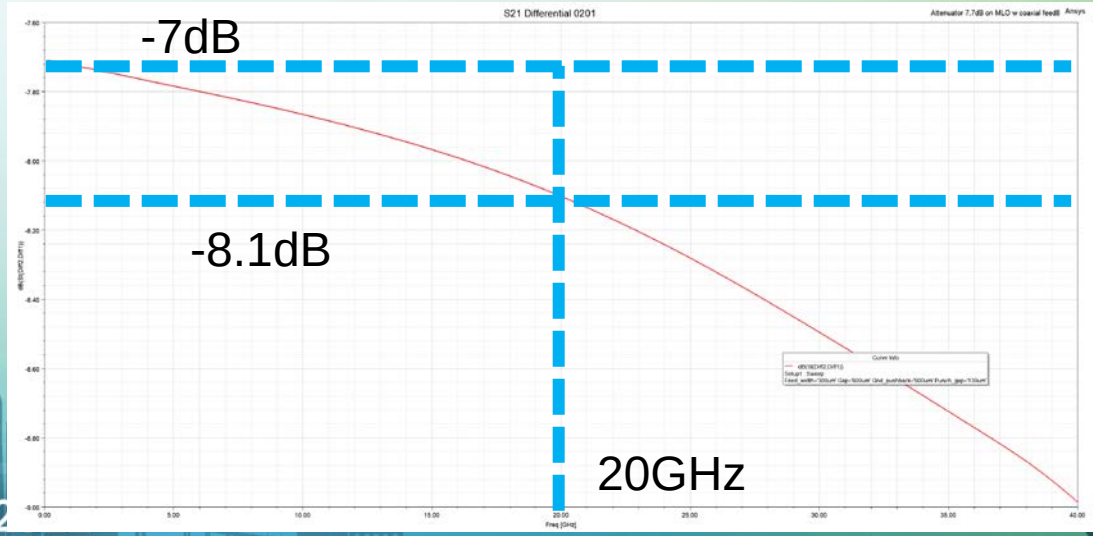


Parasitic compensations of via inductance combined with capacitance from SMT component pads. Can only be optimized with 3D field effects

Return Loss

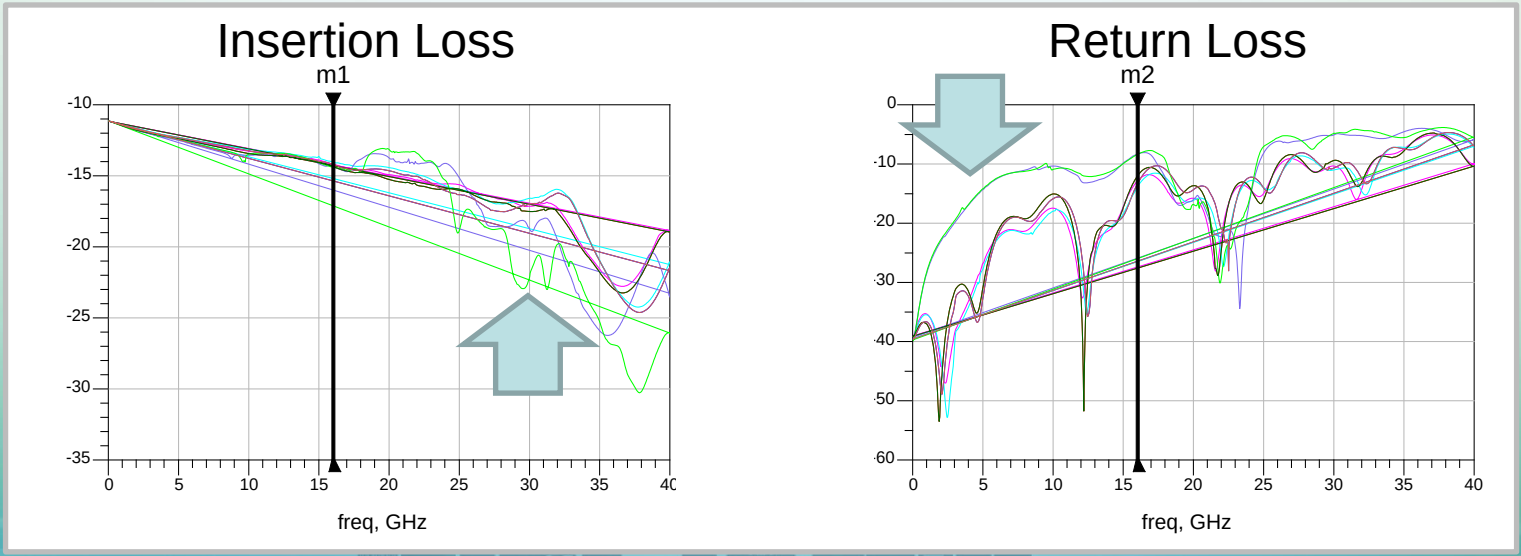


Insertion Loss



Full Path Sensitivity Analysis of Attenuation

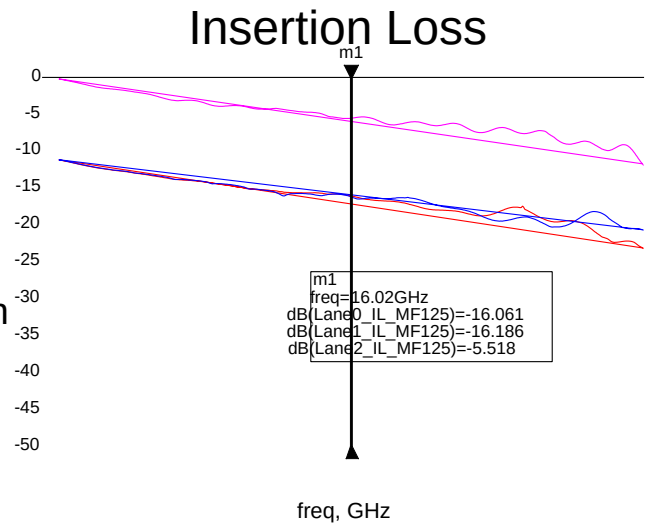
- **FFI Optimized Footprint for process/design variation**
  - Explored multiple sources of variation and multiple permutations of process variation
  - FFI optimized design to where only a single, easily controlled variable now impacts overall performance

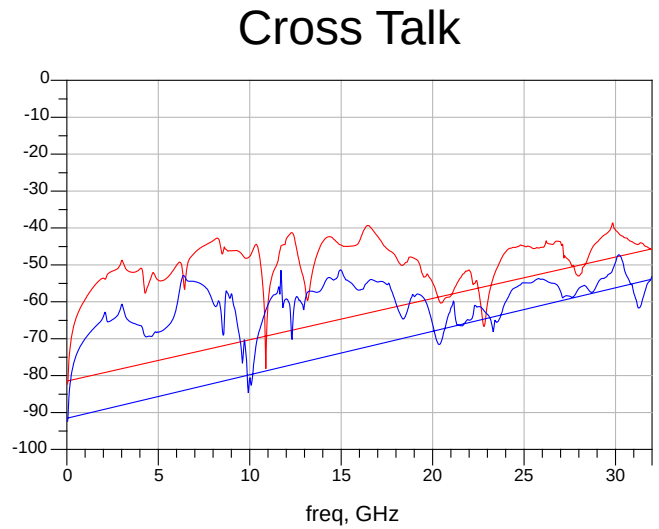


FFI Full-Path Module Matching capability

- **Full Path Simulation Includes Probe(s), MLO, and attenuation**
  - Dampens return loss “structure”
  - Improves Cross Talk
  - Flat attenuation across entire spectrum

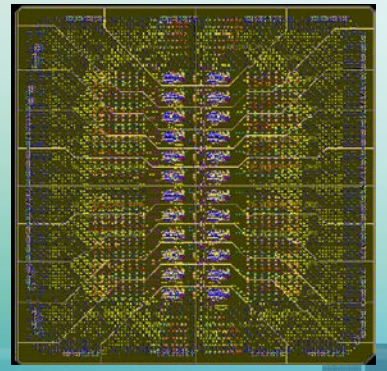
Pink = POR Loopback
Blue/Red = Attenuation

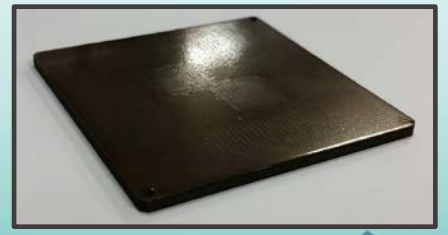




Final Thoughts: Finding Space on the Probe Card

- **Each attenuation circuit will compete with real-estate on the MLO for bypass capacitors which are used for PI improvements**
- **With some applications requiring >150 loopback differential pairs per DUT, how do we fit this all on the probe card?**
  - Solution: By increasing the active area of the MLO
- **FFI Newly released 120mm MLO increases total area by 44% compared to previous 100mm field size**





How Does Equalization Impact Wafer Test?

- **Testing the Equalization and Digital Signal Processing**
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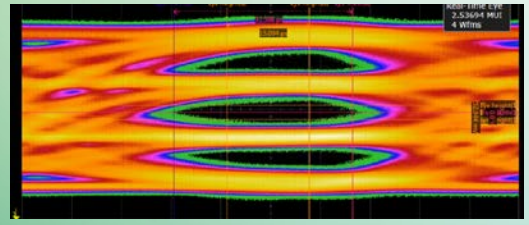
  - Challenge 2: Matching Module Performance
    - Solution 2: Custom Attenuation Network in the MLO
  - Challenge 3: Verifying that Full Functional Test will Work

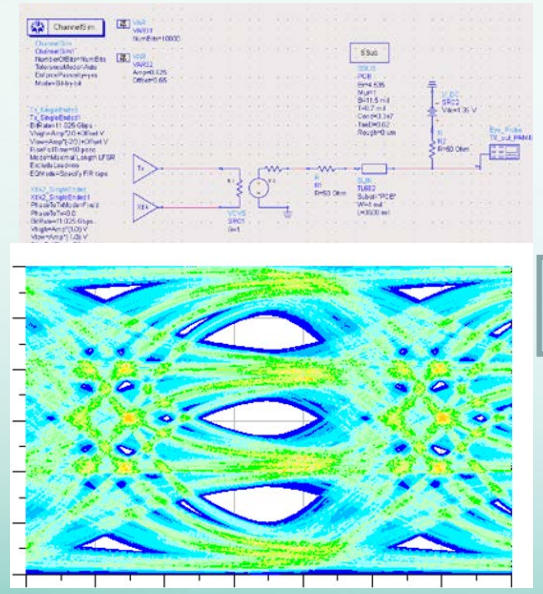
Challenge 3: How to Ensure Attenuation Works

- **How do we determine if this attenuation actually-works with equalization?**
  - Through full-digital simulation

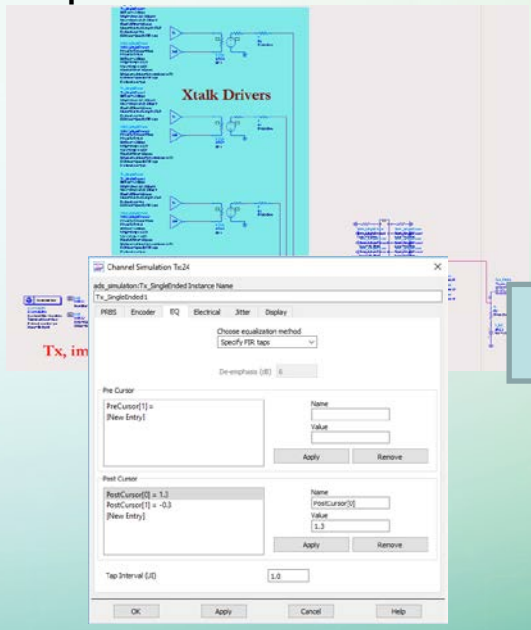
Eye Input from Customer



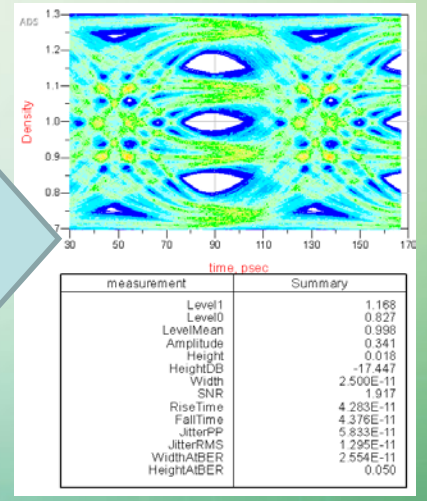
Replicate in ADS



Add Equalization and Probe Card Loss



Output final Eye diagram, BER



measurement	Summary
Level1	1.168
Level0	0.827
LevelMean	0.998
Amplitude	0.341
Height	0.018
HeightDB	-17.447
Width	2.500E-11
SNR	1.917
RiseTime	4.283E-11
FallTime	4.376E-11
JitterPP	5.833E-11
JitterRMS	1.295E-11
WidthAtBER	2.554E-11
HeightAtBER	0.050

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    - Solution 2: Custom Attenuation Network in the MLO
  - Challenge 3: Verifying that Full Functional Test will Work
    - Solution 3: Full Functional Simulation of the Probe Card with Equalization

Conclusion

- **FormFactor enables the next-generation test solutions for high-speed digital applications**
  - Hybrid Probes for custom impedance matching in the probe head
  - Custom attenuation in the MLO that matches any impedance and level of attenuation required
    - Full 3D models of attenuation correlated to measurement
    - Optimized Attenuation circuit that accounts for process variations
    - 120mm MLO size for increased space for routing and components
  - Complete Digital simulation capability that matches the actual use case of the probe card to the end environment
    - Enables fast turn-around time from probe card installation to full, optimized data collection

Special Thanks

- Uyen Nguyen – Sr. RF Engineer at FormFactor
- Ernie McReynolds – Sr. Principal Electronic Design Engineer at FormFactor