



PROBE TODAY, FOR TOMORROW
2023 CONFERENCE

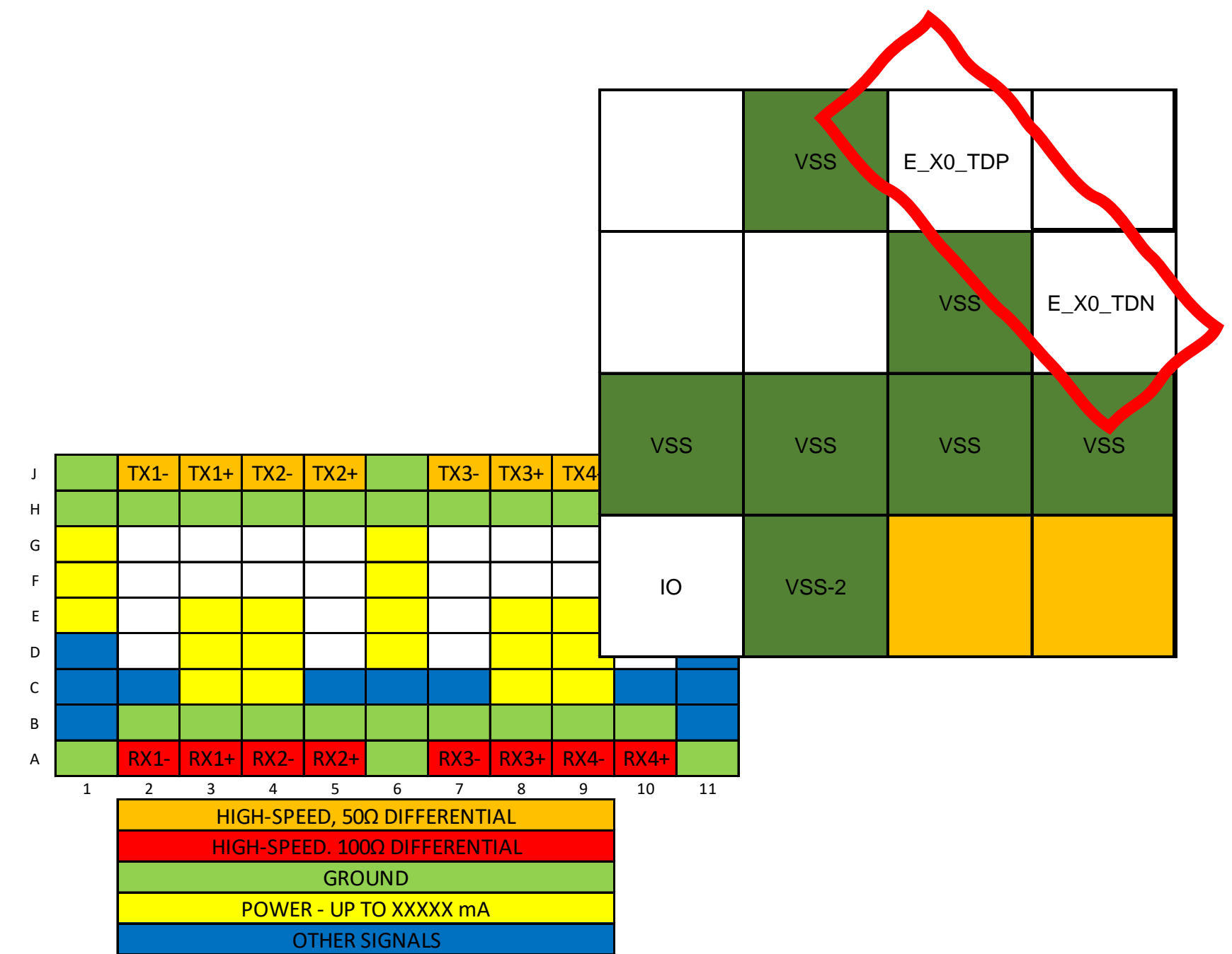
Optimizing Probe Head Design Using a J-Tuned™ Process on Spring Probe Technology

Johnstech®

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Johnstech International

What is the J-Tuning process?

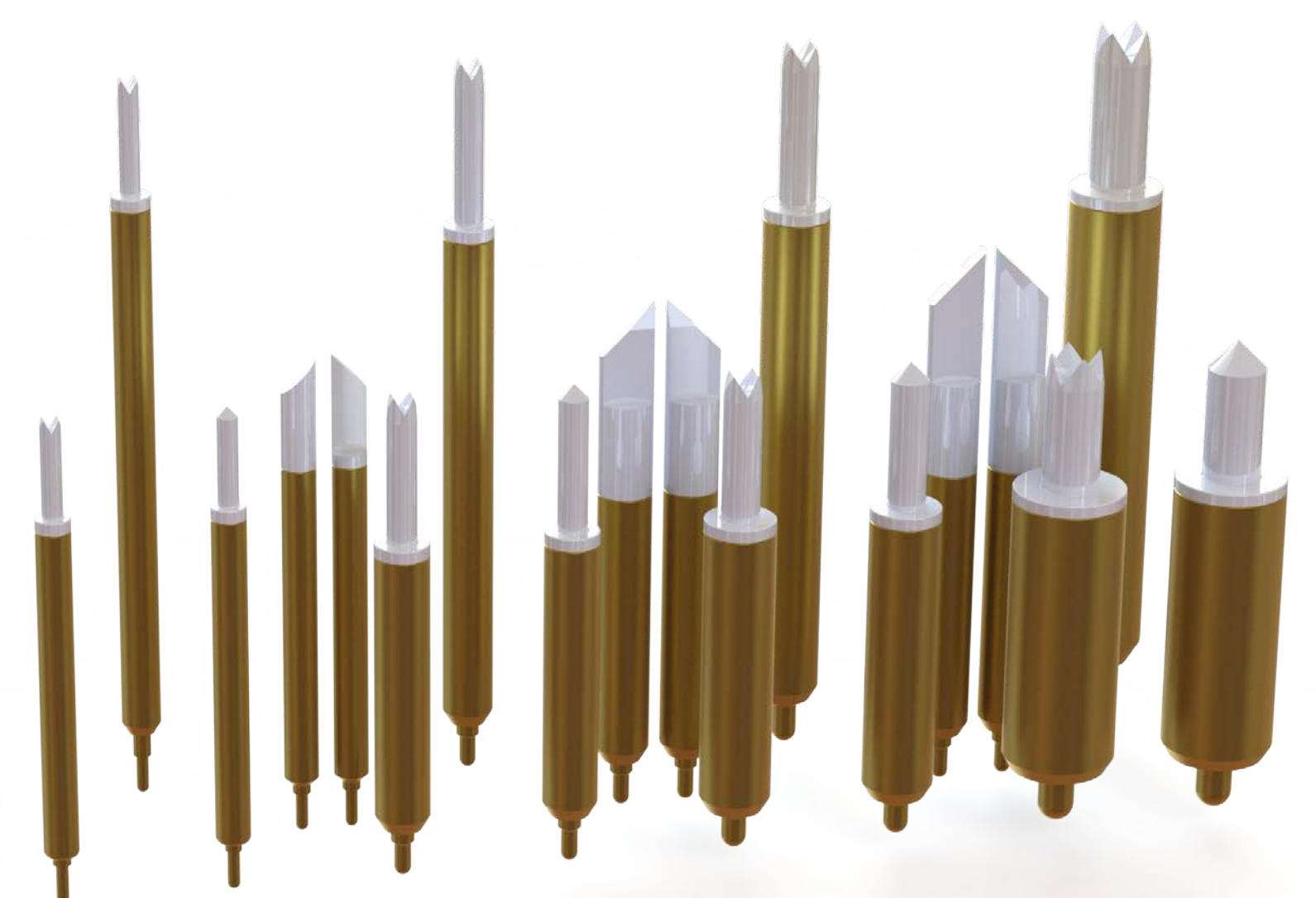
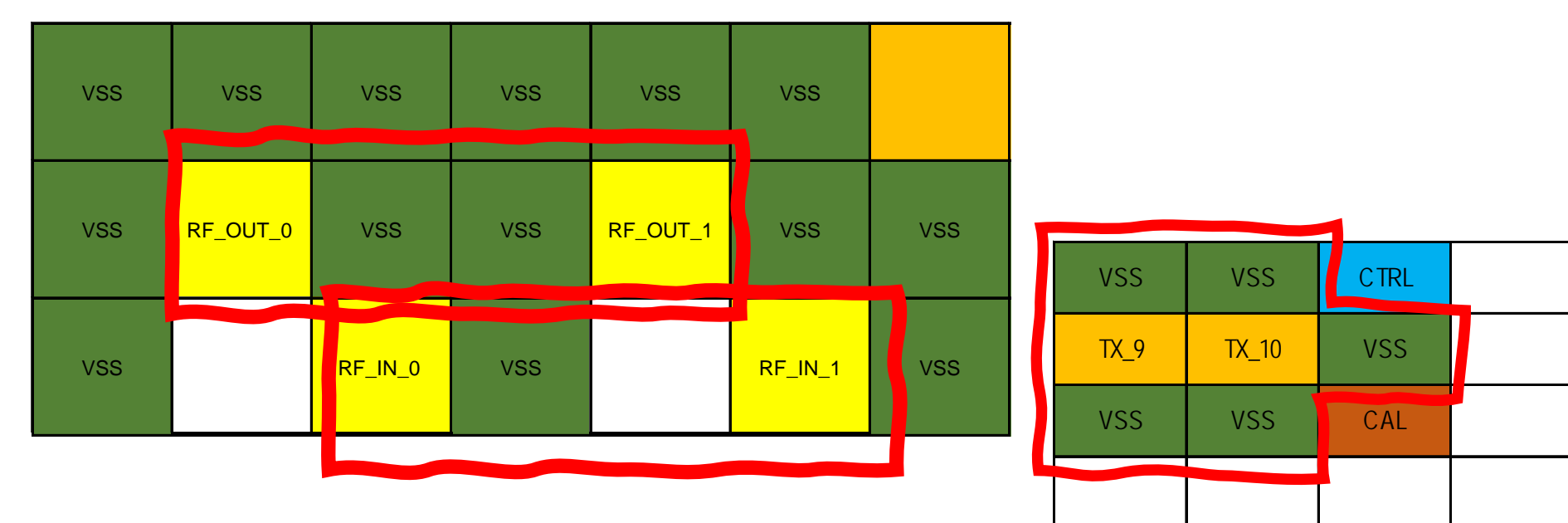
- Analyzing and understanding all the critical DUT signal pin configurations – stripping them down to basic structures:
 - Analog signals and their Insertion Loss and Return Loss requirements at given frequencies
 - Digital signals – differential pairs at given impedances: 50Ω, 100Ω, other
 - Mechanical POD/Wafer-map for physical location of signal pins, ground pins, and other pins, within DUT array
 - PCB, encrypted DUT S-Parameter models and other inputs can be included
- Review DUT data sheet parameters that are most critical:
 - Required digital data rates and modulation – NRZ, PAM-4, etc.
 - Analog losses – Insertion and Return vs. frequency (wide and narrow-band)
 - Crosstalk limits between signals
 - Kelvin requirements: $R_{\text{DS(on)}}$, critical VDO,...
 - Power requirements
- Modeling critical configurations in HFSS and other simulation tools – worst case or unique signal conditions
 - Building valid and quality S-parameter models using frequency-dependent dielectric properties
- Tuning the design models to achieve best desired performance using the available design ‘knobs’:
 - Choosing the best SHOTO or YARI spring pin for the configuration
 - Configuring the housing for optimal impedance matching to the DUT signal environment
 - Additional ANSYS mechanical and/or thermal modeling may be needed to optimize for planarity and thermal requirements



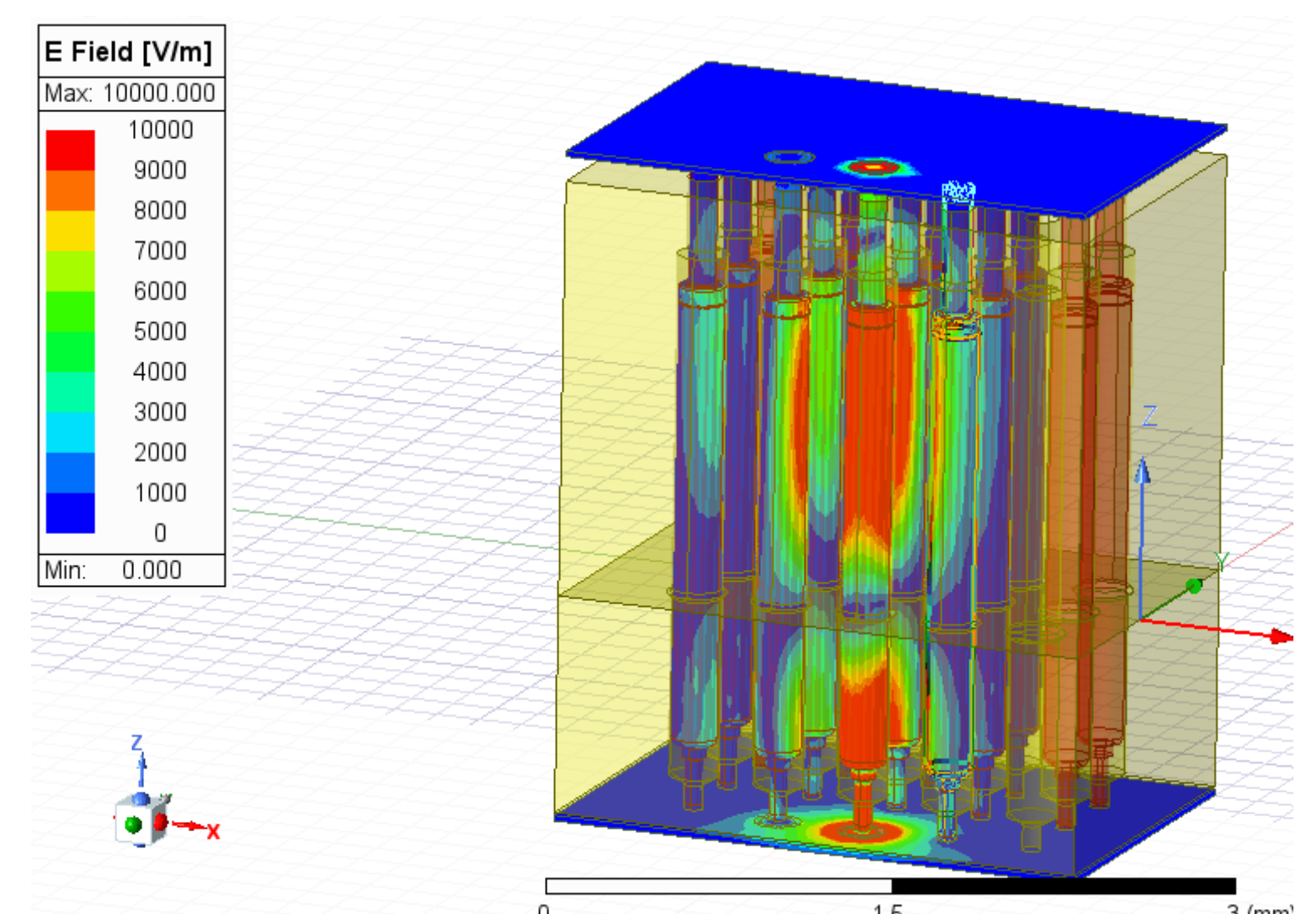
Output Stage MOSFETs		switching		
$R_{\text{DS(on)LS}}$	Drain-to-source resistance, low side	$T_j = 25^\circ\text{C}$, LDMOS only	40	mΩ
$R_{\text{DS(on)HS}}$	Drain-to-source resistance, high side	$T_j = 25^\circ\text{C}$, LDMOS only	40	mΩ

IDD Protection

INPUT TO OUTPUT CHARACTERISTICS		V _{CE} = High, V _{IN} = 0.5V _{DD}		
VDO	Drop-out voltage IN to OUT	CE = Low, V _{IN} = 5V, I _{OUT} = 1A	170 280	mV



Johnstech SHOTO, YARI, and DAISHO pins are highly standardized to give maximum flexibility for J-Tuning probe head performance



Validating Models and Measurements

Probe heads are considered as a passive bi-directional transmission lines. The S-parameter representations must then always demonstrate Passivity, Reciprocity, and Causality:

Passivity:

- The component is passive if it consumes energy, but does not produce energy
- Is incapable of power gain
- $S_{21} < 0$
- $-1 < S_{11}$ or $S_{22} < +1$
- There must be no energy of the propagating EM wave before $t=0$ in the TDR (Time Domain) plot

Reciprocity:

- A reciprocal network always has a symmetric S-parameter matrix. The transmission of a signal between any two ports should not depend on the direction of propagation
- For a passive system, $S_{12} = S_{21}$

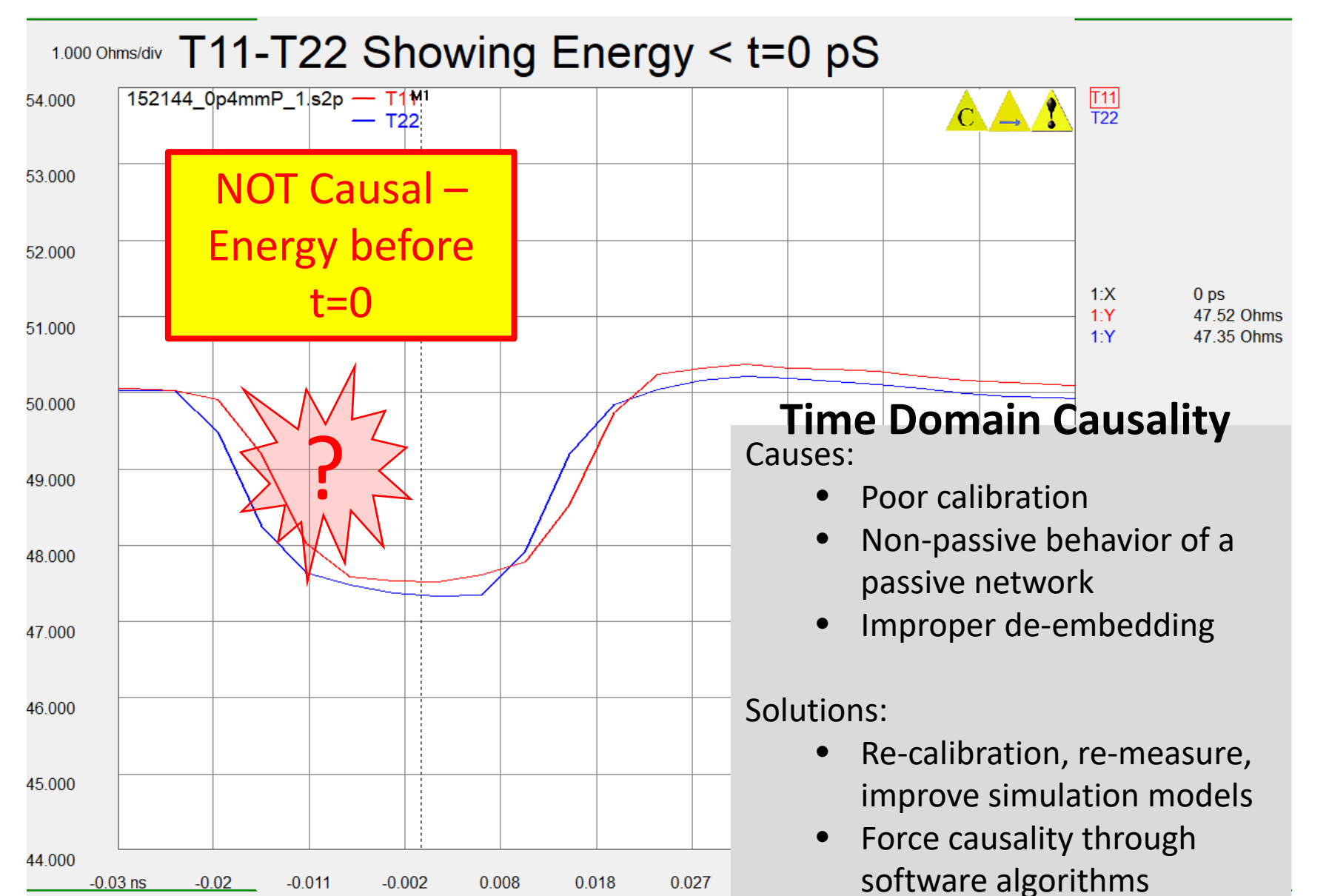
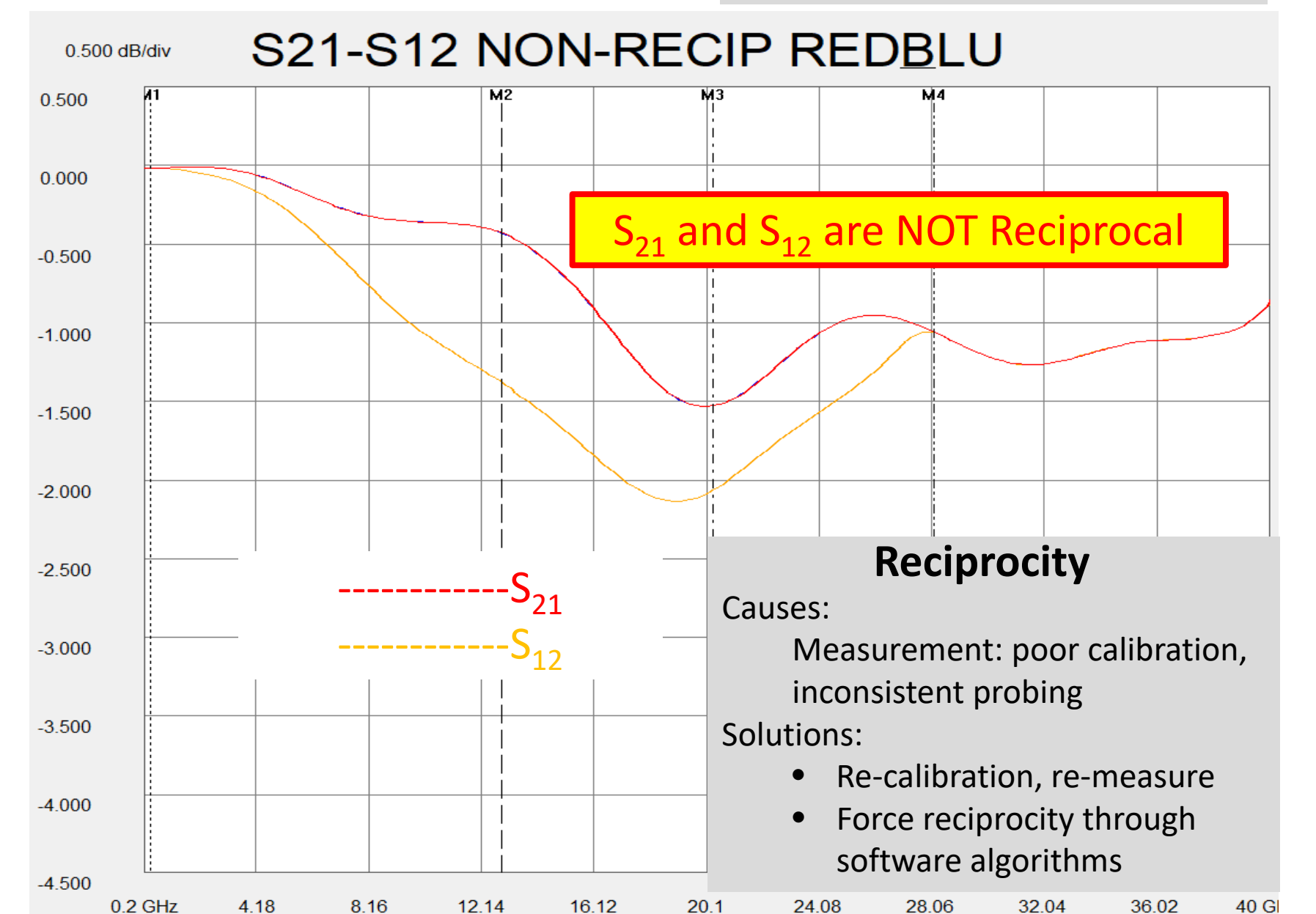
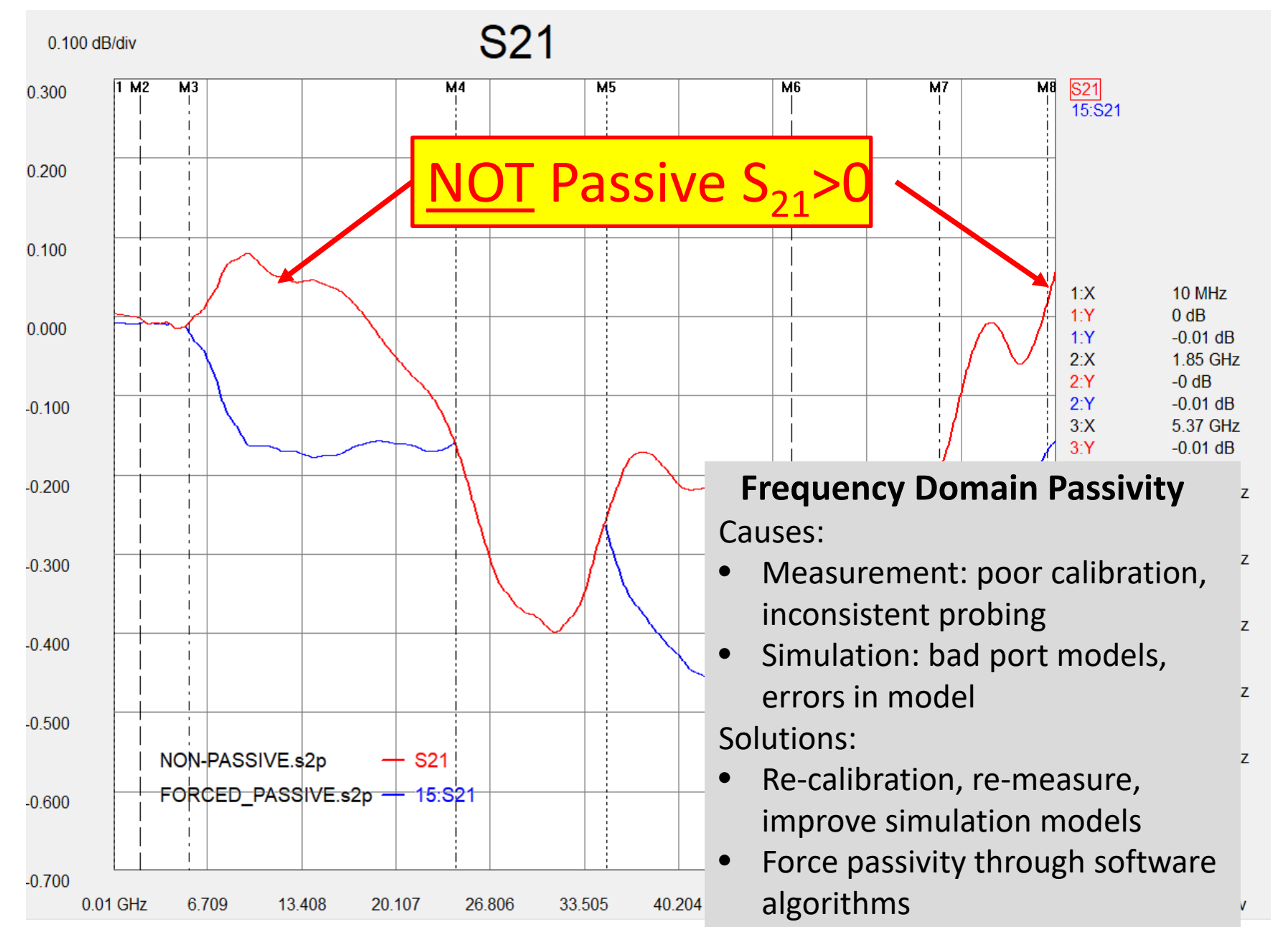
Causality:

- Extrapolates to > sweep range. Not a real physical model. Used mainly for transient simulations, so optional
- 2 ways of determining / forcing causality:
 - DFT (Discrete Fourier Transform) (Keysight)
 - Causality estimation (Anritsu) using Smith Chart techniques of phase rotation

There is discussion over which method is better and for which type of application

Testing and Correcting For Passivity, Reciprocity

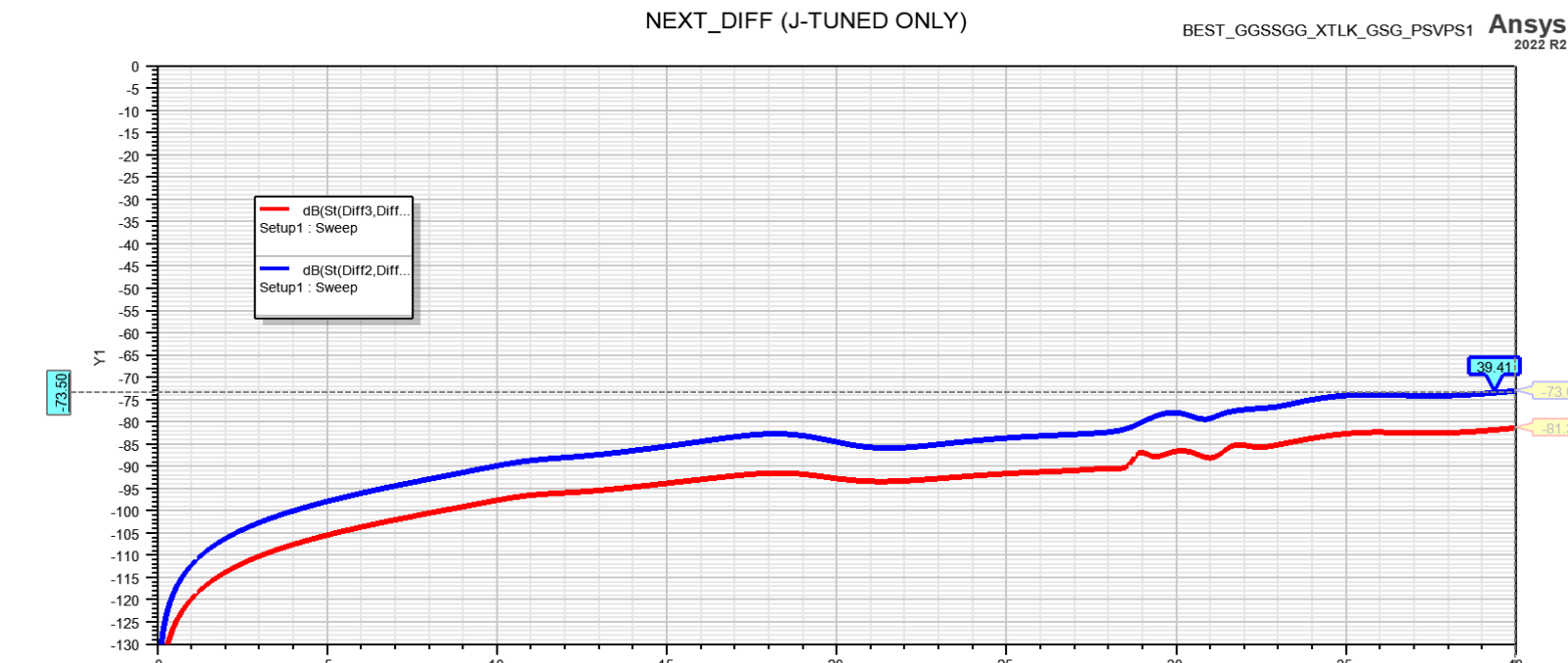
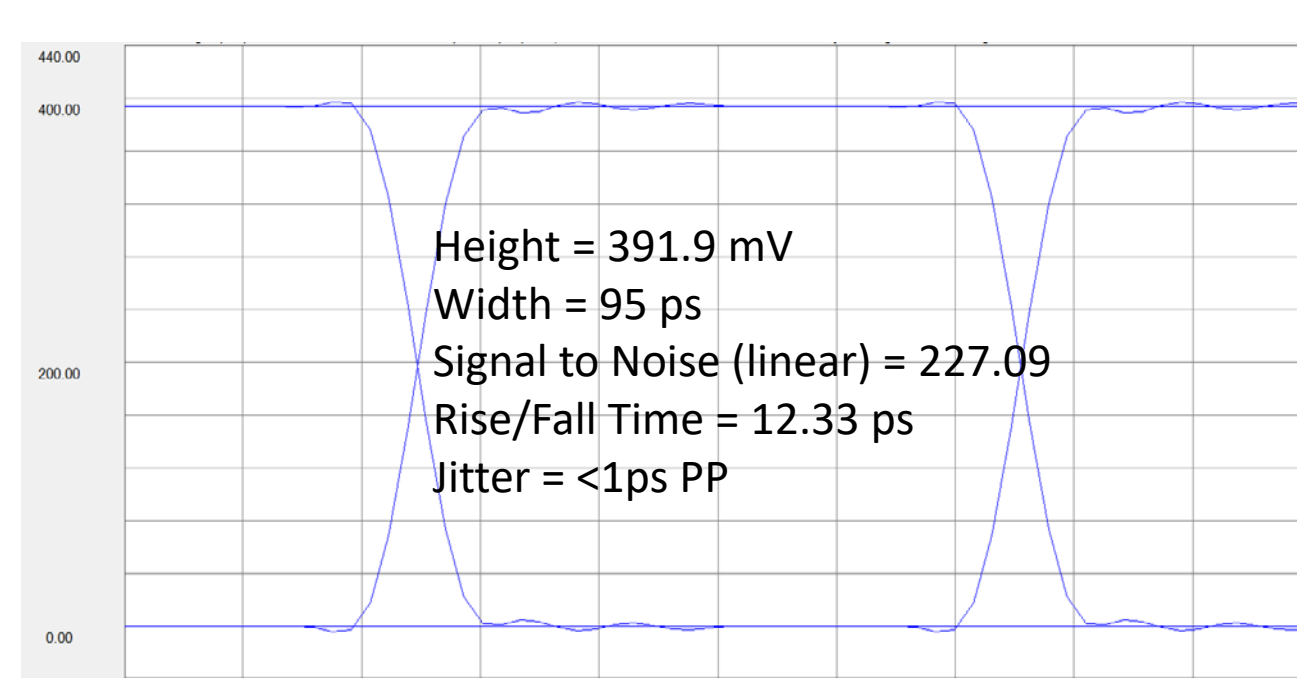
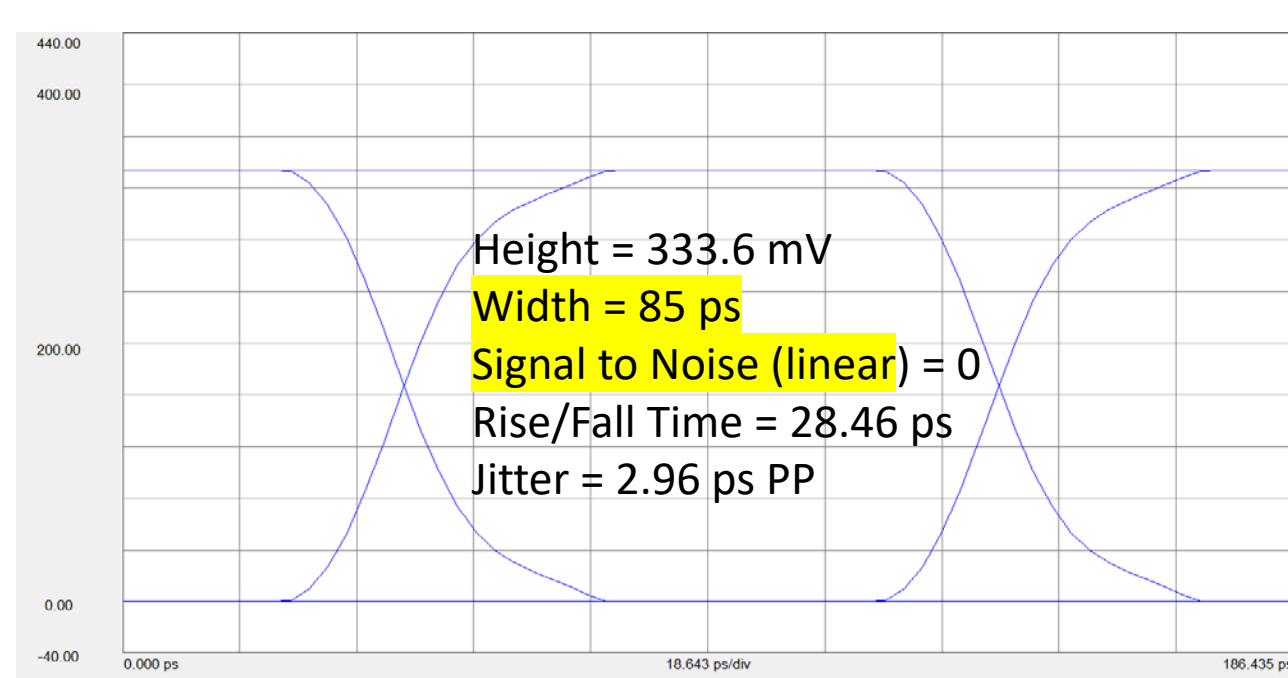
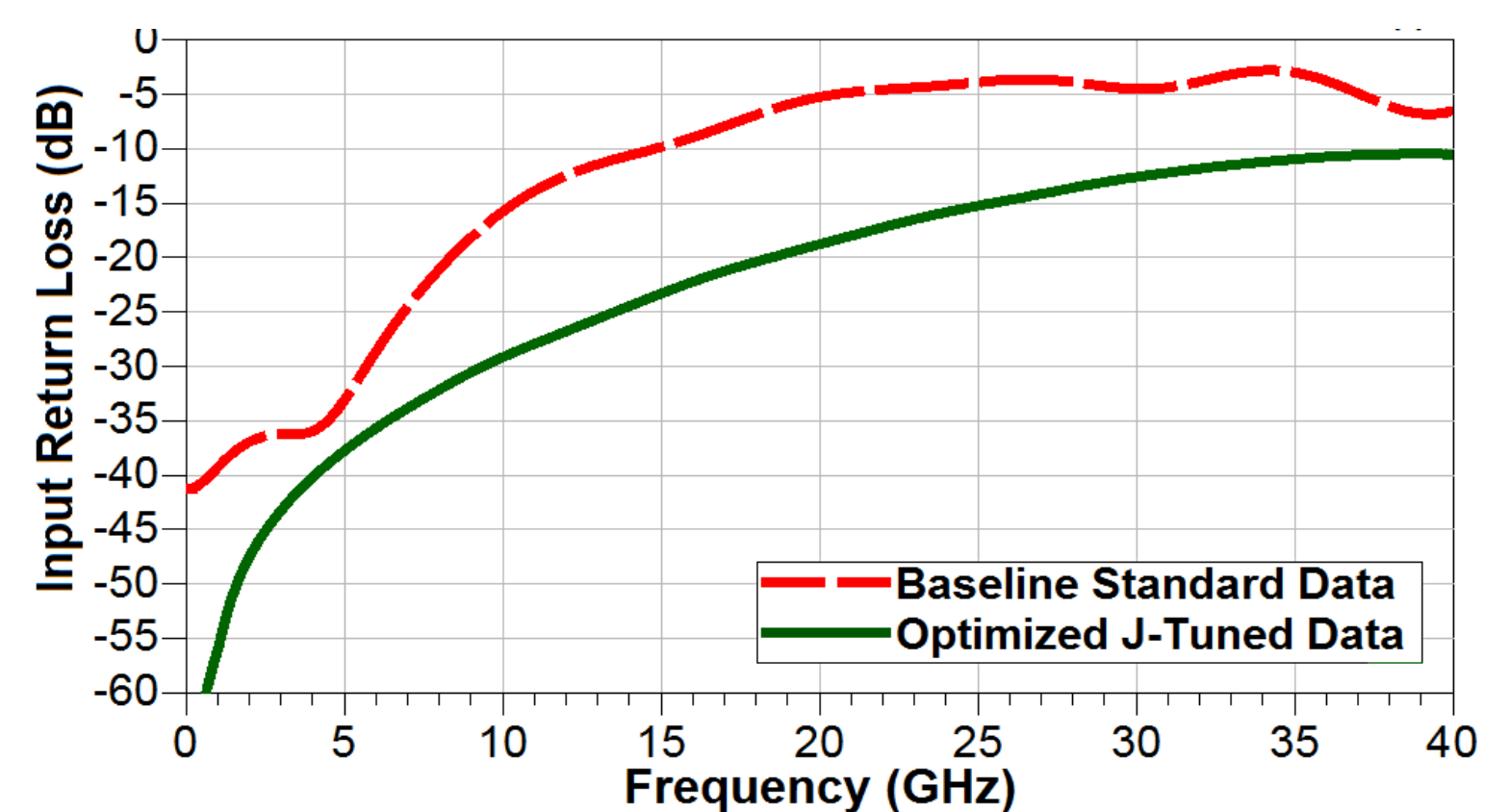
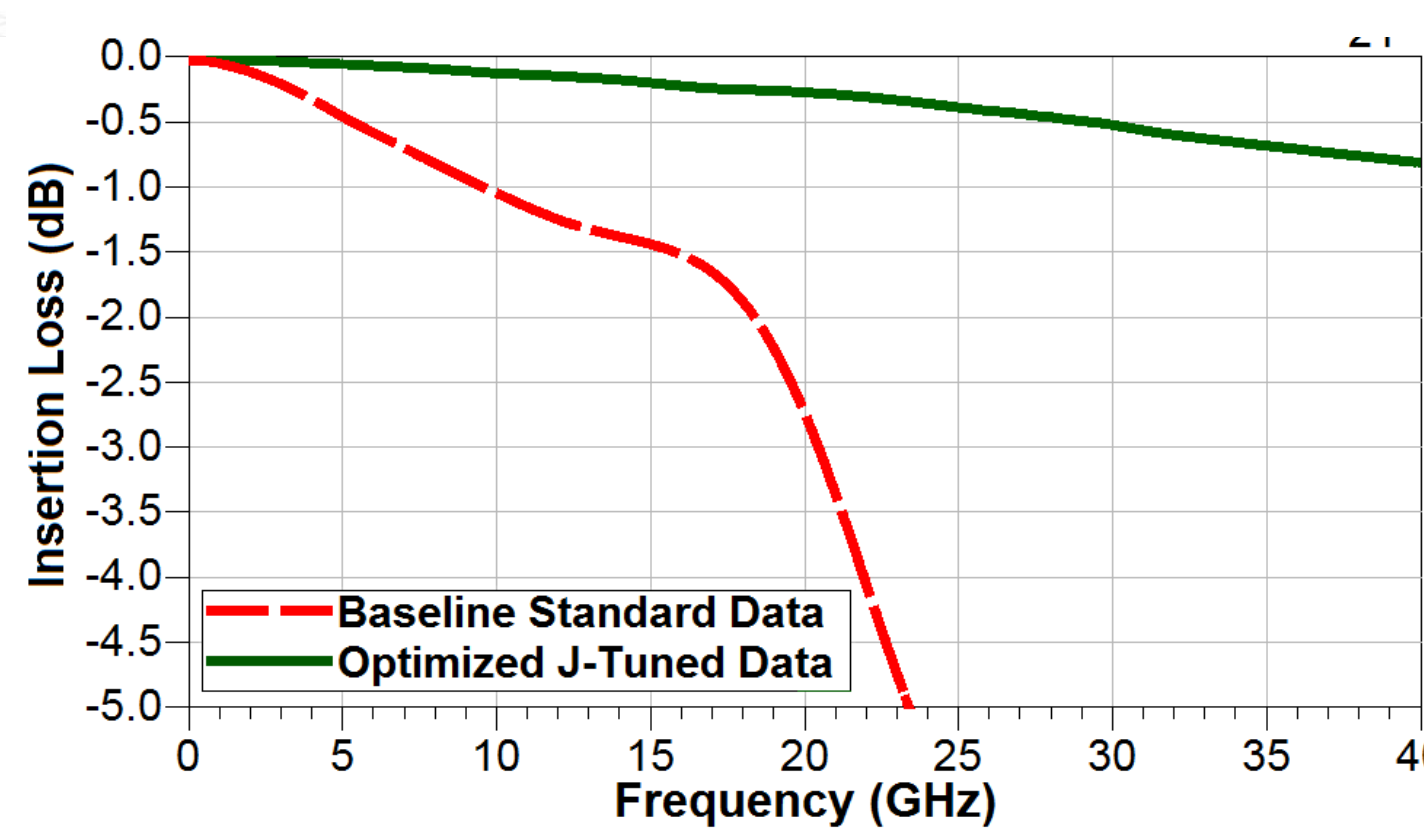
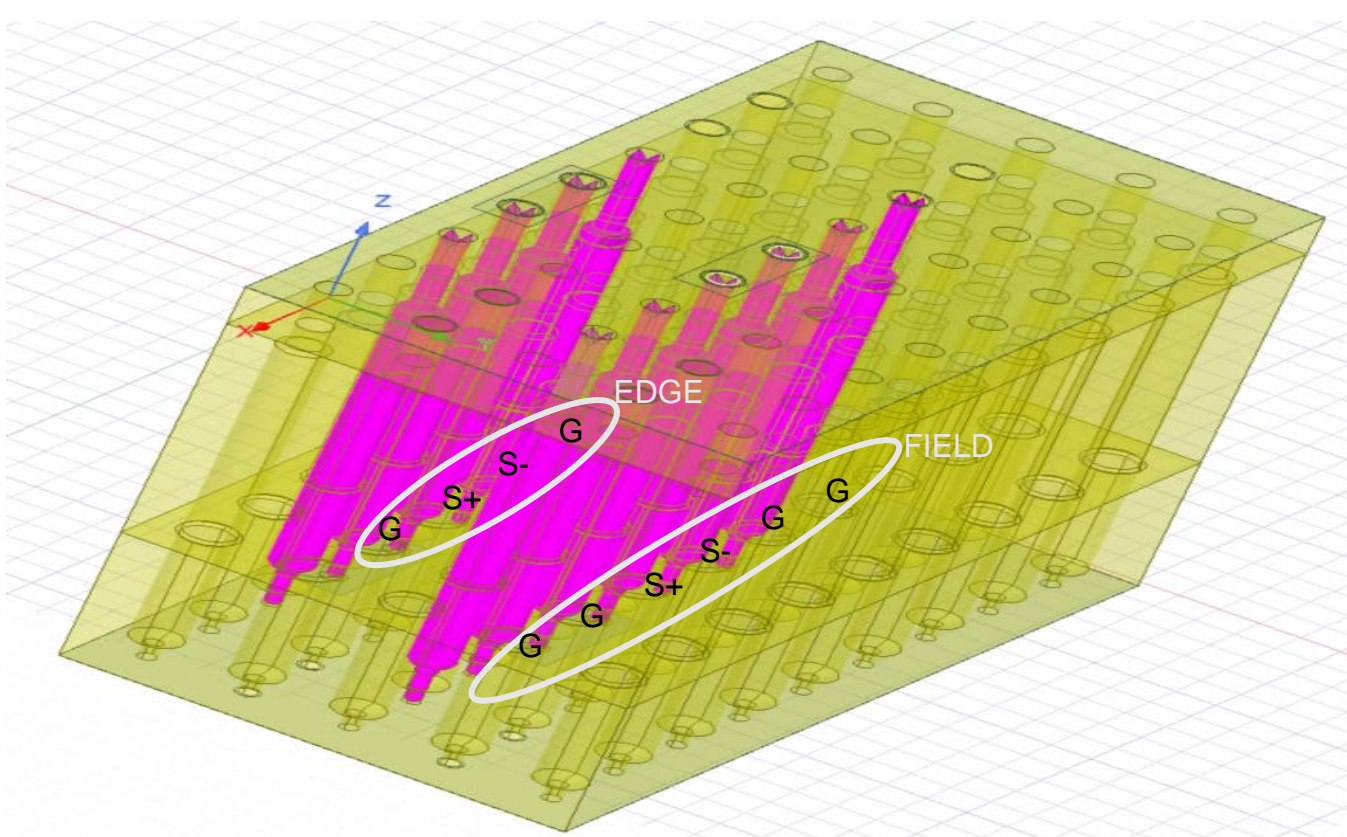
- Post-processing software offered on the market can test for these 3 validity tests on a S-parameter files and force the S parameter matrices to be valid



J-Tuning Optimization Case Study 1

DOE of 6 simulation models applied to customer data sheet specifications:

- Data rate: 10.56 Gbps serial NRZ – BW 5.28 GHz
- 3rd, 5th, 7th harmonic GSSG bandwidth: 15.8, 26.4, 37 GHz
- Match 100Ω differential and 25Ω common mode impedance

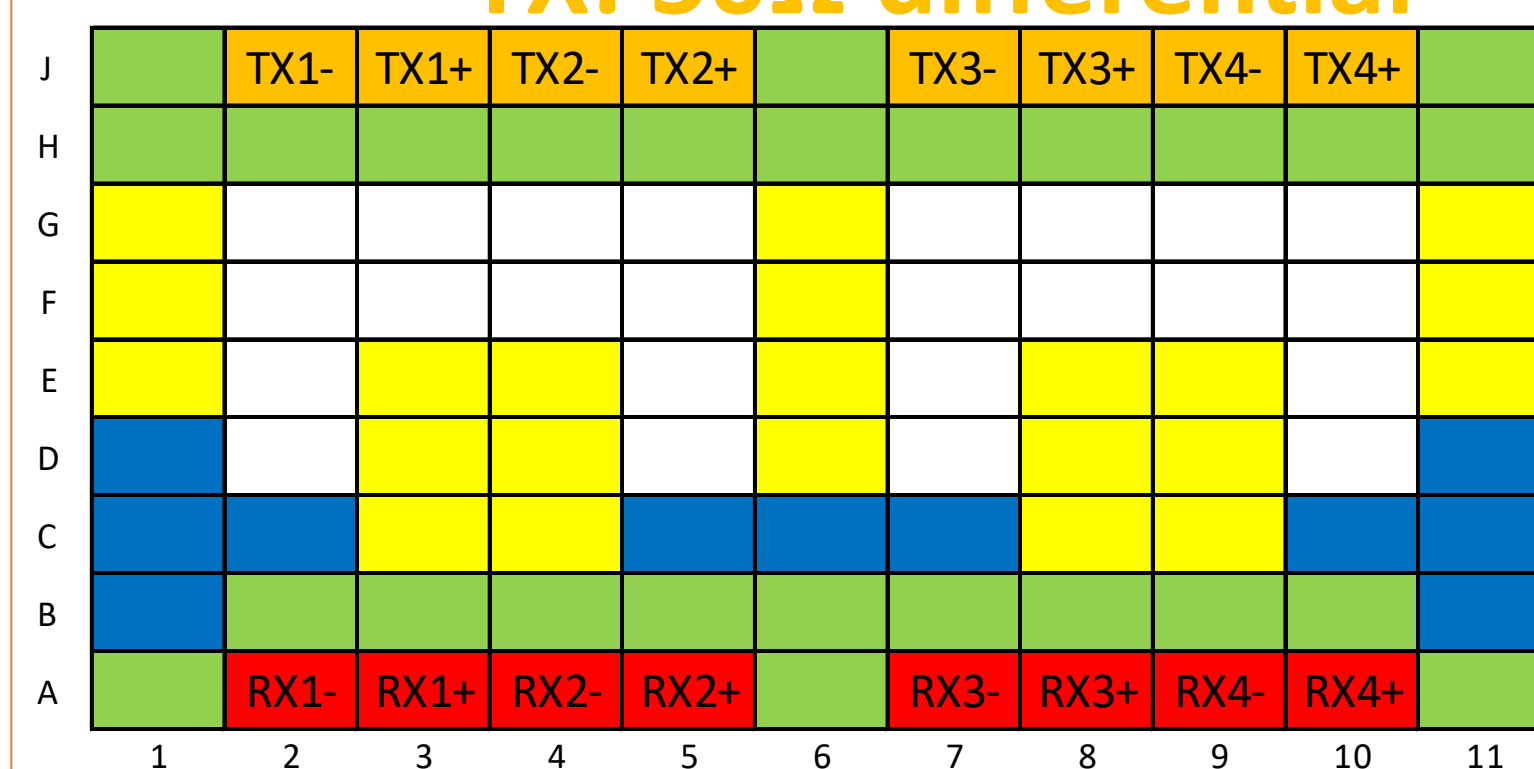


J-Tuning Optimization Case Study 2

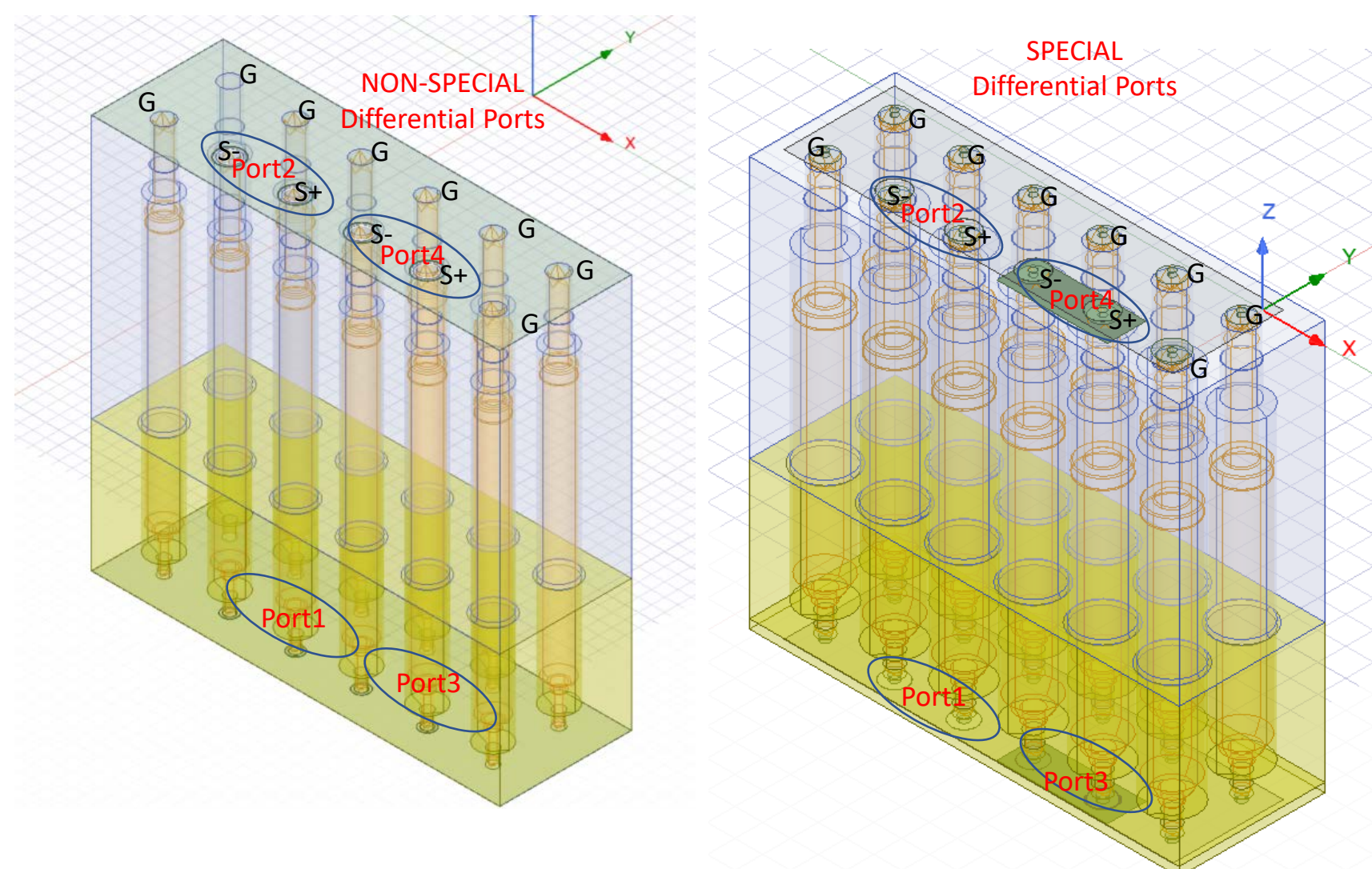
Goal: Replace existing multisite probe head with more robust spring probe solution without degradation in RF performance:

- Data rate: 10.56 Gbps serial NRZ – BW 5.28 GHz
- 3rd harmonic GSSG bandwidth: 15 GHz -1dB Insertion Loss, 10dB Return Loss
- Match 50Ω differential and 100Ω differential impedance

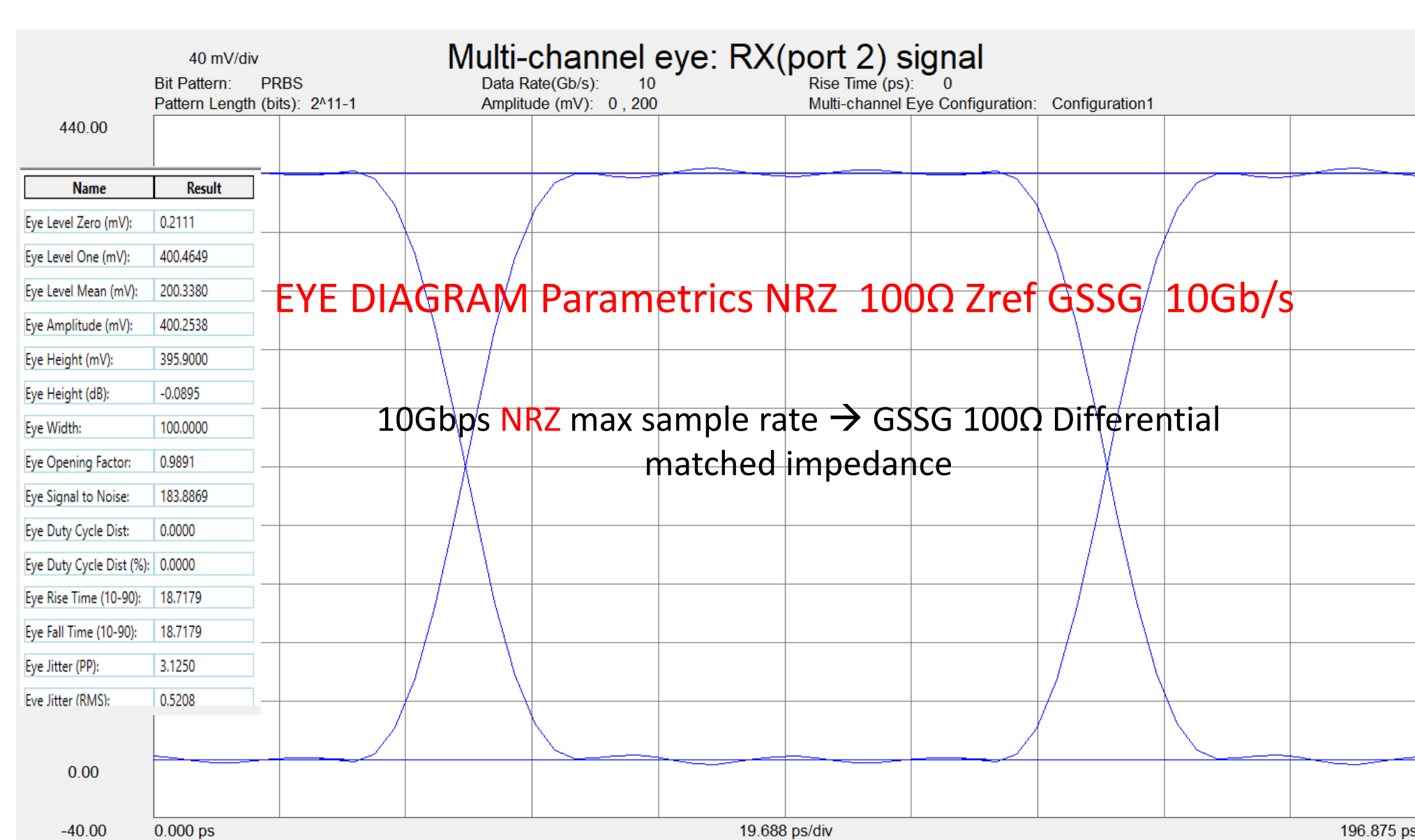
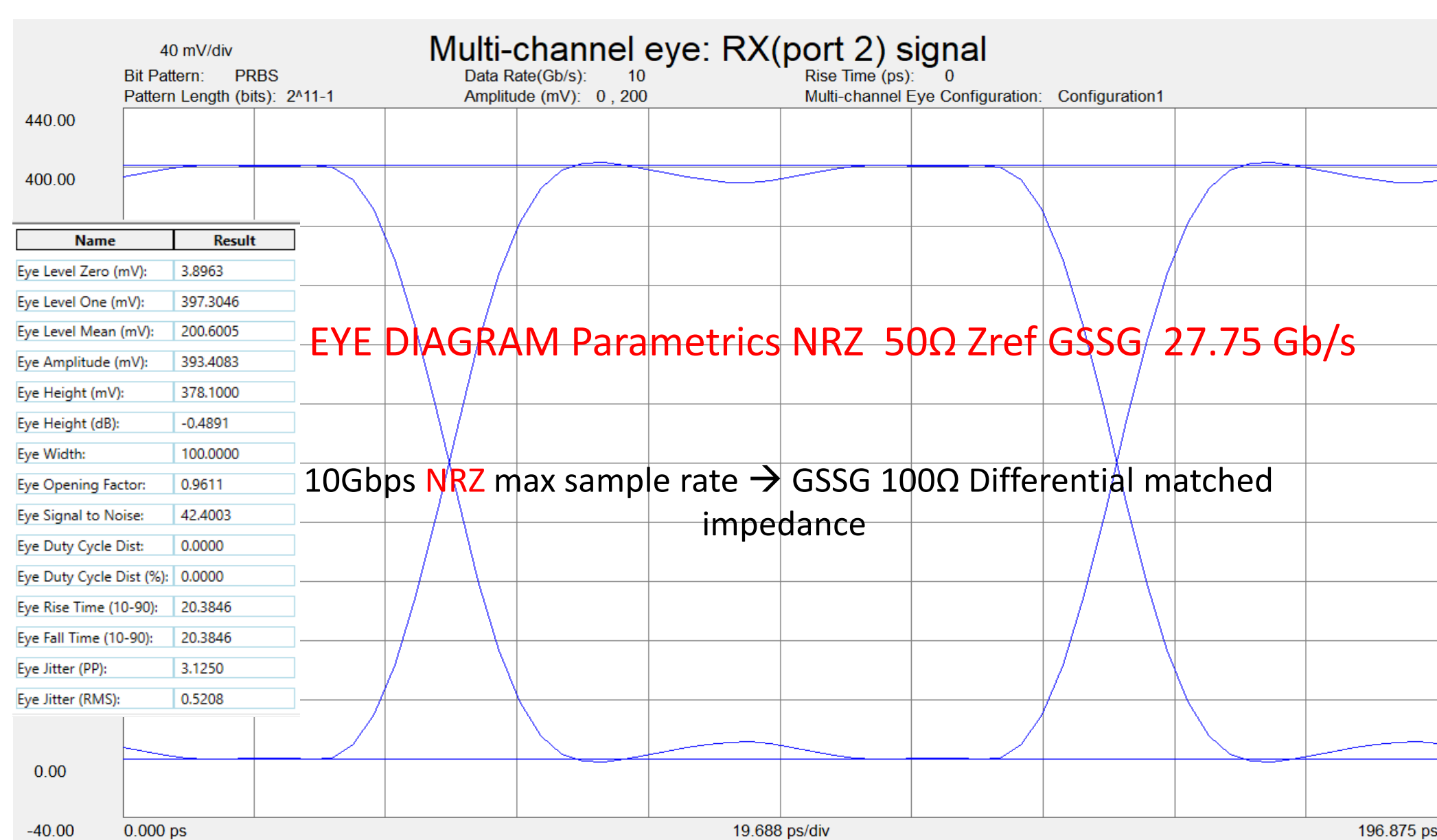
TX: 50Ω differential



RX: 100Ω differential



Final J-Tuned Model Type	Differential Impedance	-1 dB Insertion Loss (GHz) / @15 GHz	-10 dB Return Loss (GHz) Sdd22 DUT Side / @15 GHz
PROBE/HSG CONFIG A	100 Ω Diff	>40 GHz -0.25 dB	24.9 GHz/-19.5 dB
PROBE/HSG CONFIG B	50 Ω Diff	20.8GHz / -0.24 dB	19 GHz/-14.9 dB



Measurement Validation and Discussion

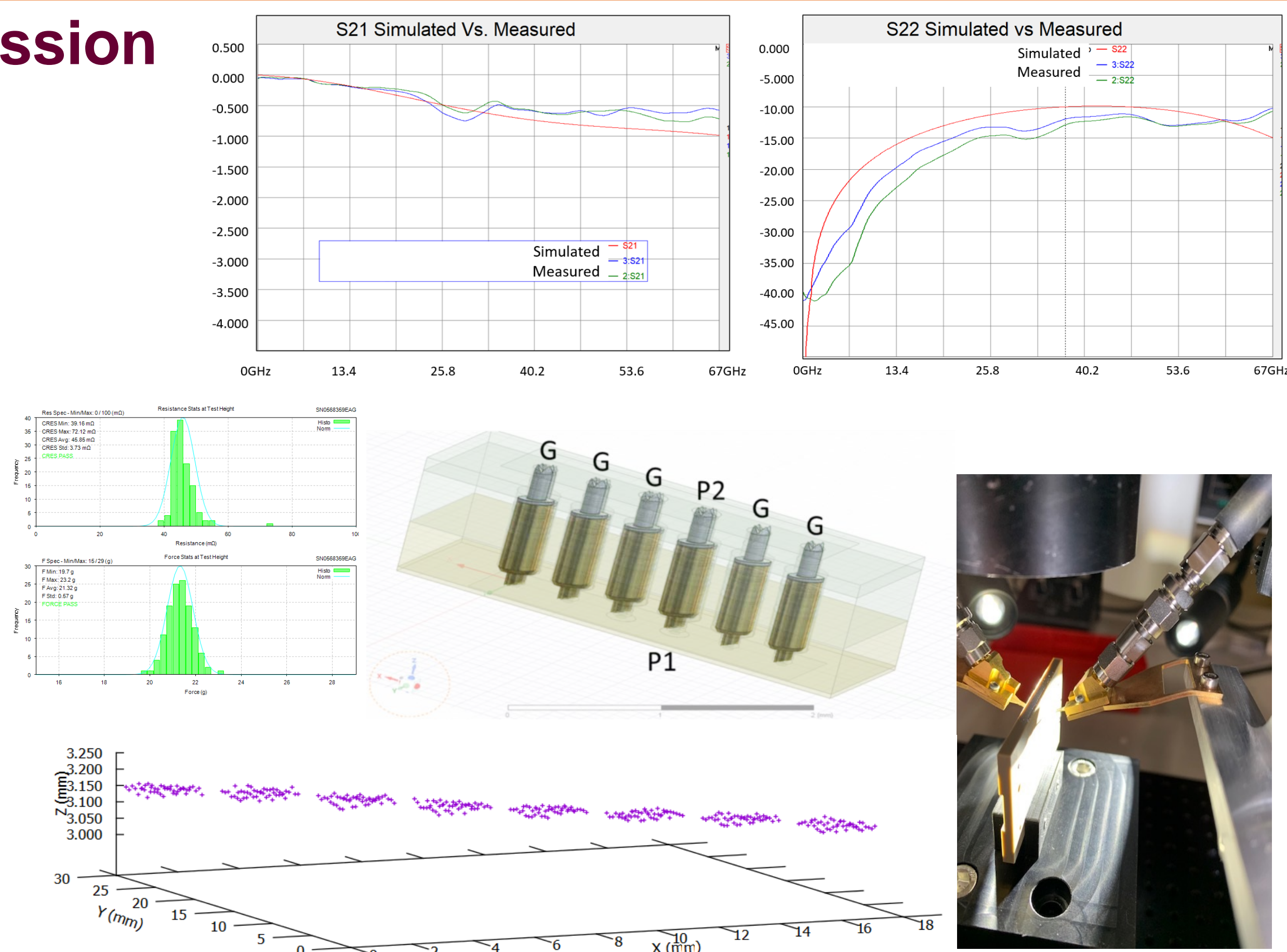
• S-Parameter validity checks:

- Passivity
- Reciprocity
- Causality

• VNA Measurements of identical configurations as simulation

• DC and mechanical checks:

- Probe card analyzer, FRD: Contact Resistance and Planarity



Questions ?

If you have any questions, please contact Valts Treibergs (vtreibergs@johnstech.com) or Jim Hattis

(jmhattis@johnstech.com), or to request a J-TUNED® optimized probe head, contact Johnstech Sales at info@johnstech.com
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