SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

High Voltage Probing goes Multi-Site

T. I. P. S.

Technical Innovation - Physical Solutions

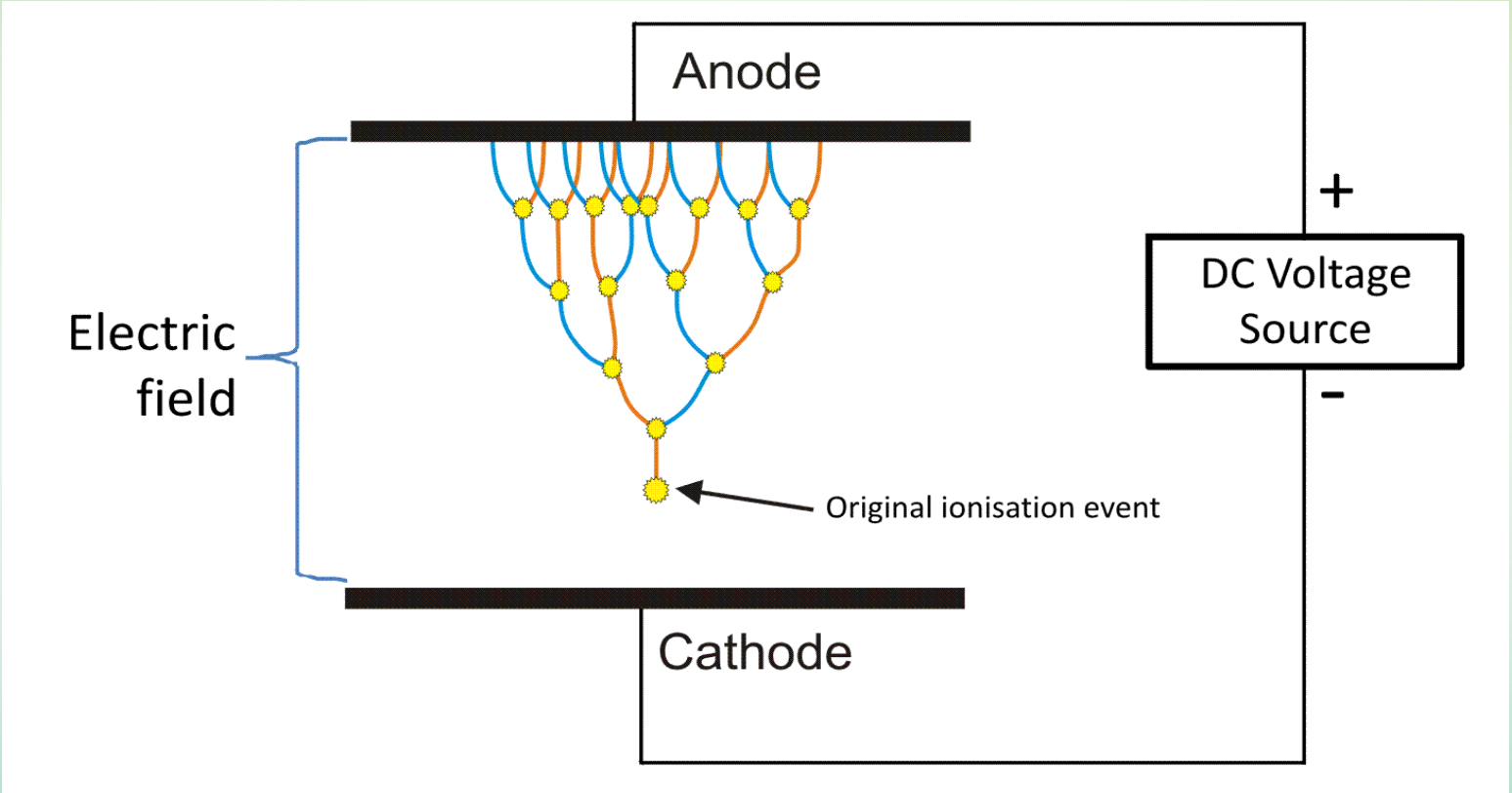
Dr. Rainer Gaggl

June 5 - 7, 2023

Overview

- High voltage wafer test – a refresher in Physics
- Single-site vs. multi-site: a few considerations
- HV "crosstalk" in multi-site arrangements
- Parallel vs. sequential HV test schemes (and combos)
- Probe card design and wafer edge test coverage
- Summary and Outlook

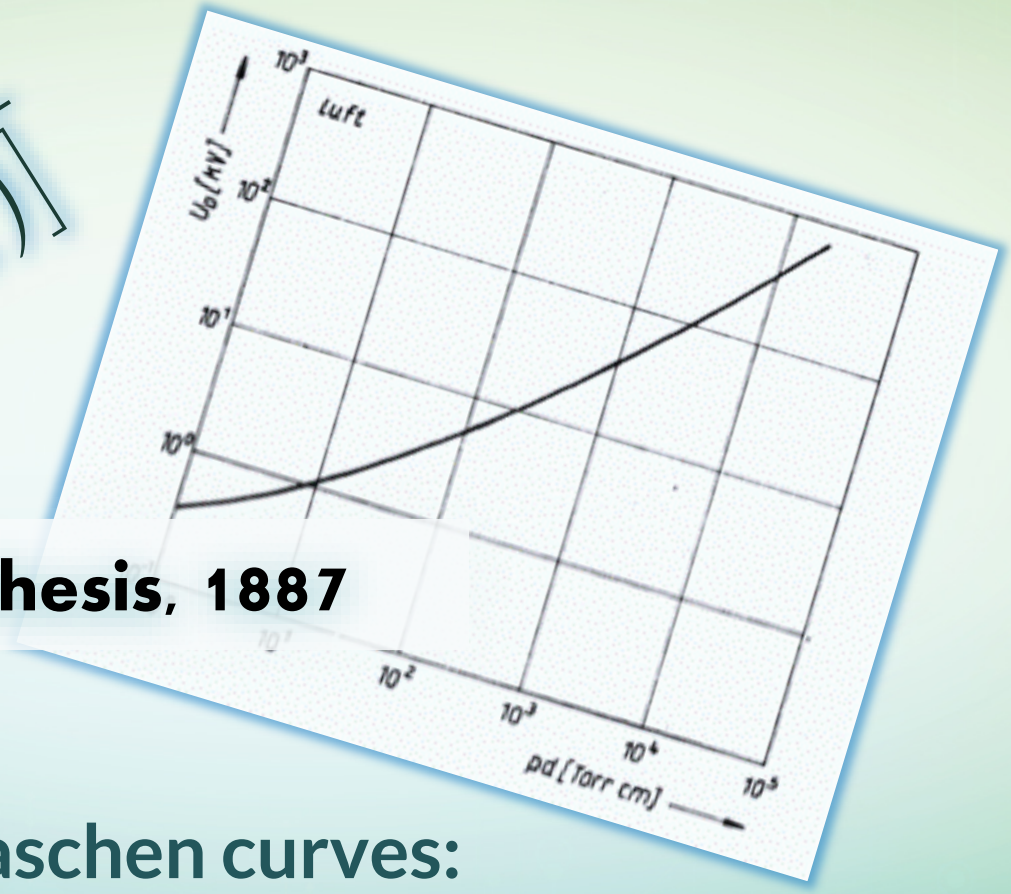
High Voltage Wafer Test – Arcing!



Townsend avalanche discharge

High Voltage Wafer Test – Arcing!

$$V_B = \frac{Bpd}{\ln(Apd) - \ln\left[\ln\left(1 + \frac{1}{\gamma_{se}}\right)\right]}$$



Ph.D. thesis, 1887

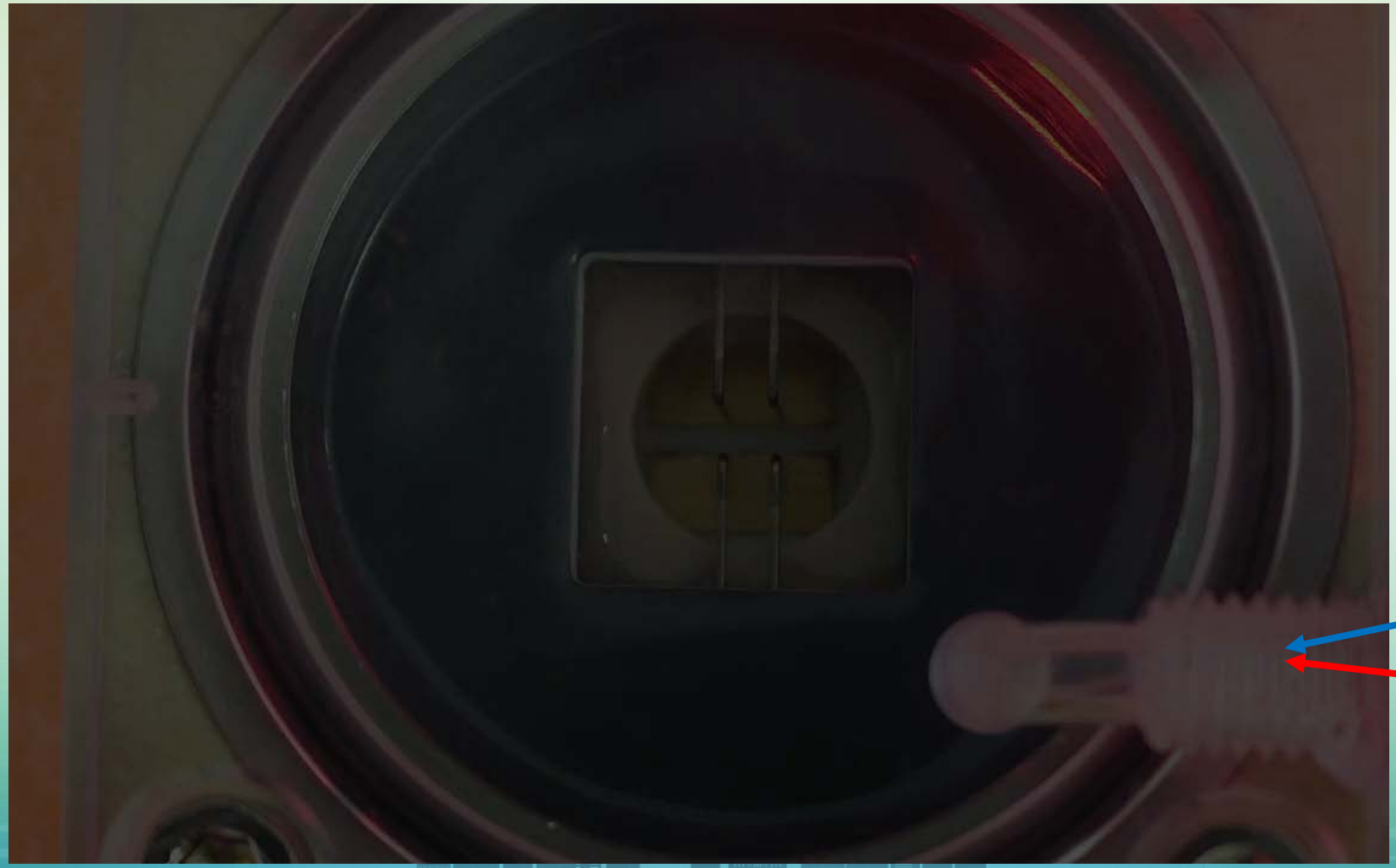
Friedrich Paschen *)

Paschen equation, Paschen curves:
breakthrough voltage (V_B) as a function of gas pressure (p)

*) picture source: Wikipedia

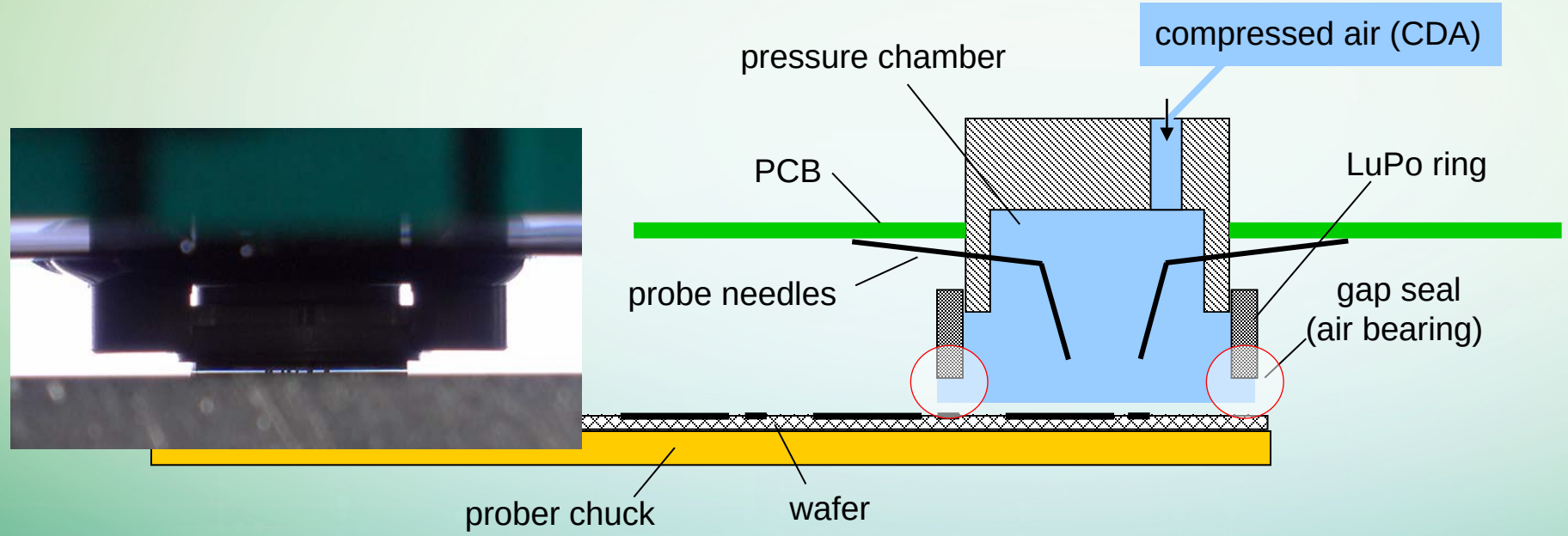
High Voltage Wafer Test – Arcing!

- Application of "Paschen Law"- TIPS HV "LuPo" probe card (pressure chamber)



High Voltage Wafer Test – Arcing!

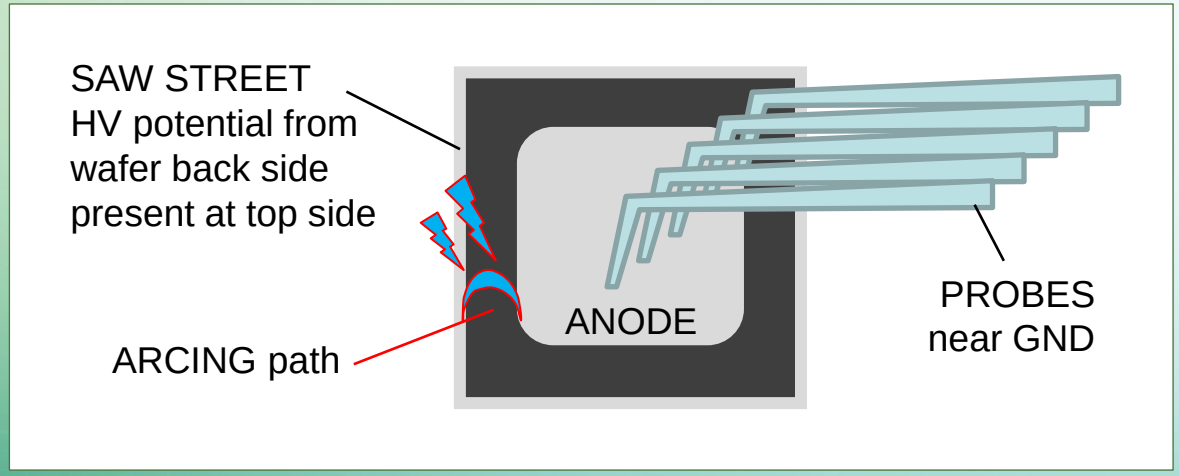
- TIPS "LuPo" HV probe card – how does it work



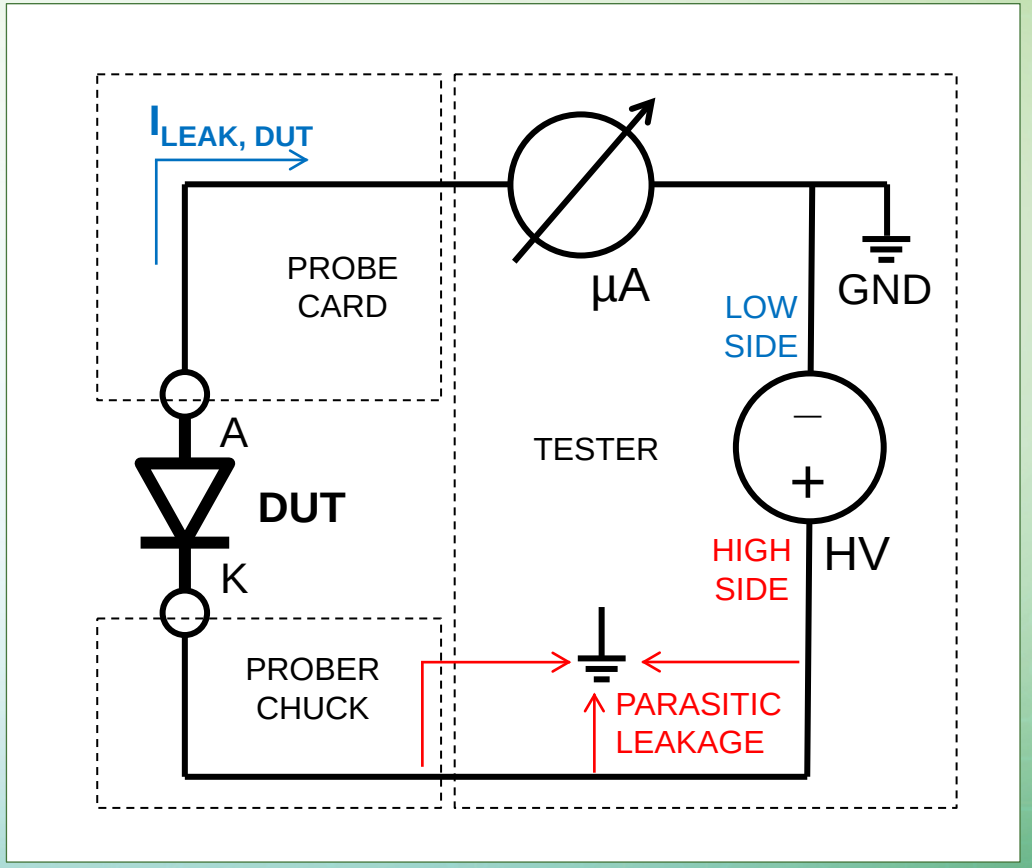
Considerations – Single vs. Multi site

A simple case study: HV Power Diode - reverse leakage current / blocking voltage – SINGLE SITE

- arcing risk from chip pad to saw street
- no arcing between needles (all at same potential near GND)
- I_{LEAK} measurement not affected by **parasitic** high side leakage to GND



Power diode – probe card contacting scheme



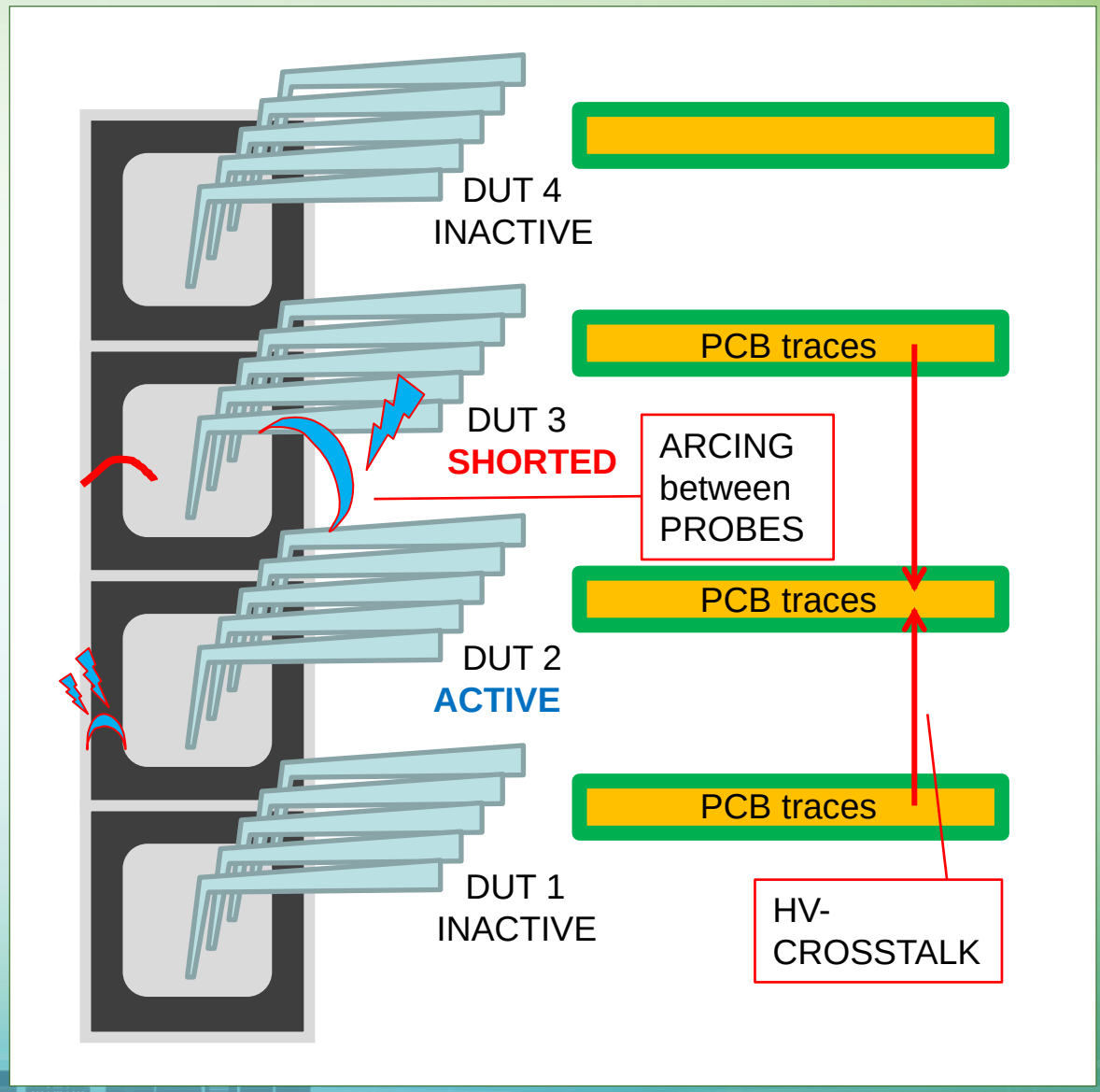
HV leakage test - simplified schematics

Considerations – Single vs. Multi site

HV Power Diode - MULTI-SITE Probe Card

- Additional arcing path between probes / sites !
- HV crosstalk from adjacent sites
- Safety aspects: traces present on probe card PCB, relay matrix that can be connected with HV High side

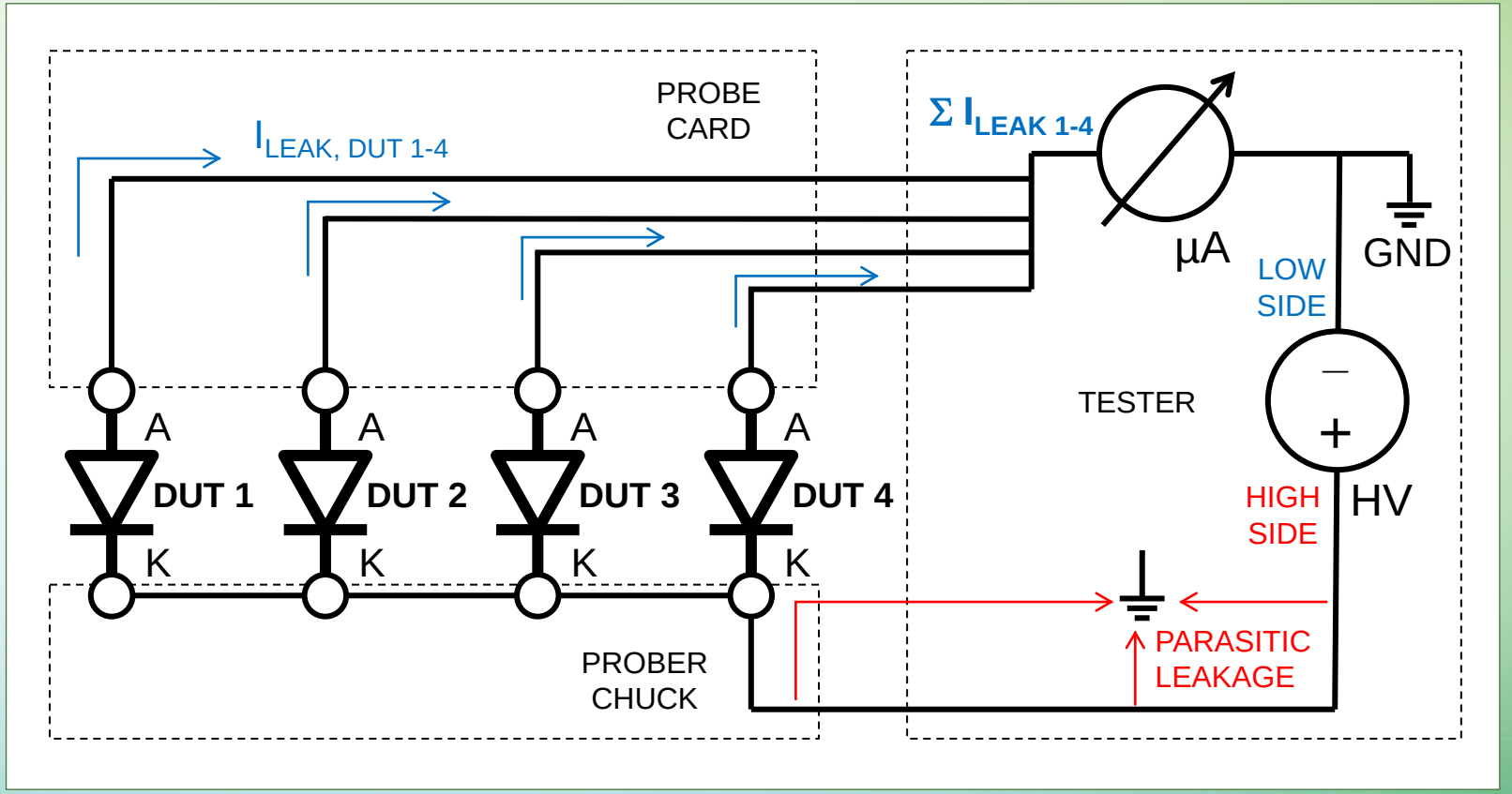
-> Can be avoided / minimized by
- proper probes layout using HV design rules
- appropriate PCB design techniques
- HV safety enclosure for prober / tester setup



Considerations – Multi-site, true parallel

HV – shorted DUT

- very fast (true parallel test)
- good if all 4 DUTs are good
- I_{LEAK} measurement not affected by parasitic high side leakage to GND



HV leakage test – multi-site, true parallel, simplified schematics

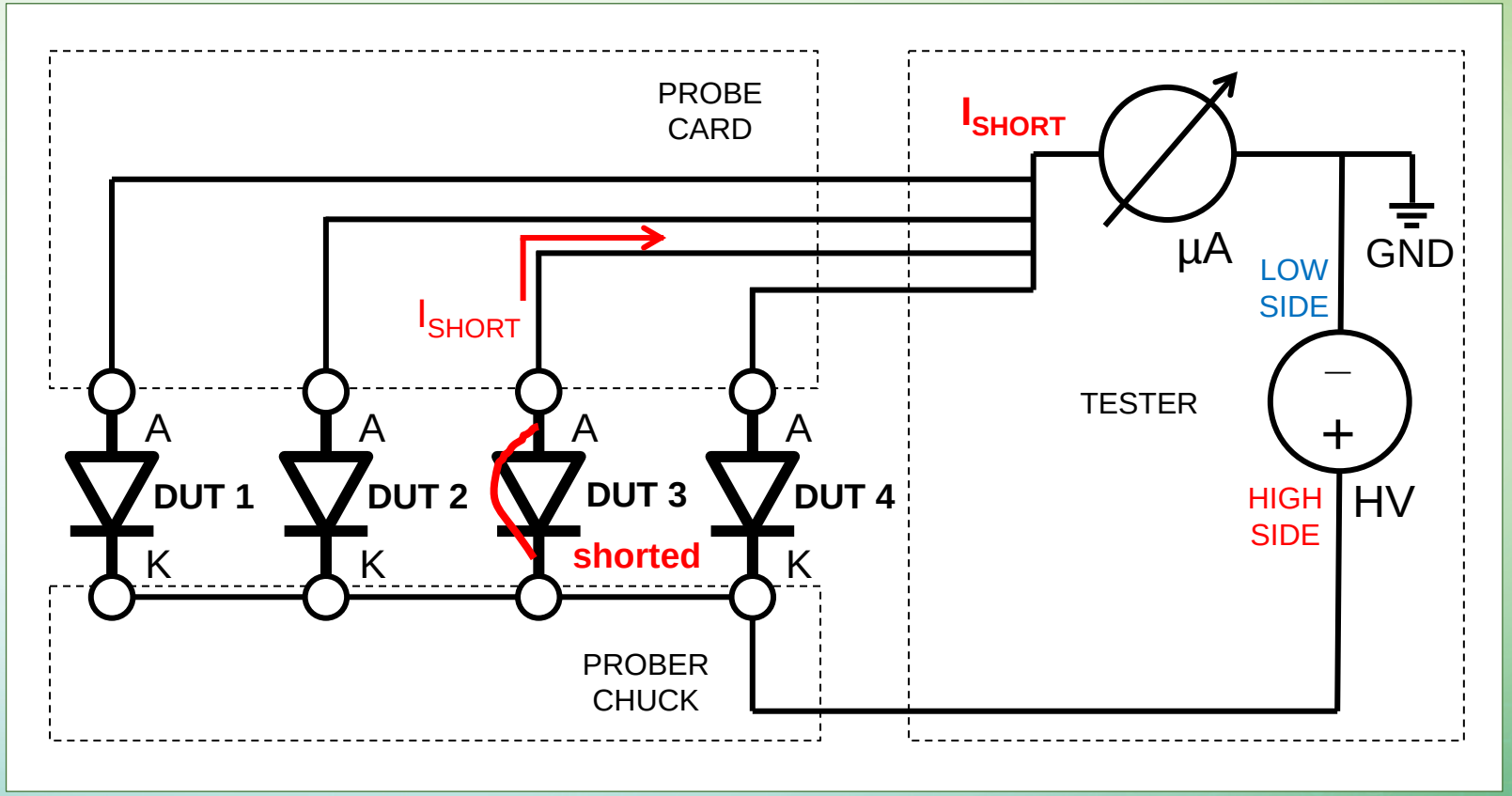
Considerations – Multi-site, true parallel

HV – shorted DUT

- very fast (true parallel test)
- good if all 4 DUTs are good
- I_{LEAK} measurement not affected by **parasitic** high side leakage to GND

BUT...

- if one DUT gets shorted, the other 3 DUTs can't be measured and being binned FAIL
- might mask high leak DUTs if others are low leak



HV leakage test – multi-site, true parallel, simplified schematics

Considerations – Multi-site, true parallel

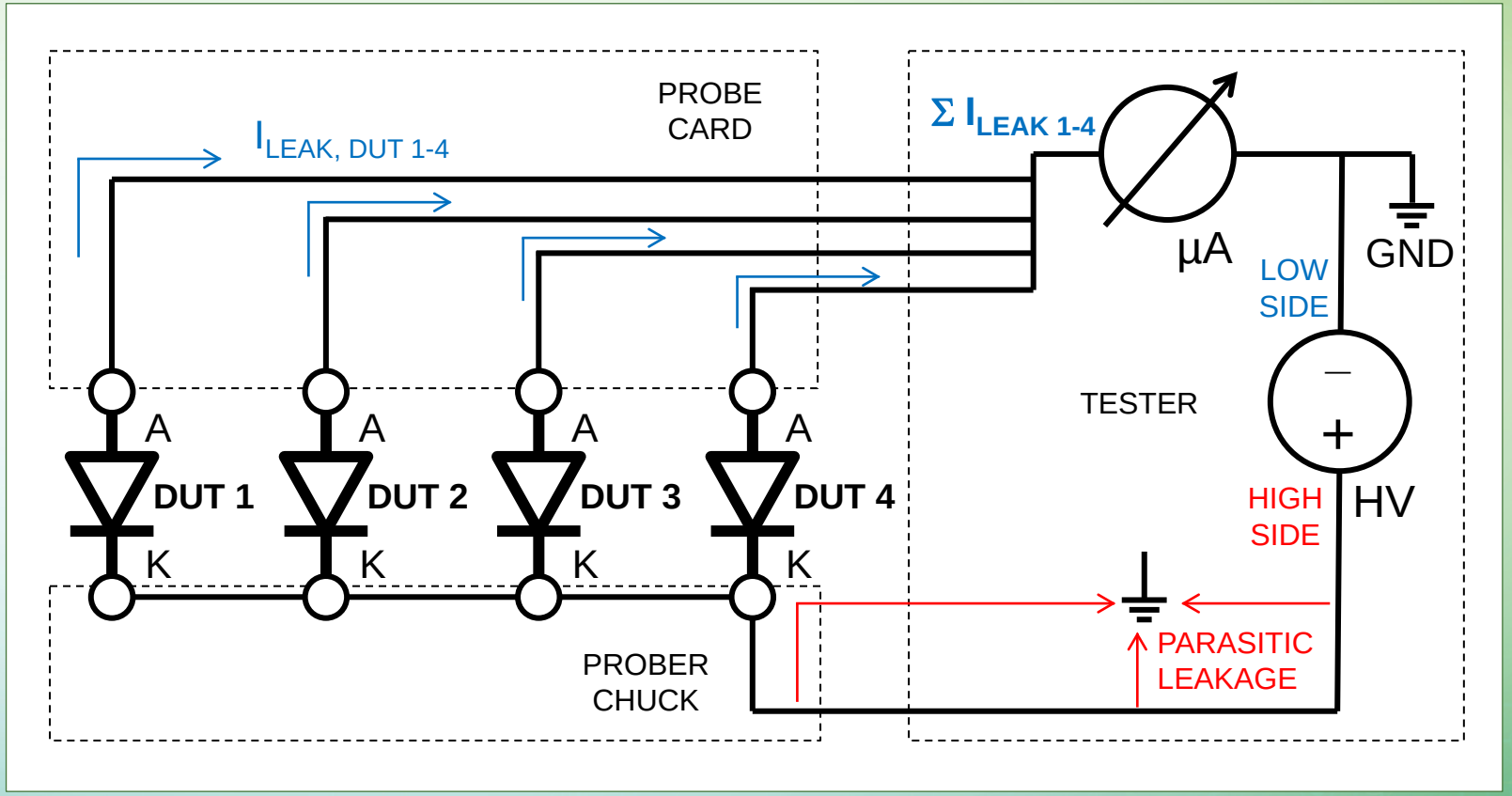
HV – shorted DUT

- very fast (true parallel test)
- good if all 4 DUTs are good
- I_{LEAK} measurement not affected by parasitic high side leakage to GND

BUT...

- if one DUT gets shorted, the other 3 DUTs can't be measured and being binned FAIL
- might mask high leak DUTs if others are low leak

-> Efficient wafer screening scheme for low DUT failure rates.



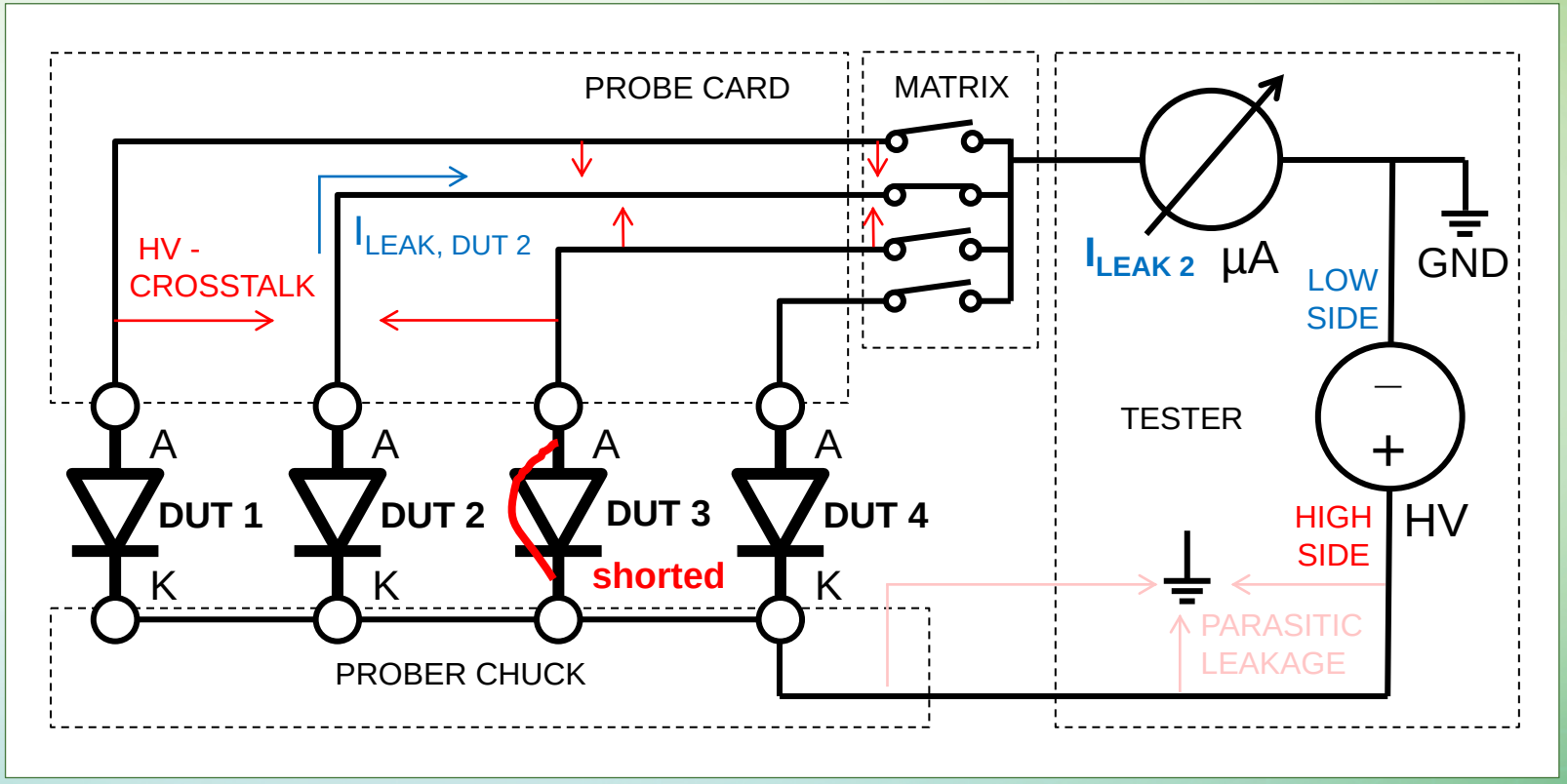
HV leakage test – multi-site, true parallel, simplified schematics

Considerations – Multi-site, sequential

HV Crosstalk

- accurate (each DUT tested individually)
- comparably slow (sequential test)
- I_{LEAK} measurement might be affected by **HV crosstalk** from neighboring sites (can be minimized by careful design)

-> Test scheme for accurate sorting at moderate to high DUT failure rates.



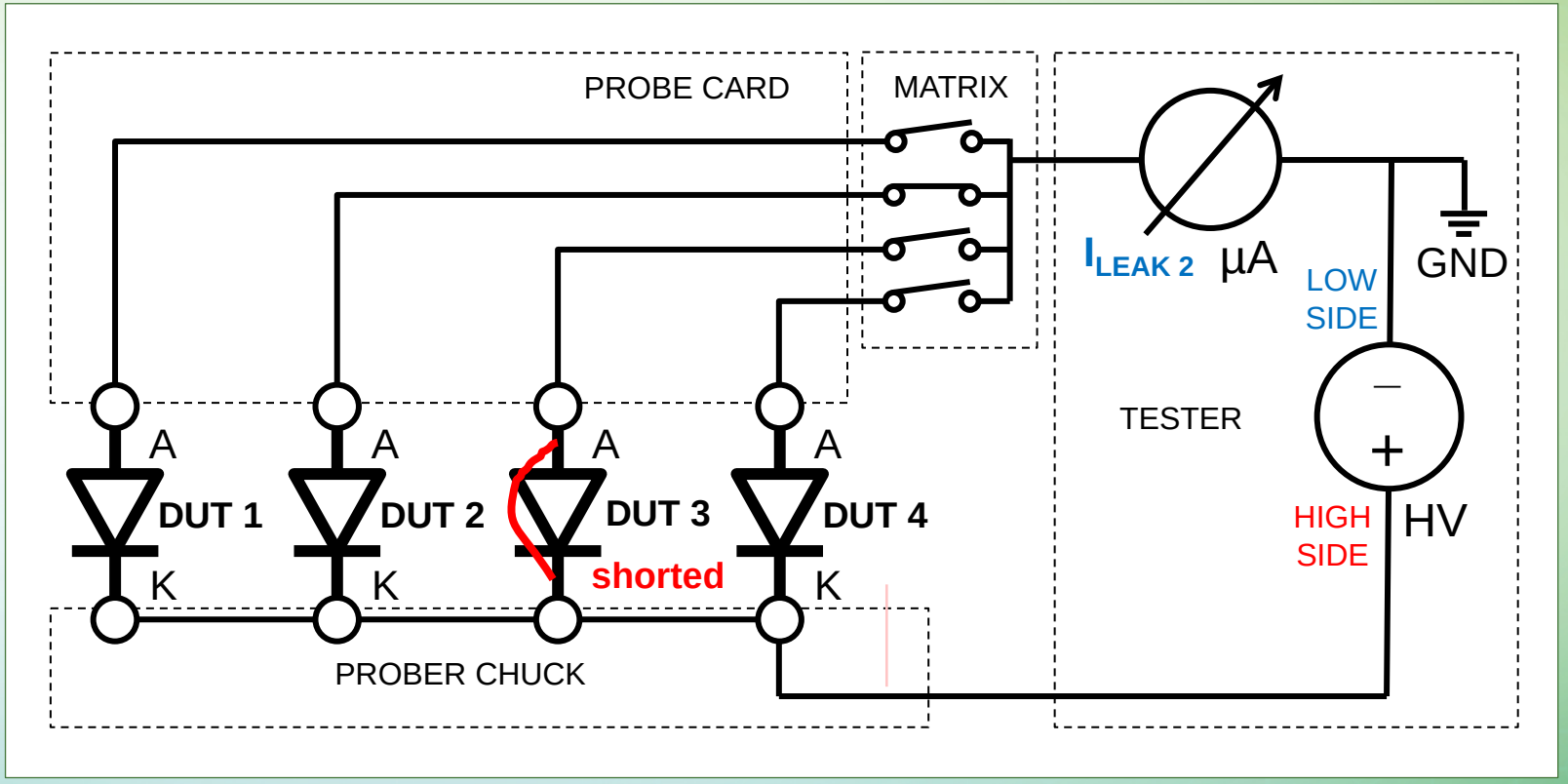
HV leakage test – multi-site, sequential, here: DUT 2 active, DUT 3 FAIL, shorted

Considerations – Multi-site, COMBO

COMBO parallel / sequential

- perform parallel test – very fast if all DUTs PASS:
- in case of parallel test FAIL -> test each DUT sequentially

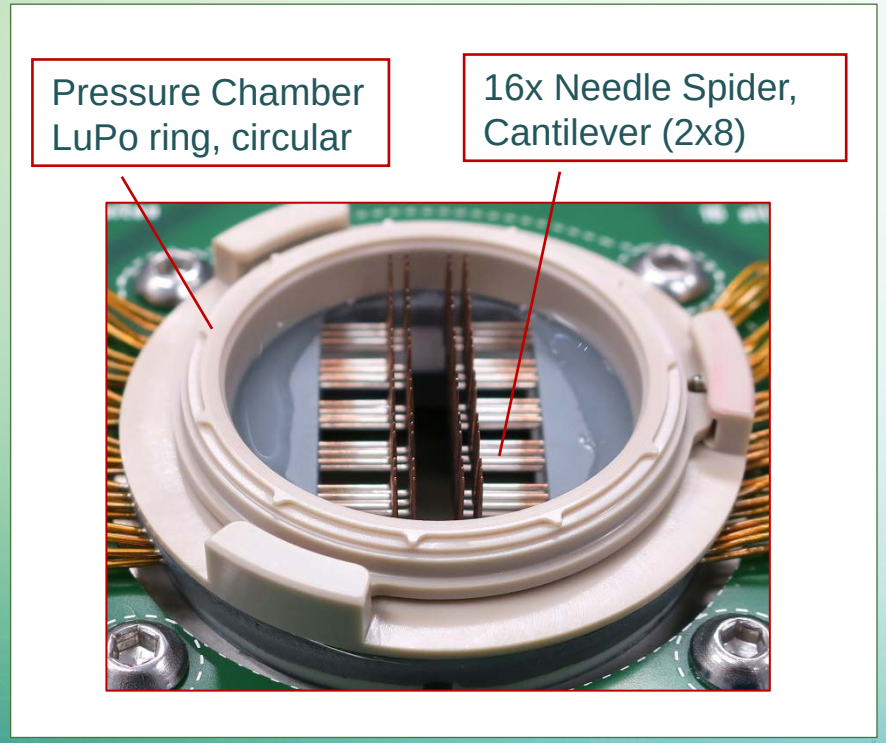
-> Most efficient test scheme, requires some efforts in test programming...

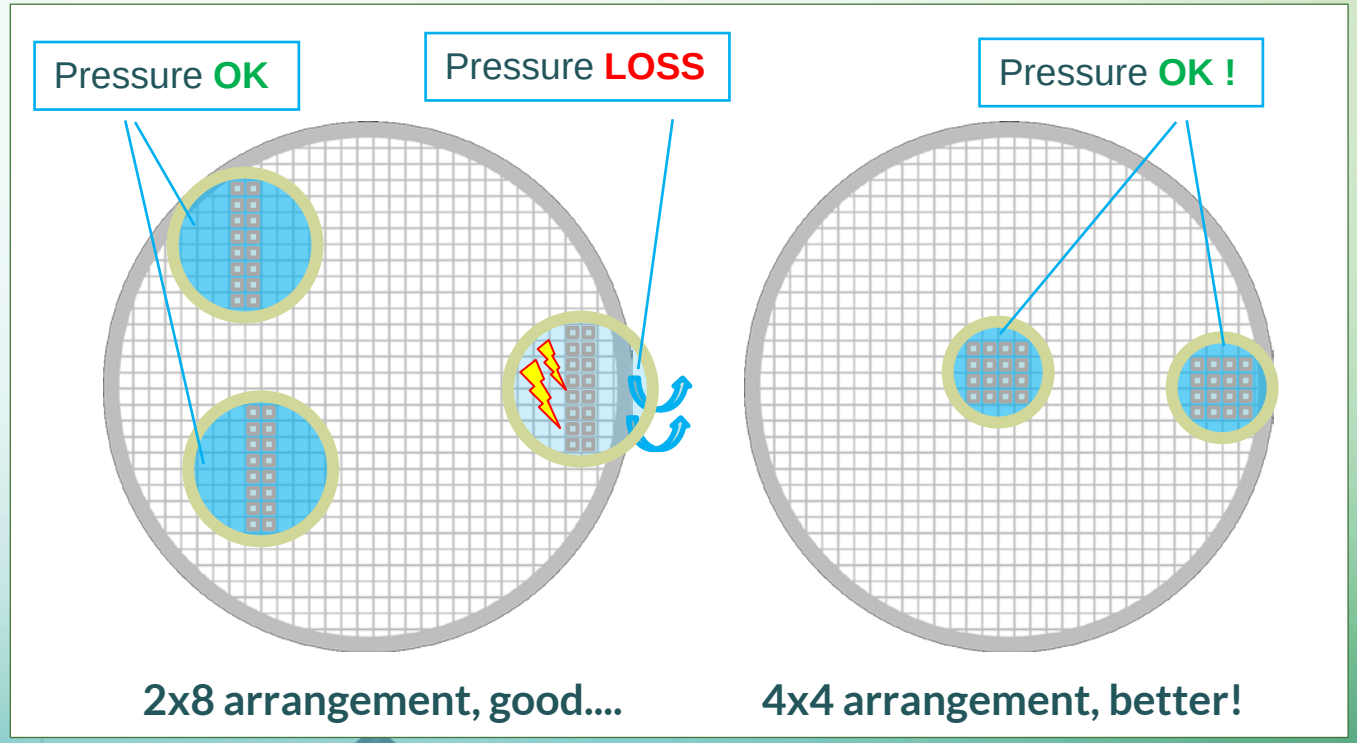


HV leakage test – multi-site, sequential, here: DUT 2 active, DUT 3 FAIL, shorted

Wafer edge: Test coverage / Probe card design

- TIPS HV "LuPo" probe cards: the pressure chamber towards the wafer ("LuPo-ring") has a circular footprint.
- Depending on multi-site DUT arrangement there might be a certain "overhang" of the pressure chamber w.r.t. DUT arrangement
- This might lead to non-testable chips near the wafer edge as the pressure chamber "hangs over" the wafer edge compromising with pressure build-up in the chamber.

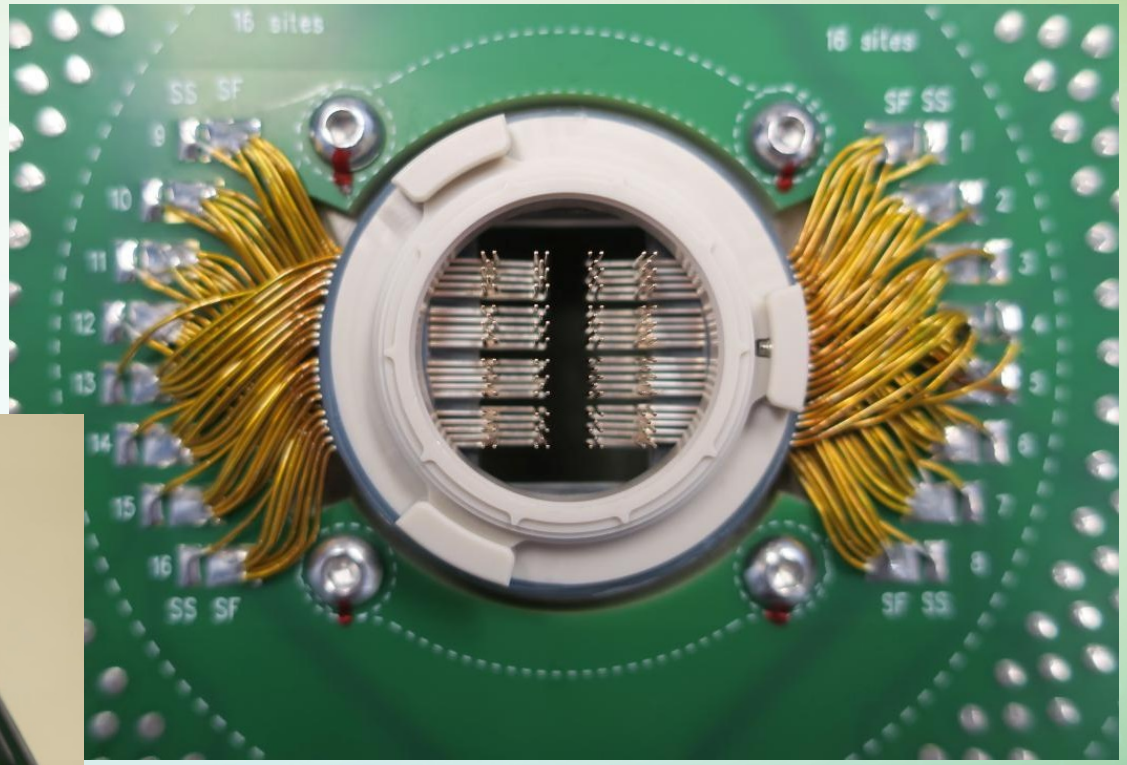


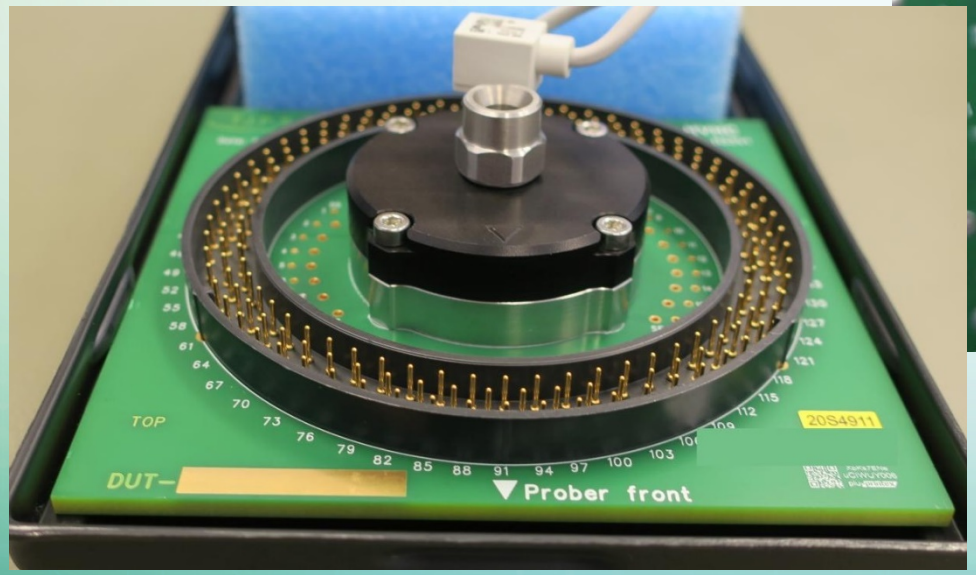


The "real" thing..... (1)

16x HV - Cantilever Probe Card

- SiC diode, 1.6 kV, 45 A
- 4x4 arrangement
- chamber pressure: 2.6 bar
- auto compressed air docking
- chamber pressure monitor

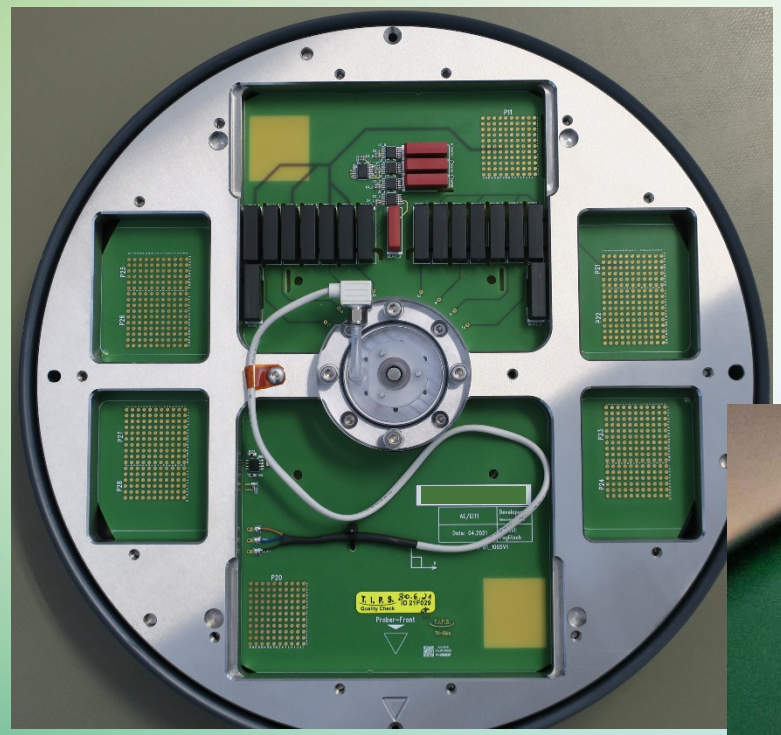


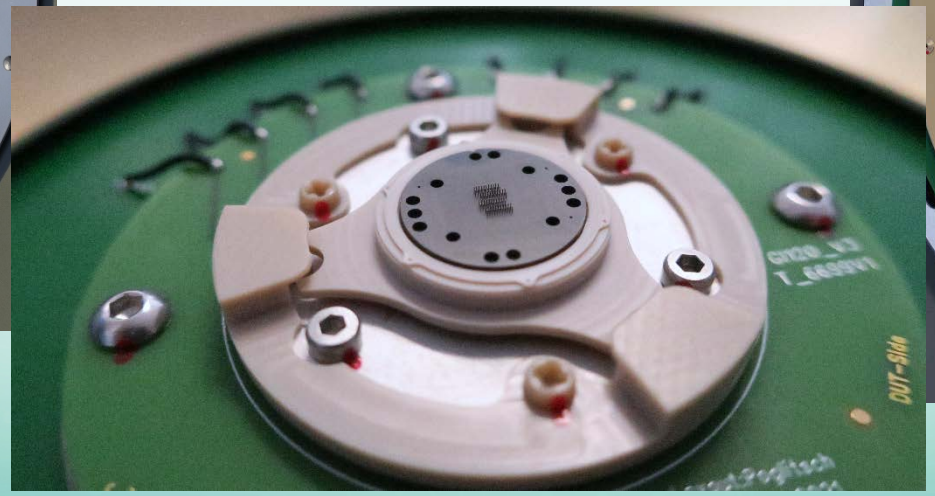


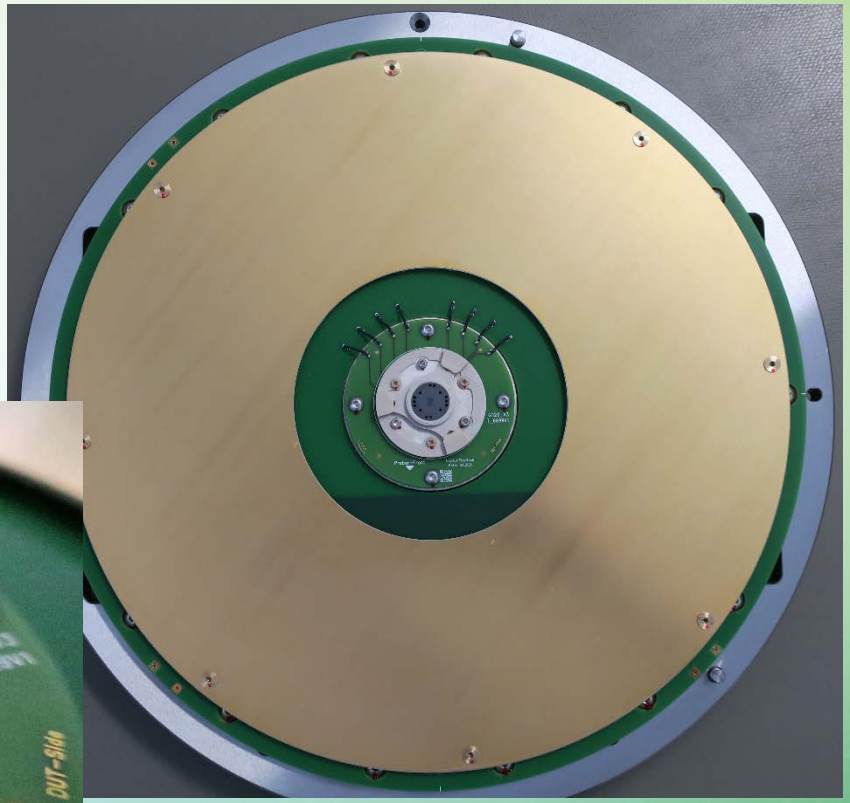
The "real" thing..... (2)

4x LuPo HV - Vertical Probe Card

- HV capacitor array, 2.2 kV
- 1x4 arrangement
- chamber pressure: 5 bar
- chamber pressure monitor
- "COMBO" multi-site test arrangement



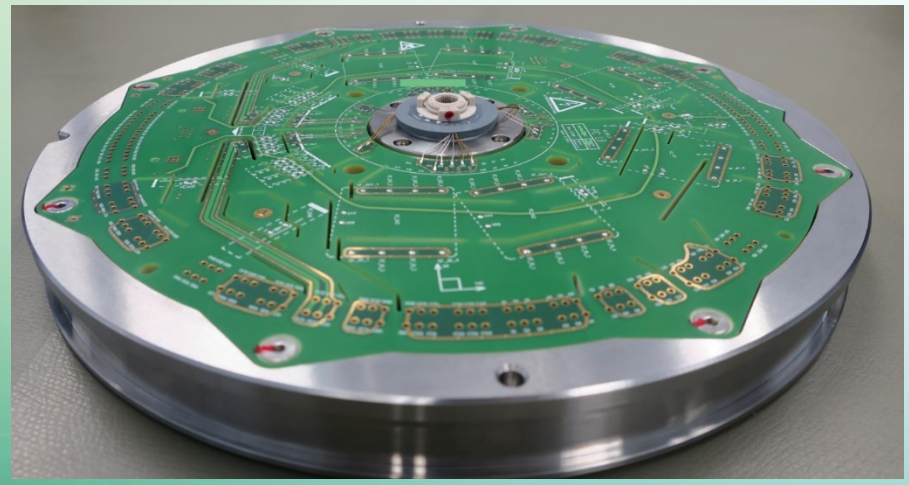


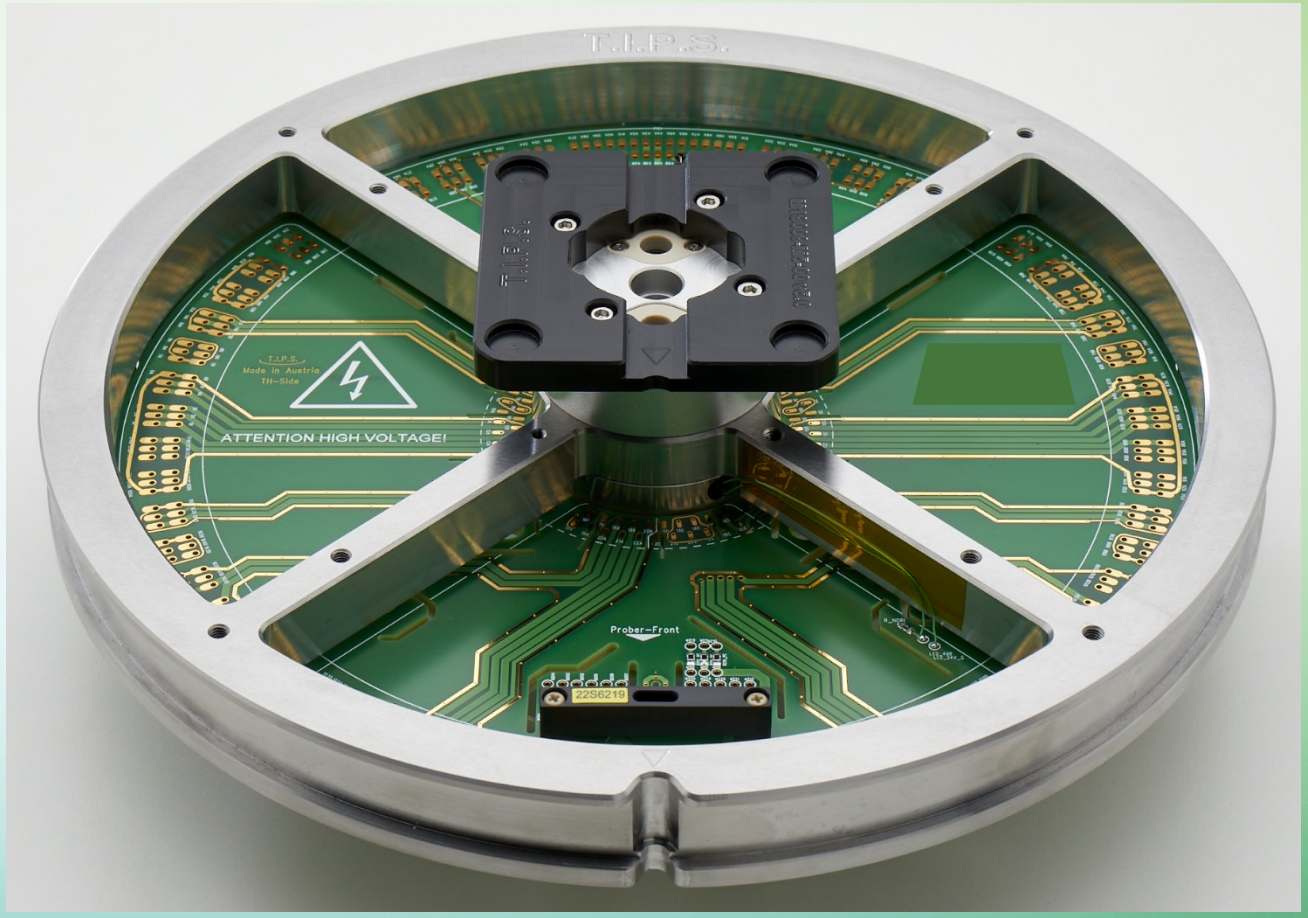


The "real" thing..... (3)

2x LuPo HV – Cantilever Probe Card

- IGBT, 3.5 kV, 100 A
- 1x2 arrangement
- low leakage HV PCB design
- auto compressed air docking
- optical arc detection
- automatic probe card changer (APC)





Summary and Outlook

- Multi-site probing for High-Voltage power devices successfully introduced for high volume mass production wafer test at several customers
- Multi-site arrangements optimized for best test coverage
- "Paschen" based HV probe card technology extended to SiC, GaN
- Fully integrated into automated probe card changer (APC) capable probers

...next steps:

- LuPo "Gen4" technology: higher chamber pressure, less CDA consumption, use of additive manufacturing techniques ("3D printing")...
- Rectangular pressure chambers for better wafer edge test coverage...?

....stay tuned!

Acknowledgements

- T.I.P.S.' design and production team in Villach, Austria
- Unnamed customers striving for "leading edge" power device probing ....
- ....and the well-respected auditorium for listening!

Thank You!