SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

Flying Probe Card Design for medical and other challenging applications

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SPEA

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Overview

1. Trends for Complex Silicon Design

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- 1.1.1 Tessellation
- 1.1.2 Maximize the use of Wafer Area

1.2 VERTICAL OPTIMIZATION

- 1.2.1 Double-Sided Wafers
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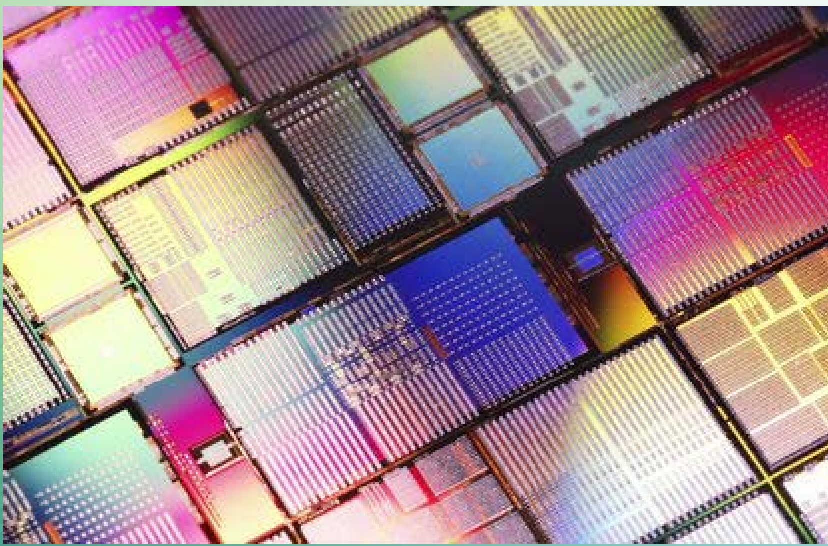
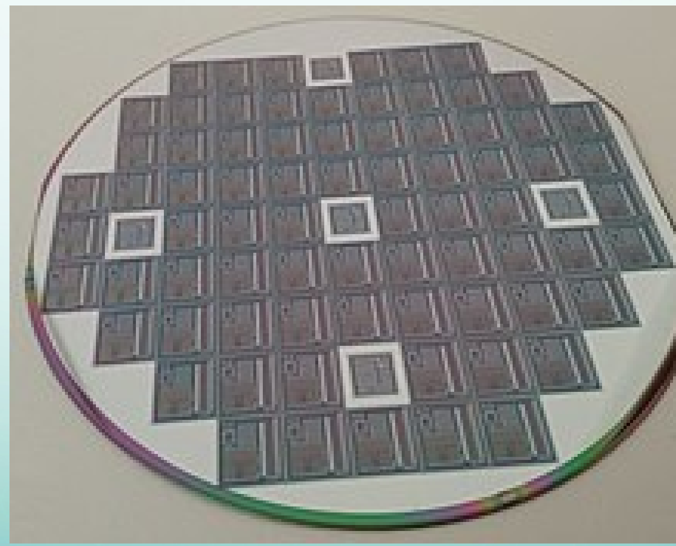
Trends for Complex Silicon Design

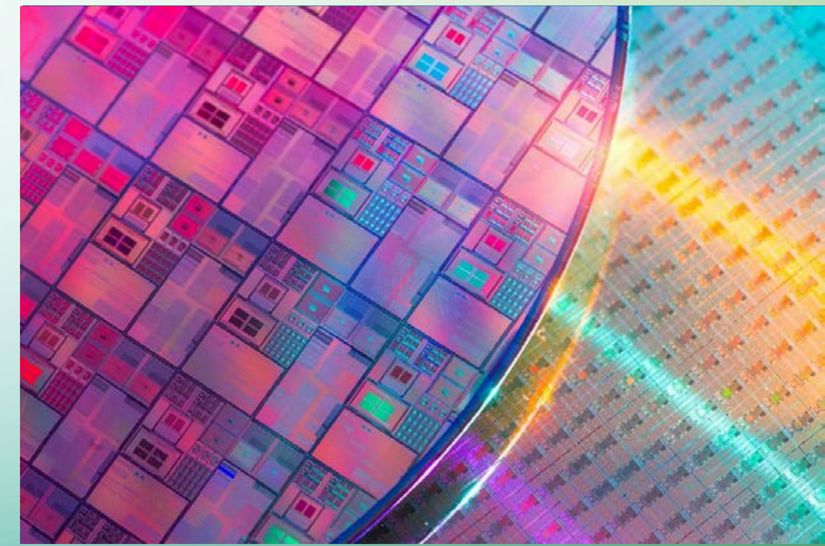
For complex applications, the need to reduce costs and maximize yield is driving a more efficient use of the semiconductor Silicon.

Two types of optimizations are possible:

- Planar Silicon Optimization
- Vertical Silicon Optimization







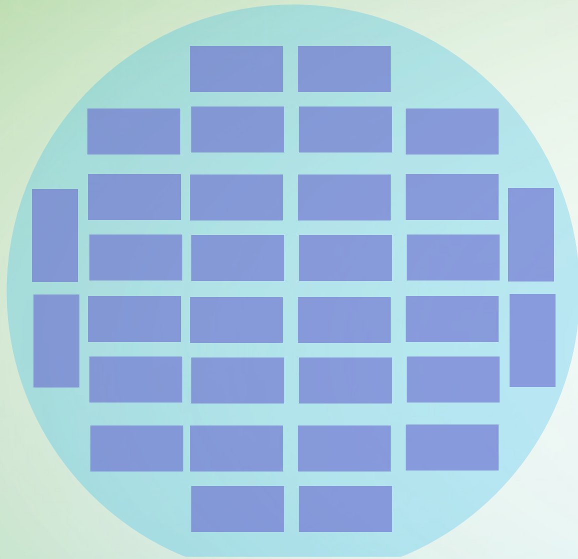
PLANAR SILICON OPTIMIZATION

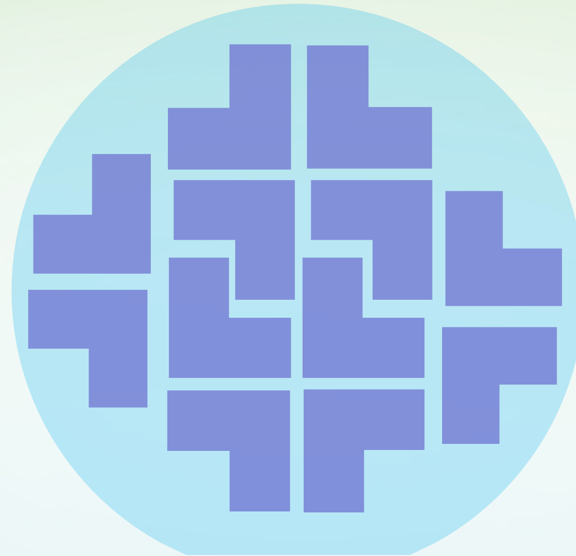
Tessellation

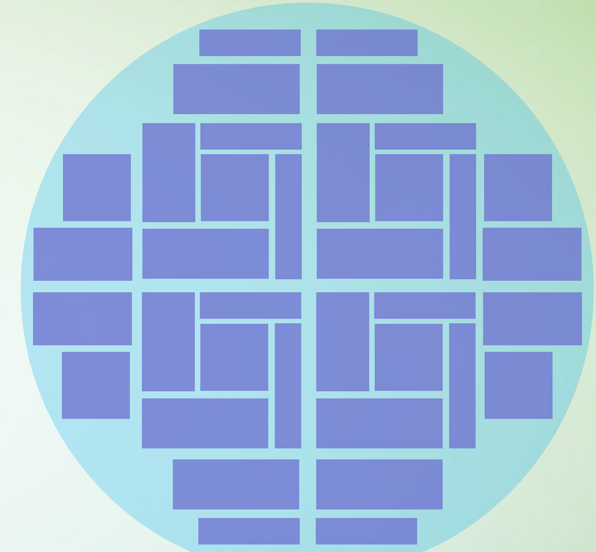
Technique to use all the planar space available with non-square shapes.

M.C. Esher

Maximize the use of Wafer Area





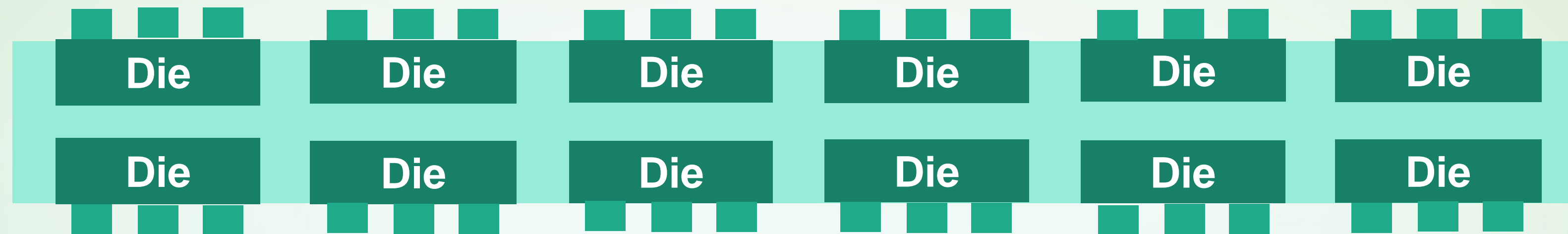


- Non-square dies
- Uneven geometries
- Diversified die orientation
- Multi-Project Wafers (MPW)

VERTICAL SILICON OPTIMIZATION

Double Sided Wafers

Double-sided wafer with single side dies:

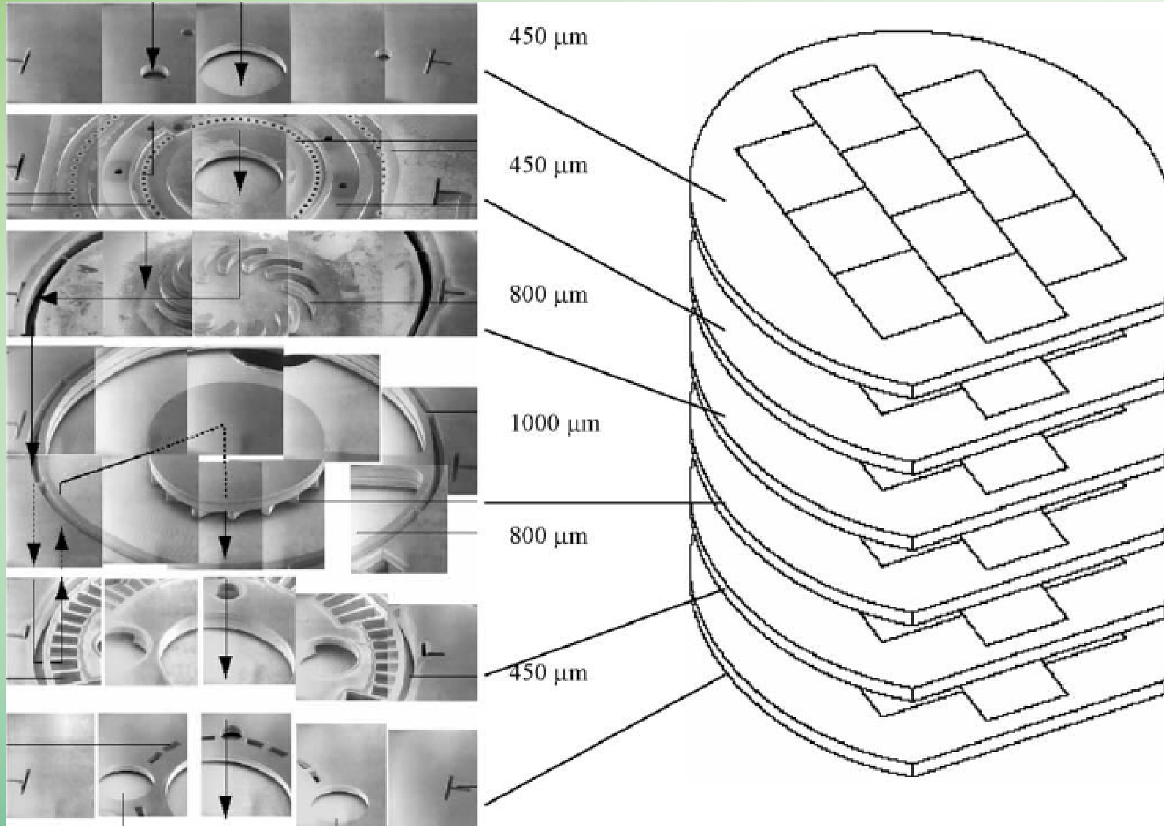


Section view

Double-sided wafer with pass-through dies:

Section view

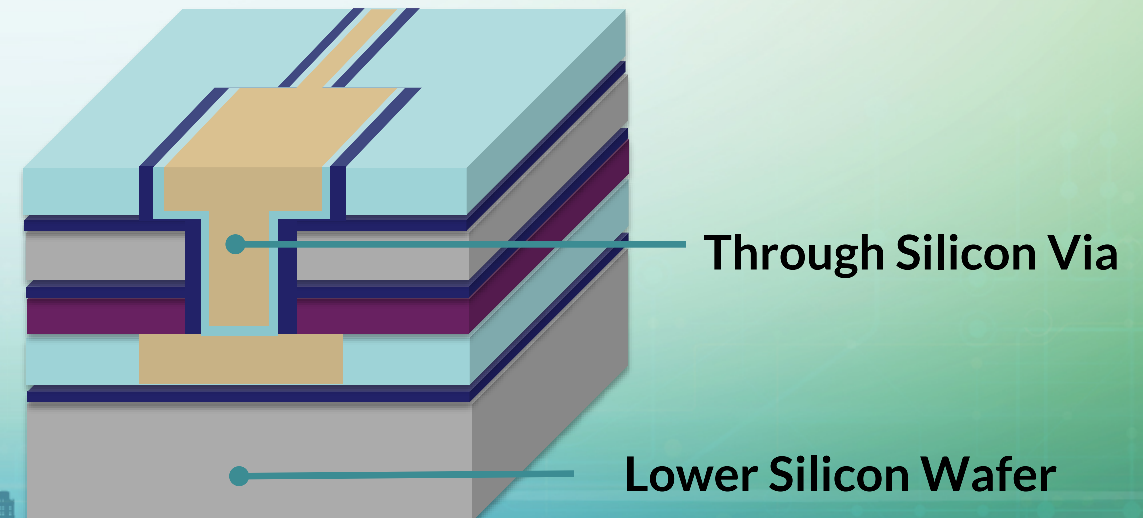
Multilayer Structures



An example of wafer stack schematics for a MEMS device.

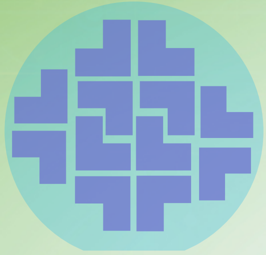
(Source: Miki, Norihisa & Zhang, Xin & Khanna, Rajat & Ayon, Arturo & Ward, D. & Spearing, S., A study of multi-stack silicon-direct wafer bonding for MEMS manufacturing. 407 – 410)

- **Wafer bonding techniques enable the fabrication of vertically interconnected multilayer stacks**
- **Silicon-top-silicon, or varied materials (glass, …)**
- **Advantages in performance, form factor, and integration**

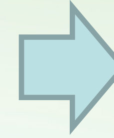


IMPACT ON TESTING PROCESS

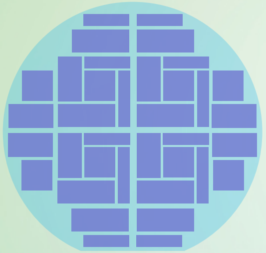
Impact on Testing Process



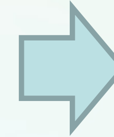
- Unconventional die shape and pattern orientation



Cannot be tested with standard prober



- Multi-Project Wafers



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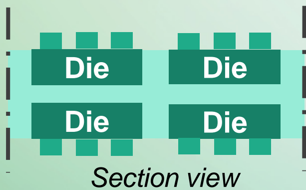
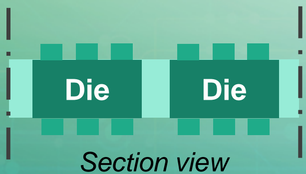


- Double-sided wafer with single side dies

Requires 2 insertions on standard prober



- Double-sided wafer with pass-through dies

Cannot be tested with standard prober

Standard Probing Architecture

ATE TEST HEAD

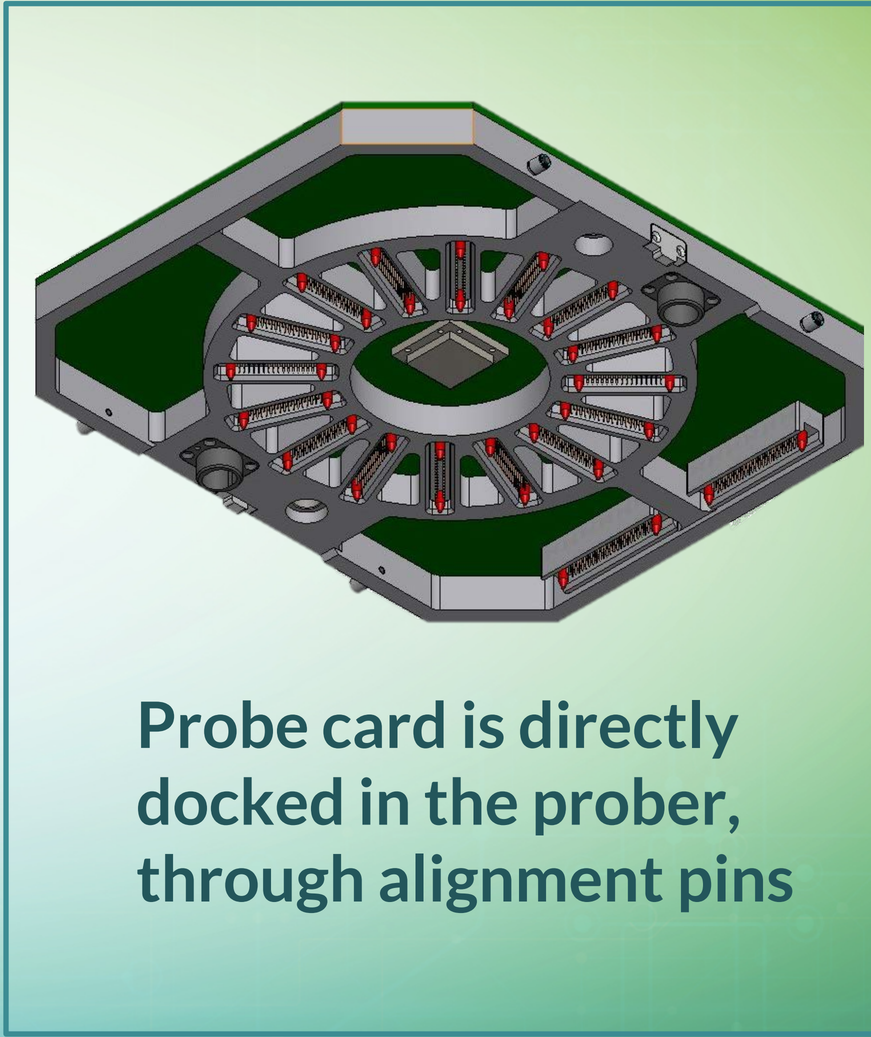
PROBE CARD

Probe Card Needle Tips

Wafer

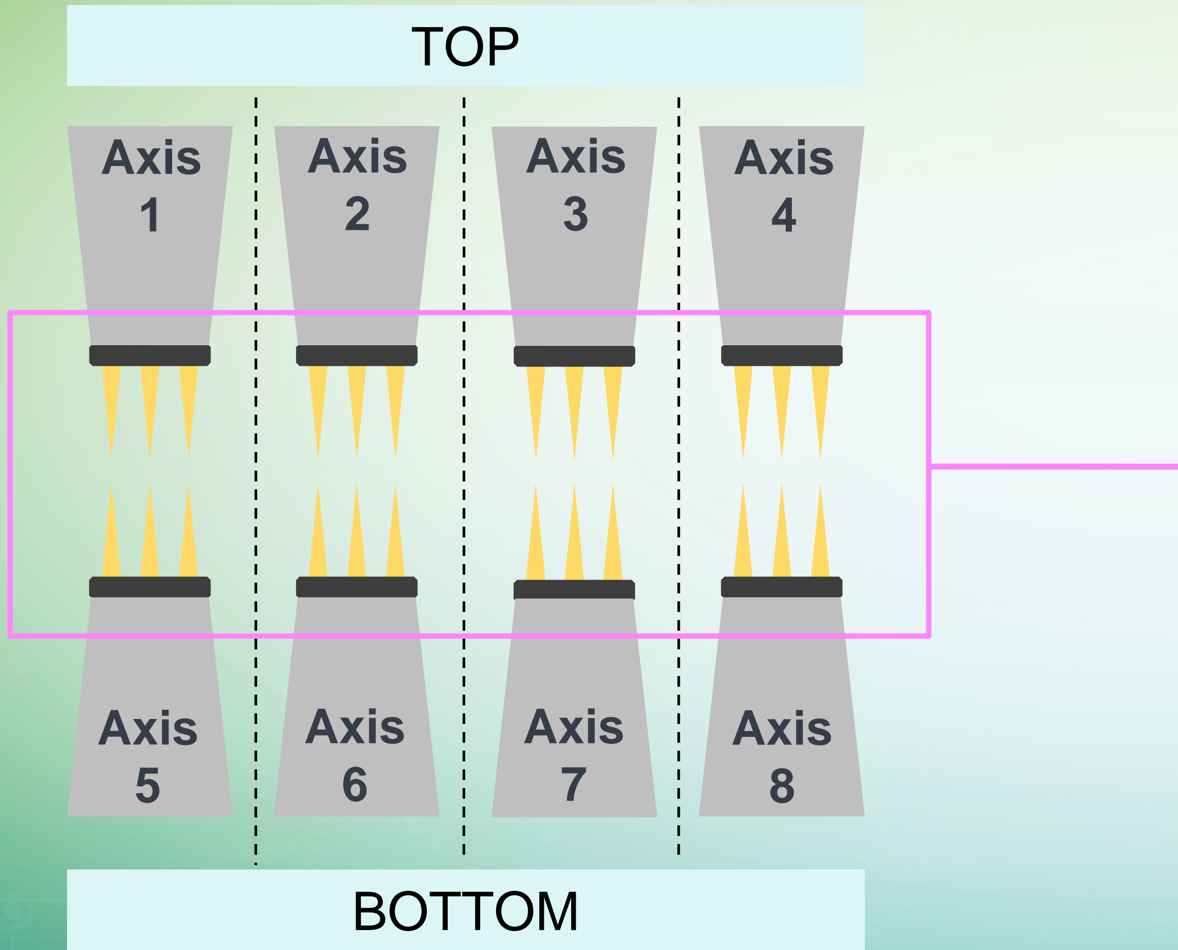
WAFER CHUCK

PROBER



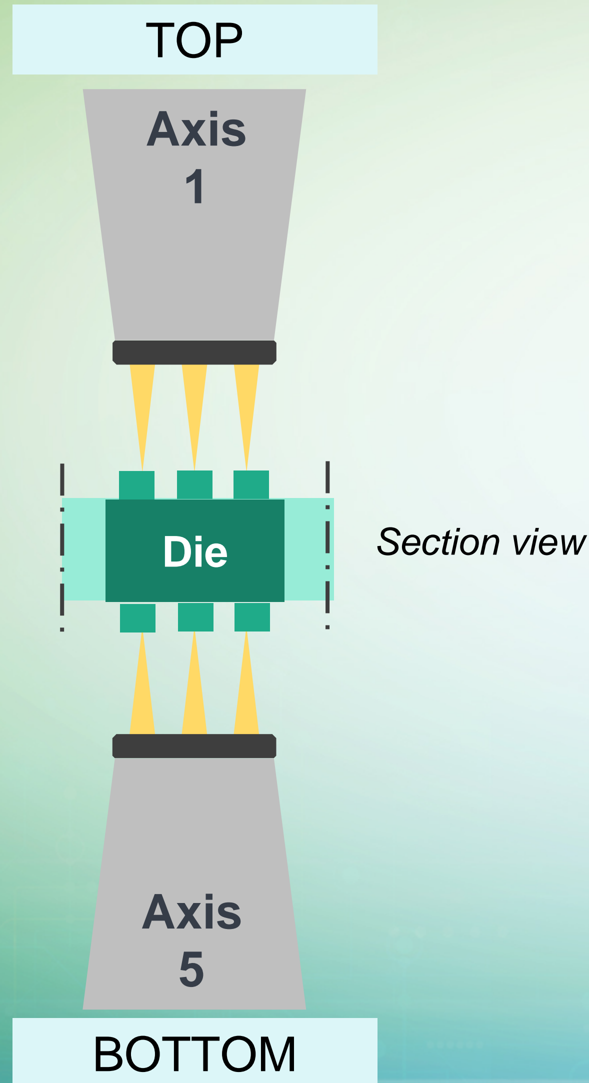
Probe card is directly docked in the prober, through alignment pins

Multiple Mobile Probe Cards



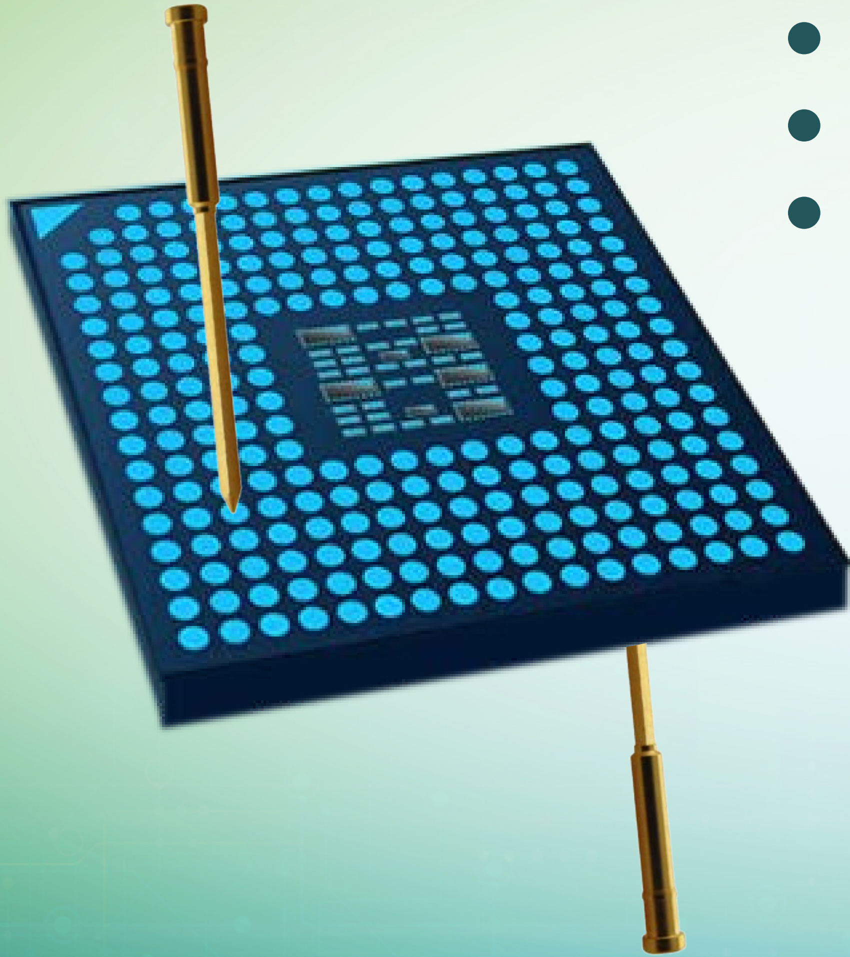
- 8 different small probe cards (4 Top + 4 Bottom)
- Each probe card can have a different design, to address any die density / shape / map
- Each probe card is moved on XYZ by an independent prober axis

Probing on Both Wafer Sides

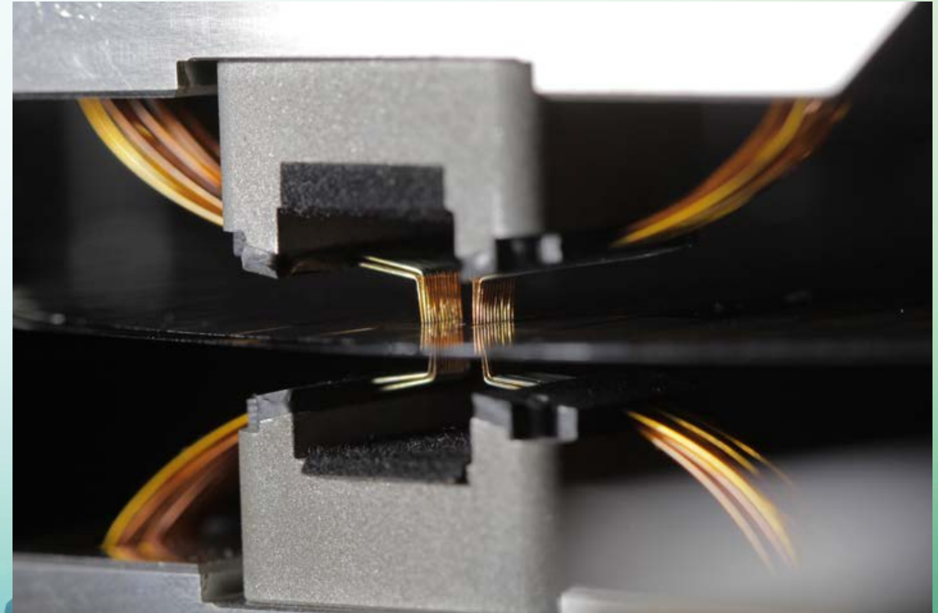


- Possibility to contact a pad from both sides simultaneously:
  - Continuity Test of Pass-Through Dies
  - Test of Multi-Layer Wafers (top-top, bottom-bottom, top-bottom)
  - “Virtual KGD Test” with high-accuracy measurements

Top-Bottom Continuity Test

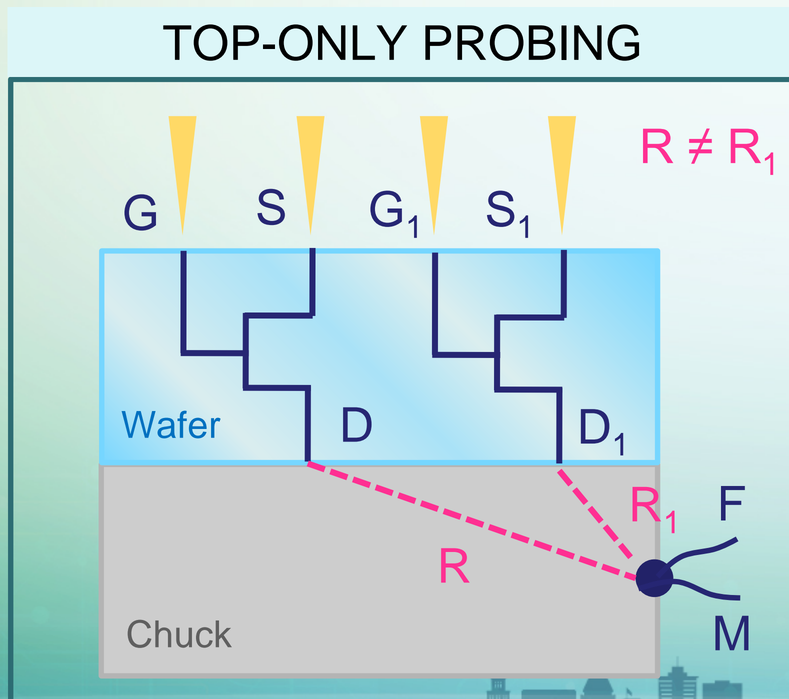


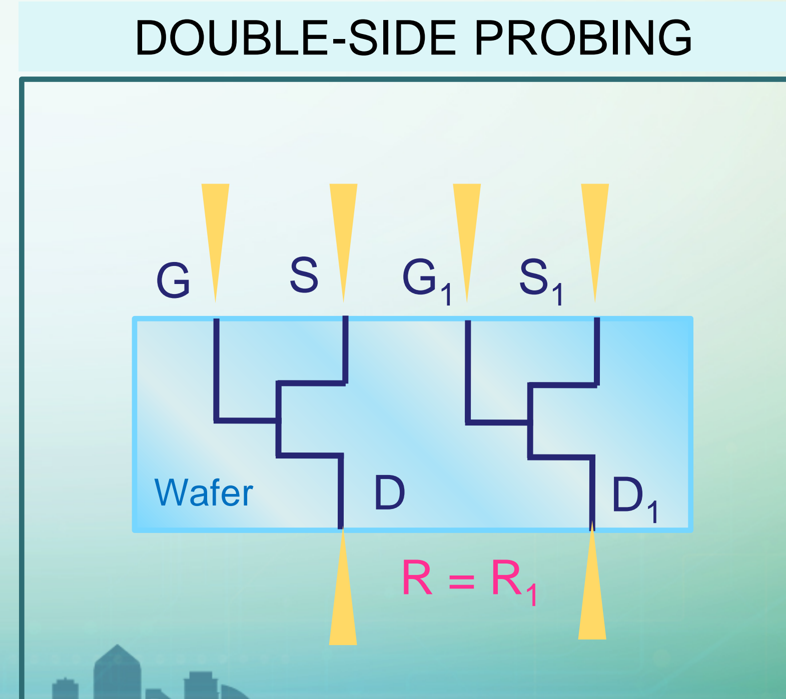
- Top-Bottom continuity test of all pads
- Resistance range from uOhm to GOhm
- Capacitance range from pF to mF



"Virtual KGD Test"

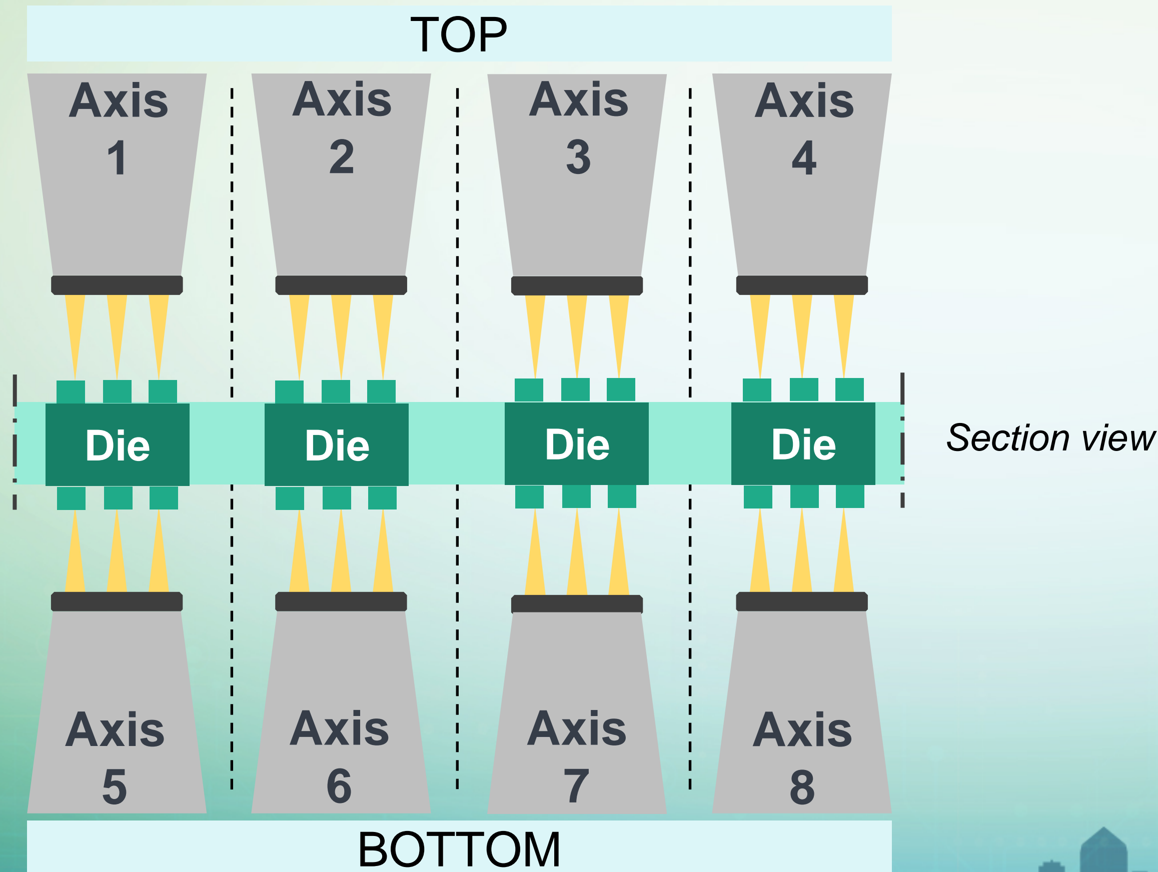
- Possibility to contact a pad from both sides simultaneously makes it possible to perform a "virtual KGD test" on power devices:
  - Extreme accuracy in resistance test (e.g. dRDSon), as the current path length is the same for all dies (chuck influence is eliminated)





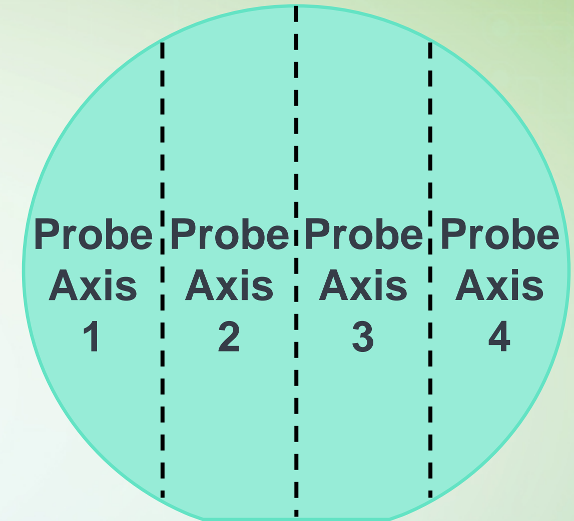
Parallel Double-Side Test

4 identical couples of probe cards (1 top + 1 bottom) can test different areas of the wafer at the same time, on both sides.

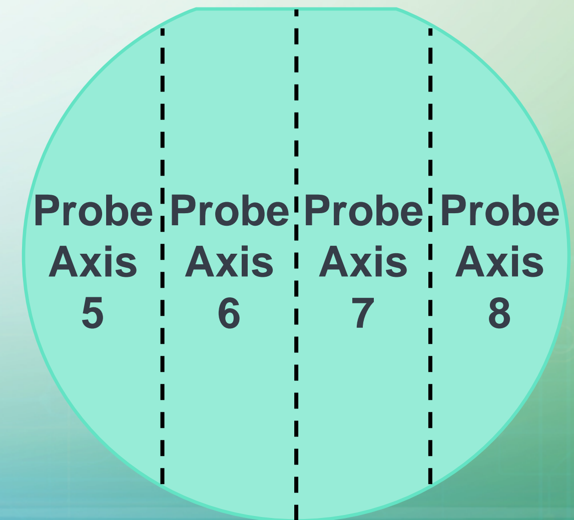


Section view

Top View

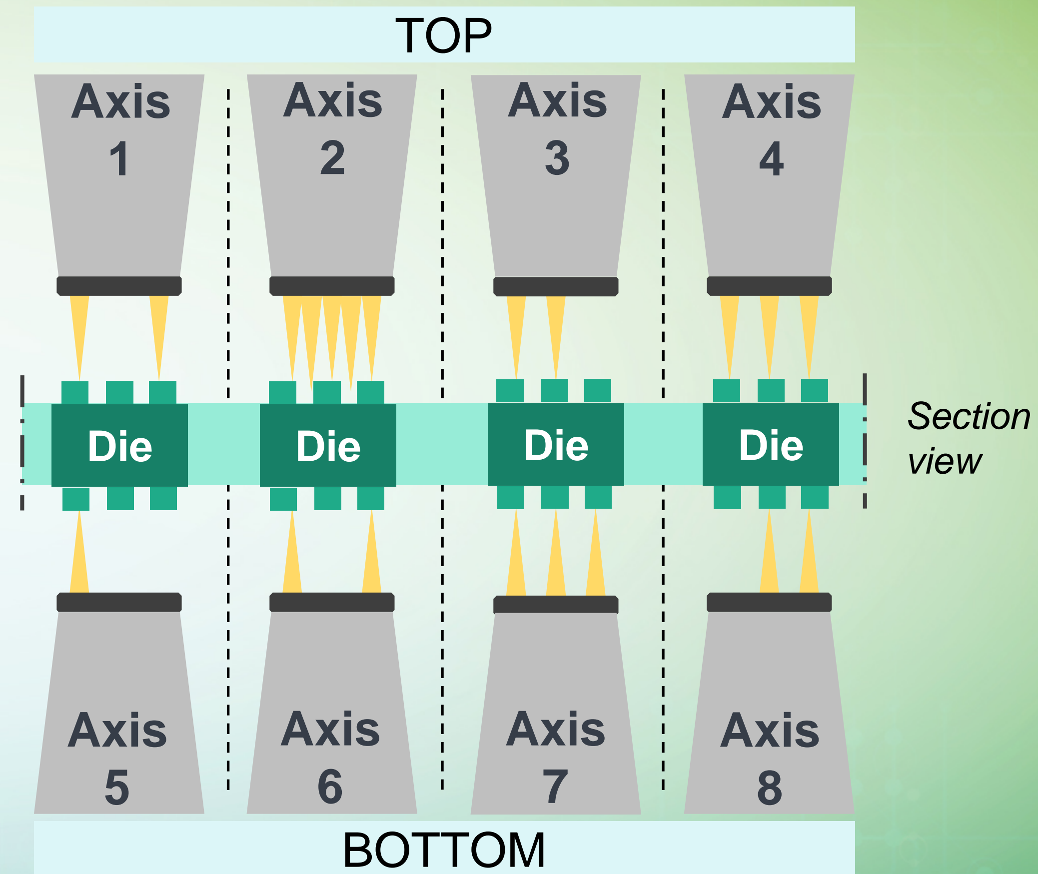


Bottom View



Varied Probe Card Layouts

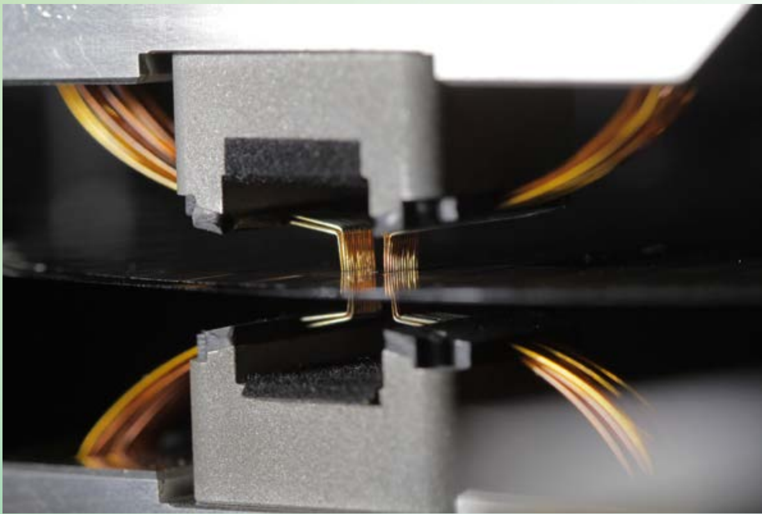
- The possibility to mount different probe card designs for the different axes allows for:
  - Single passage for both control pattern test and pad test
  - Test of multi-project wafer (every axis can mount the probe card for a specific device)
  - Test of wafers with uneven geometries (e.g. mirrored or rotated layouts for the different dies)
- In this case, every probe card perform a specific test function, with a proper probing layout, on the whole wafer area or in a portion of the wafer

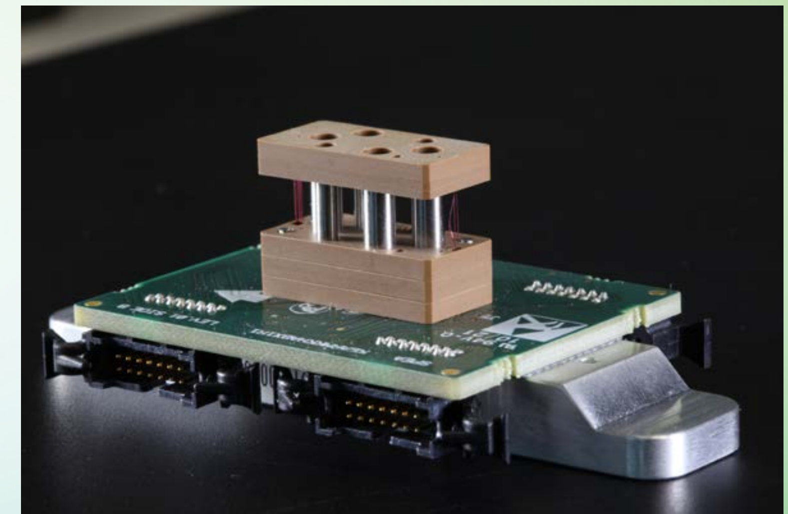


As the double-side probing on a single die can be performed with any combination of top axis / bottom axis, wafer layout design is not limited by "design for testability" rules.

Probe Card Technologies

- **Different technologies for the mobile probe cards are suitable for different applications**





Cantilever probe
- High-Current (512+A)
- For discretes, Diodes, Transistors…

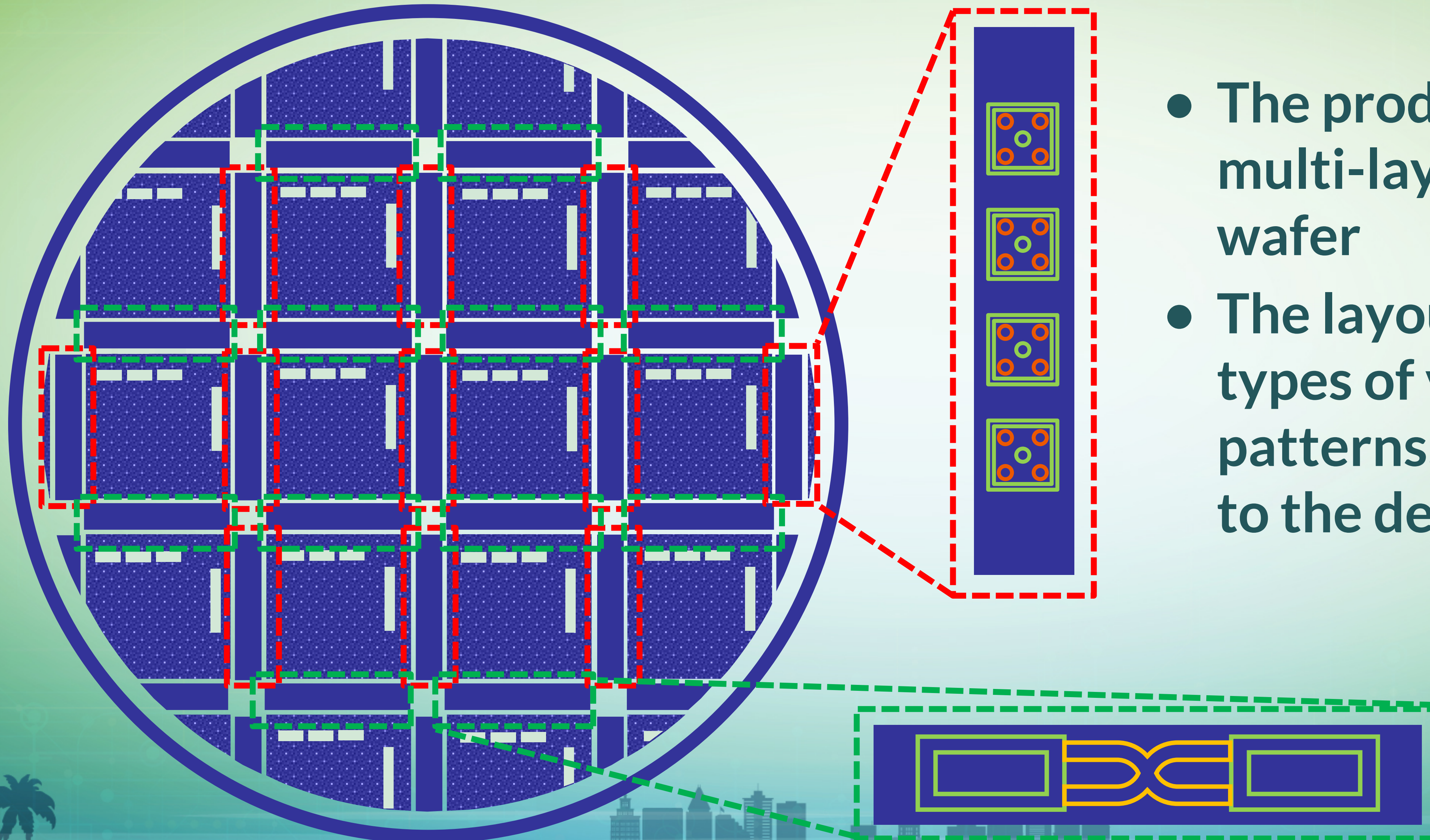
Vertical probe
- 150um Pitch
- For digital devices with short distance between pads

Wiring probe
- 40um Pitch
- For digital devices with short distance between pads

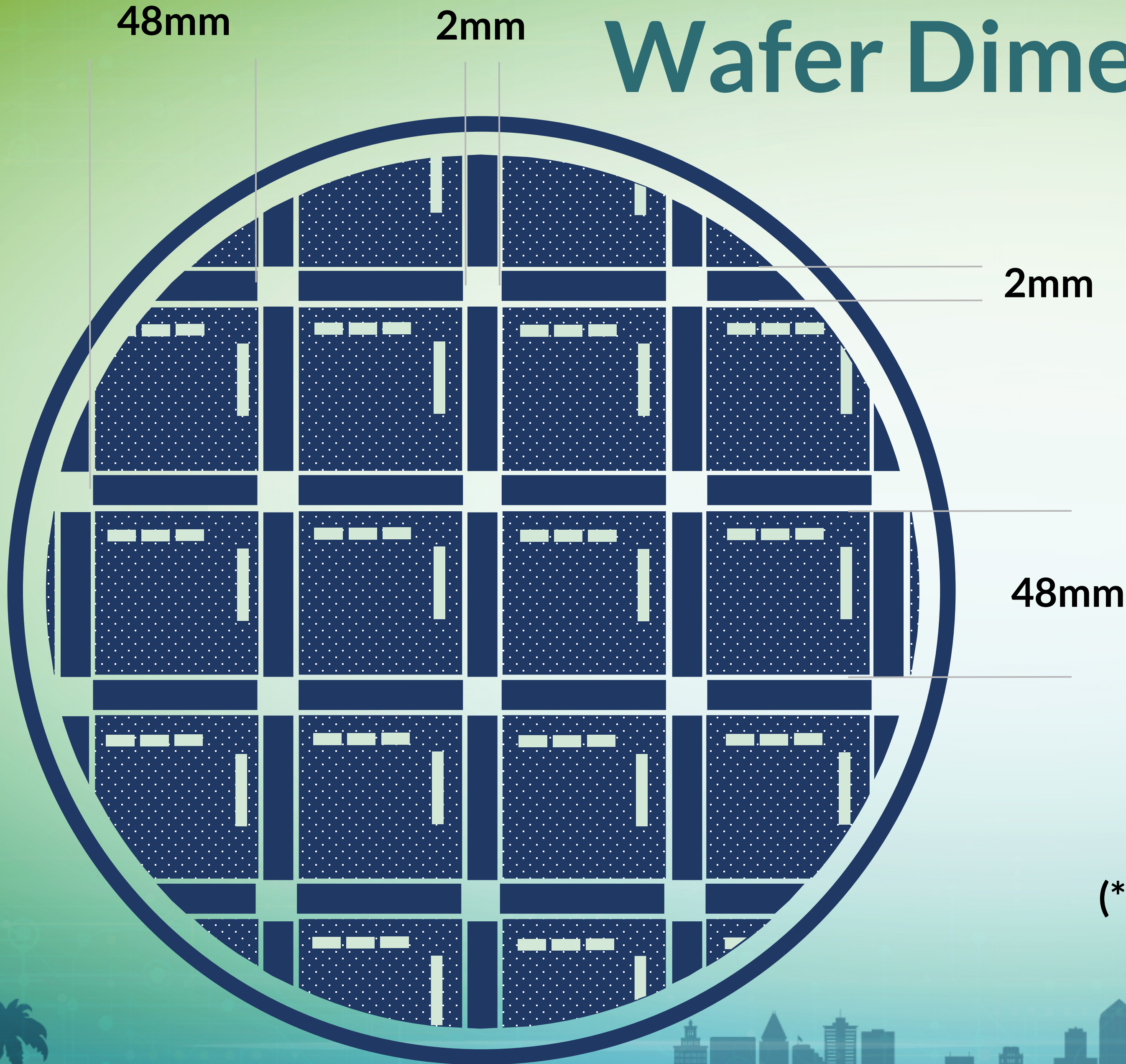
CASE STUDY #1

MULTI-LAYER STUCK WAFER TEST

Product To Be Tested



- The product is a multi-layer silicon wafer
- The layout includes 2 types of verification patterns, in addition to the devices



Wafer Dimensions

Dimension	Nominal	Tolerance
Diameter	200 mm	± 0.2 mm
Thickness	0.200 mm	±0.025 mm
Flat Length	57.5 mm	± 1.0 mm
Warpage (*)	25um	± 25 µm
Total Thickness Variation	5	± 5 µm

(*) Warpage is automatically compensated by laser surface mapping

Test Requirements

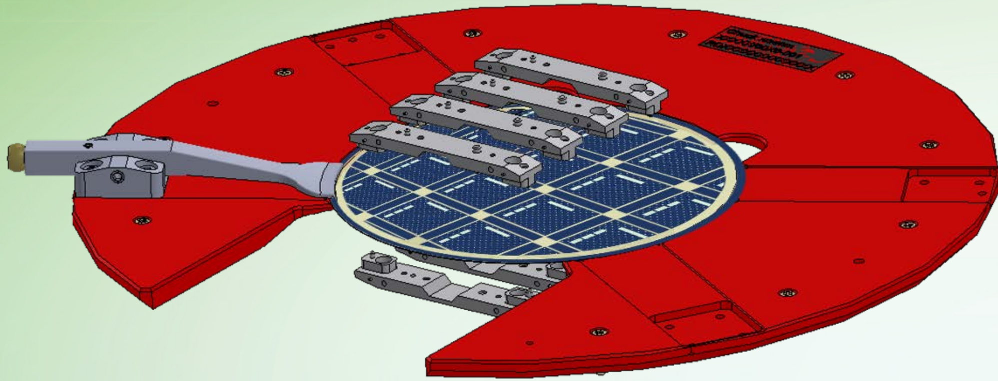
FIRST PHASE: PROCESS CHARACTERIZATION

- Top/Bottom Capacitive & Resistive Test on every chip
- Kelvin Test on Verification Patterns, to cross-check the manufacturing process
- The test sequence must be performed on every layer

SECOND PHASE: VOLUME PRODUCTION

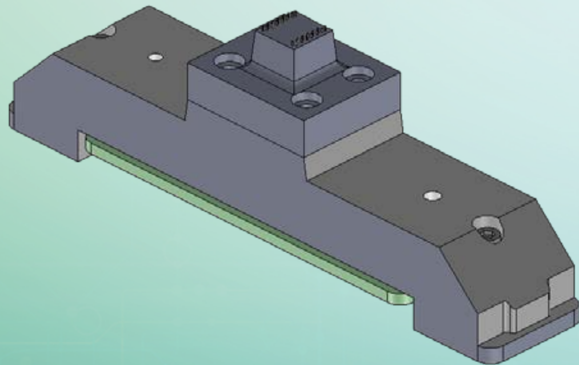
- Kelvin Test on Verification Patterns to validate the wafer quality

Chuck and Probe Card Design

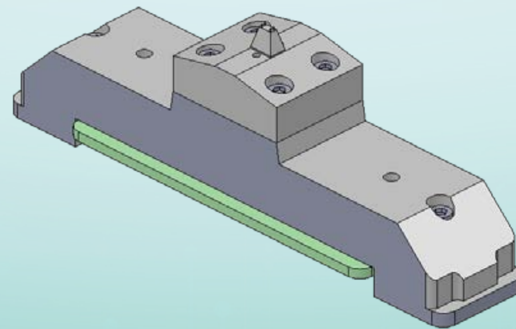


On the top and bottom side, 4 probe cards designs are required:

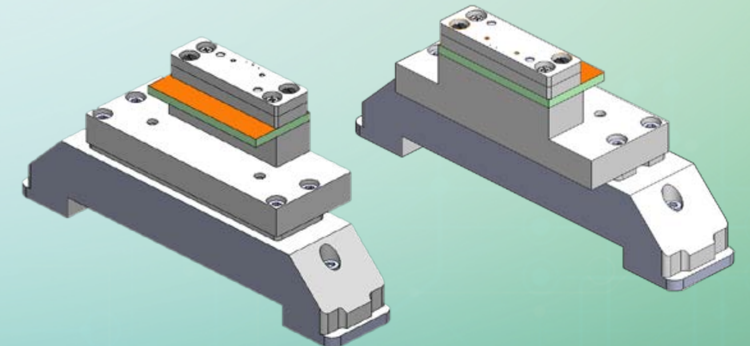
Probe Card for Pattern #1



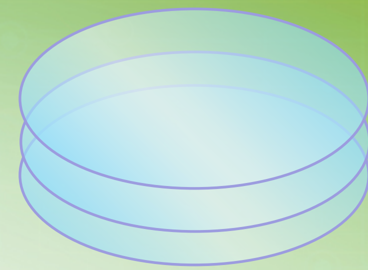
Probe Card for Pattern #2



2 Probe Cards with 1 needle for pad probing



Multi-Layer Test Steps



Step 1 - 1 layer		Step2 - 2 layers		Step 3 - 3 layers	
TOP Kelvin Test on Verification Pattern	TOP/BOTTOM Resistive/Capacitive Test on Pad	TOP Kelvin Test on Verification Pattern	TOP/BOTTOM Resistive/Capacitive Test on Pad	TOP Kelvin Test on Verification Pattern	TOP/BOTTOM Resistive/Capacitive Test on Pad
BOTTOM Kelvin Test on Verification Pattern	TOP/BOTTOM Resistive/Capacitive Test on Pad	TOP Kelvin Test on Verification Pattern	TOP/BOTTOM Resistive/Capacitive Test on Pad	TOP Kelvin Test on Verification Pattern	TOP/BOTTOM Resistive/Capacitive Test on Pad

CASE STUDY #2

PROBE MARK AUTO DETECTION

Introduction

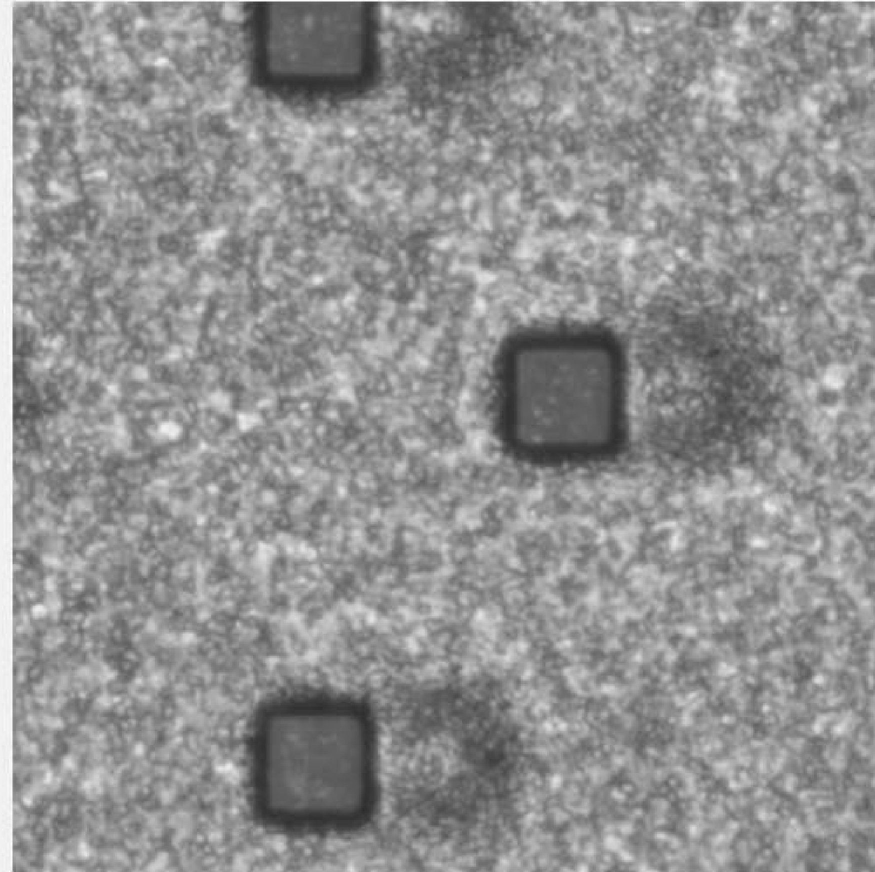
- The adjustment of probing offset and overdrive parameters can be tough and time-consuming
- To speed up and automate this operation, an automatic optical inspection performed before and after the probing can be helpful
- A specific combination of standard geometrical algorithms and AI-based algorithms has been developed to efficiently and accurately detect the touch point and make the required corrections

Analysis for Auto Detection

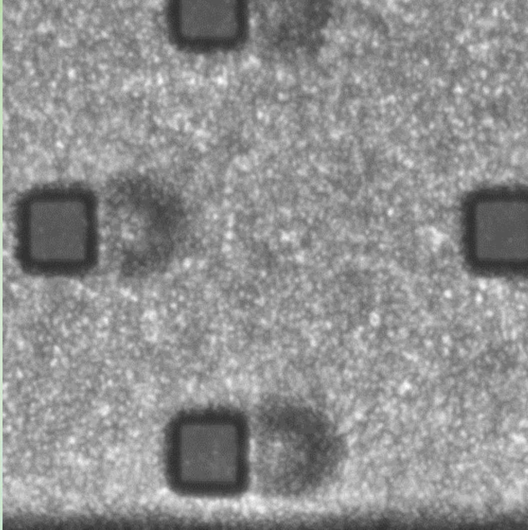
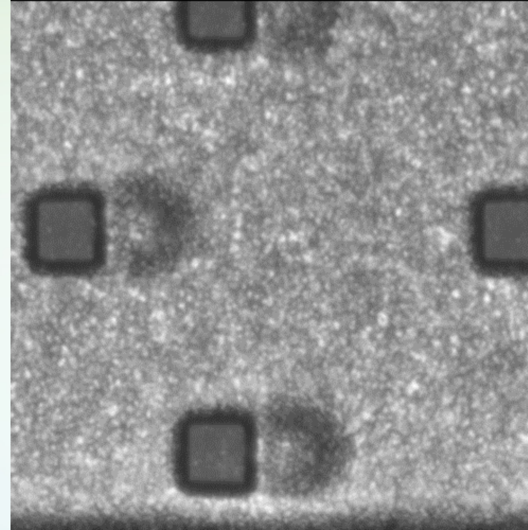
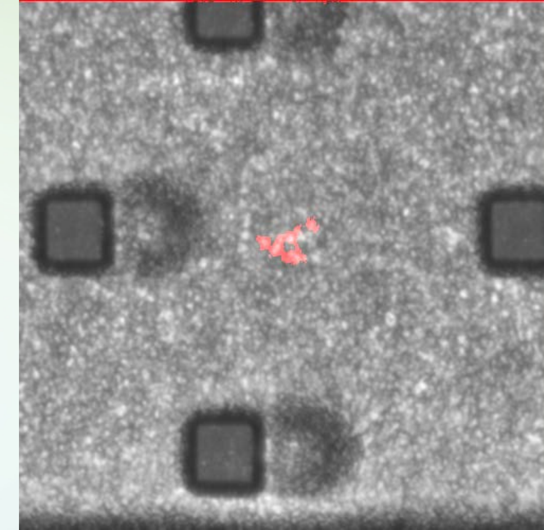
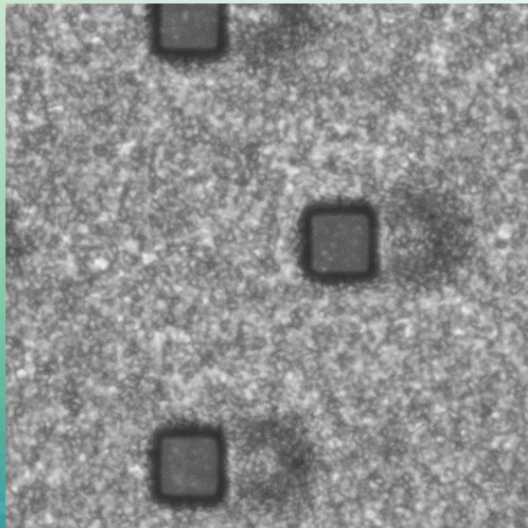
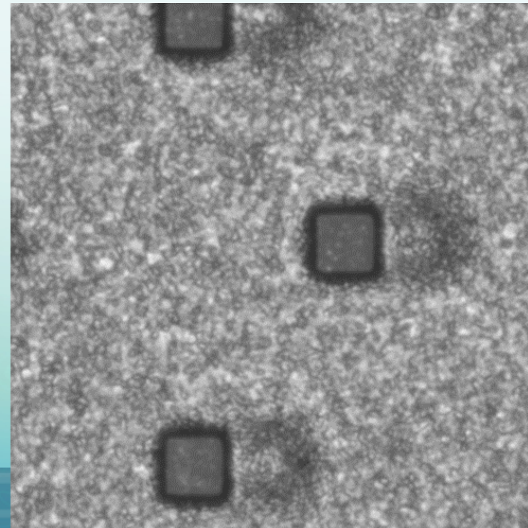
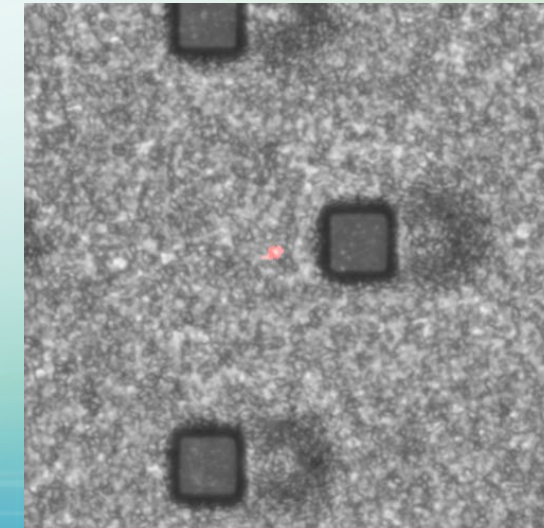
The video shows a rapid transition, repeated several times, between image acquired before and after the probe touch, in order to be able to identify the touch visually.
At the end, we can see the result of the identification of the touch by the developed image processing algorithm.

The probe used has a diameter of 20 µm.

The red mark size is approximatively 16x12 µm.



Optical Test Results

	Before Touch	After Touch	Test Result
1			
2			

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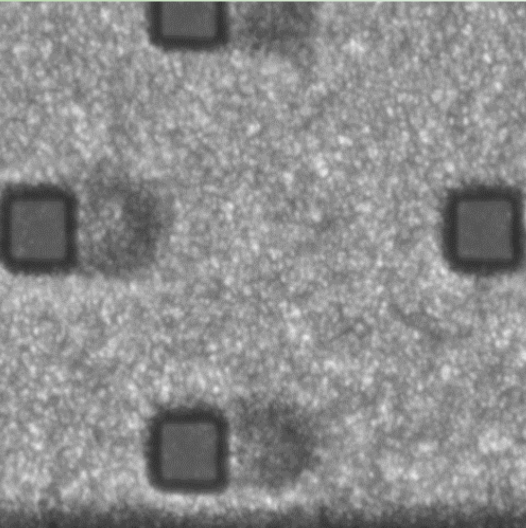
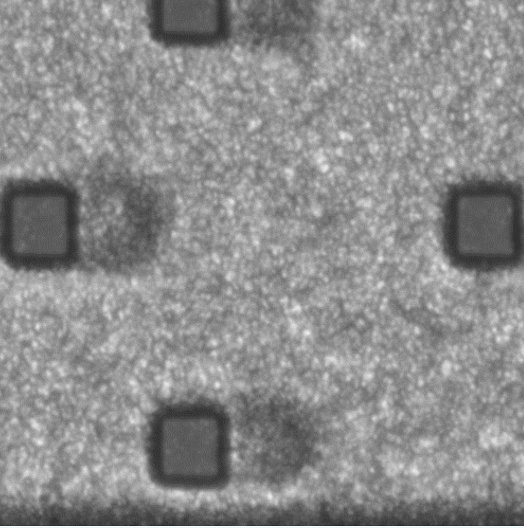
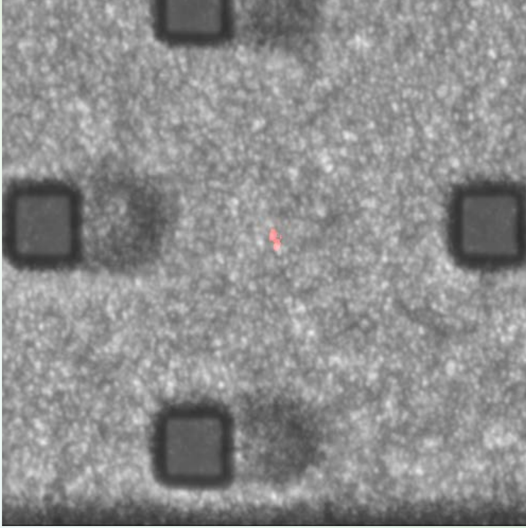
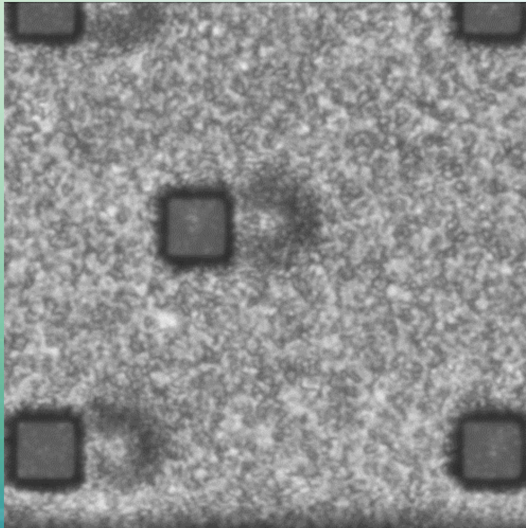
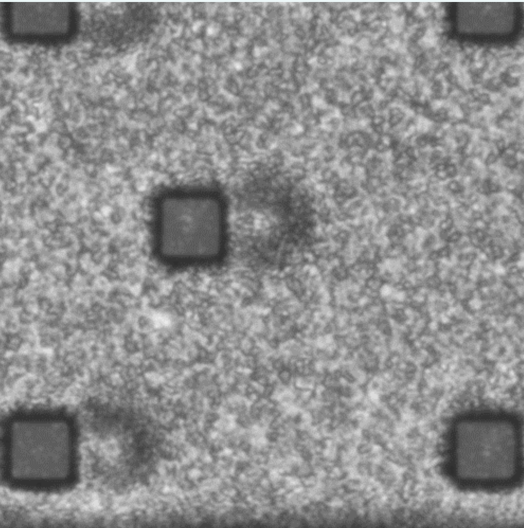
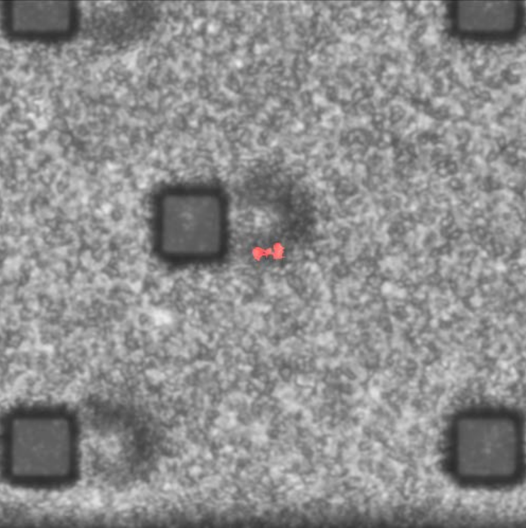
3			
4			

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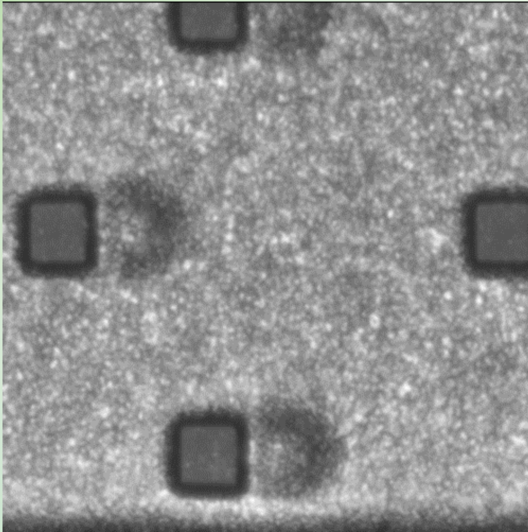
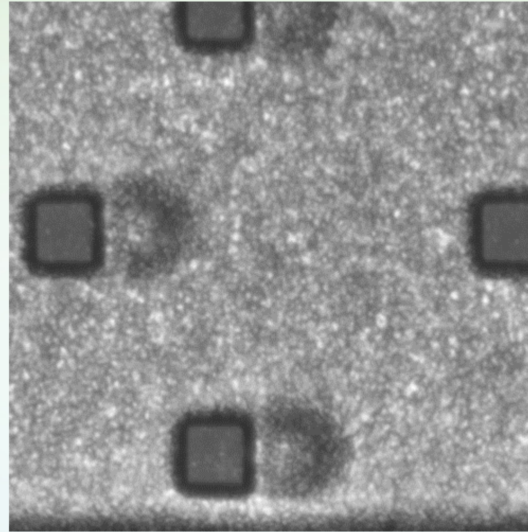
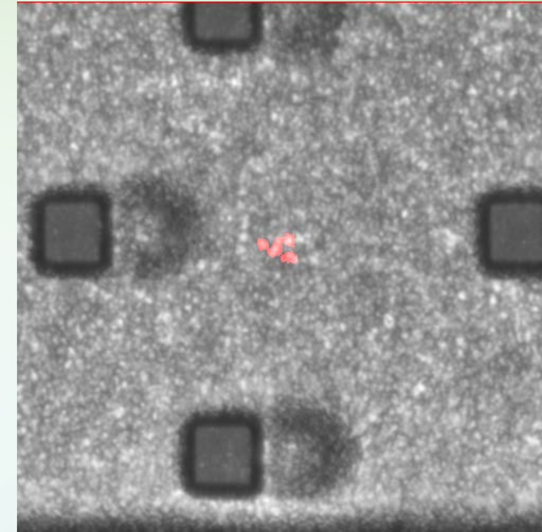
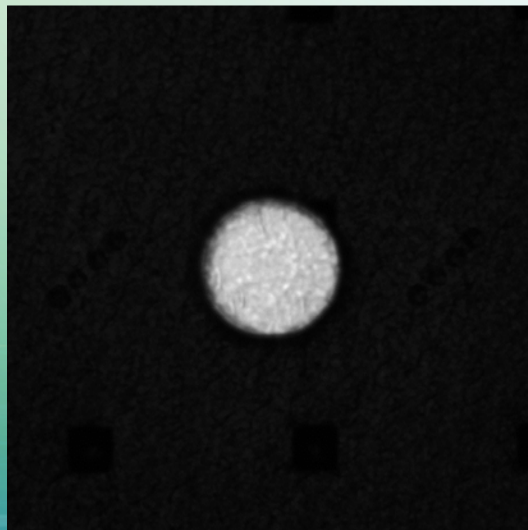
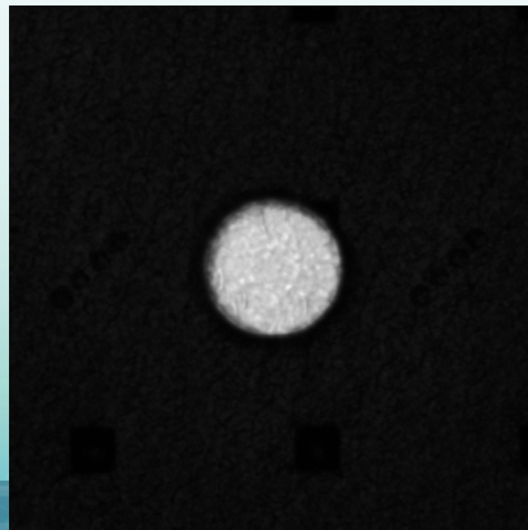
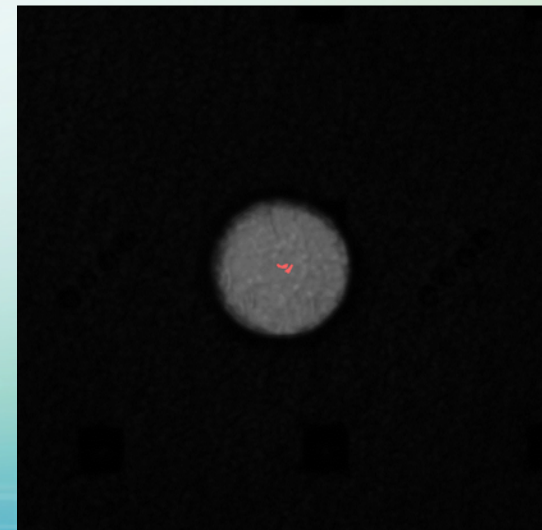
5			
6			

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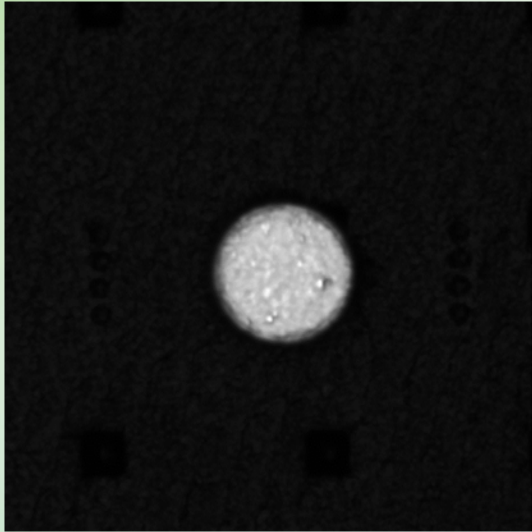
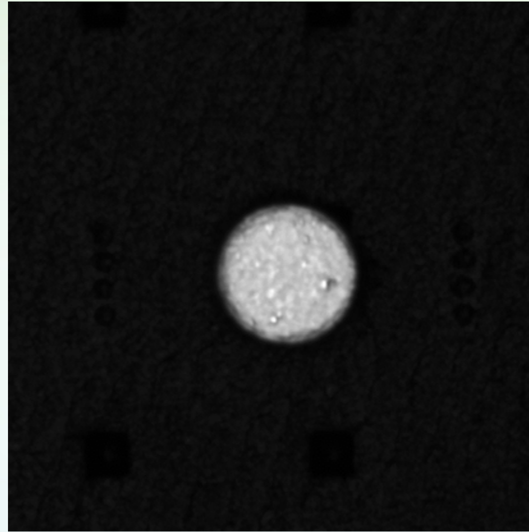
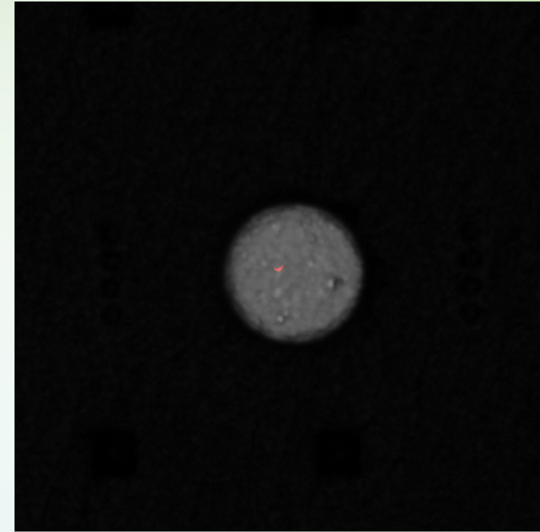
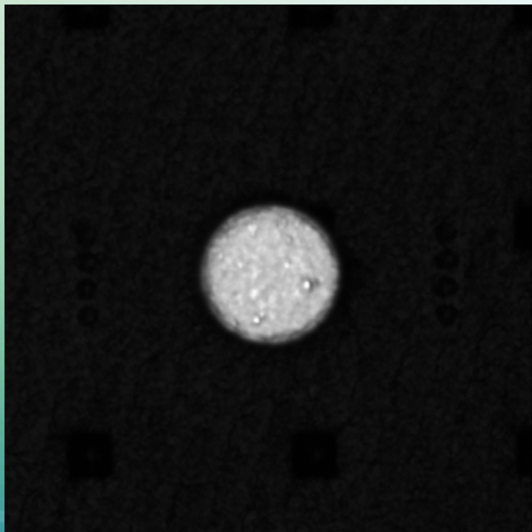
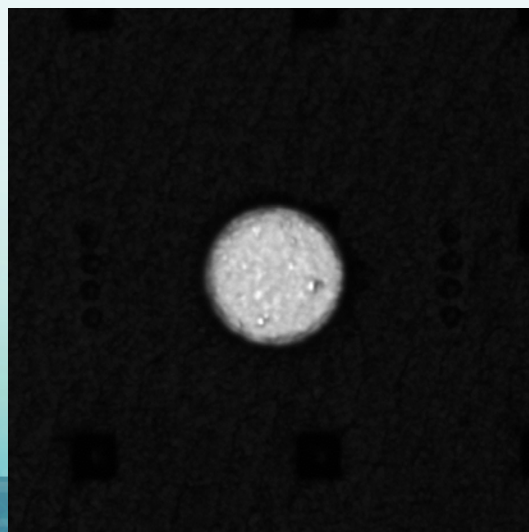
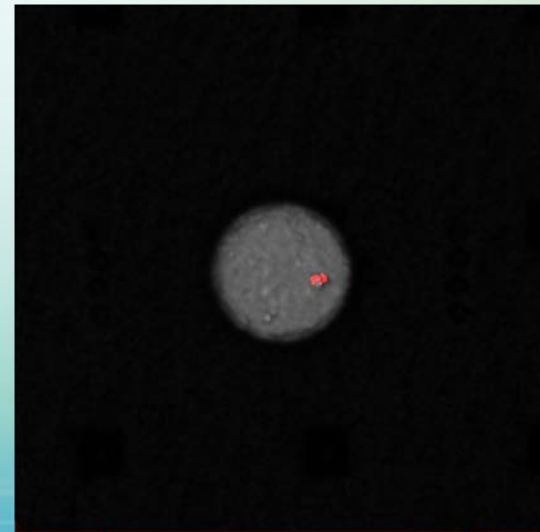
	Before Touch	After Touch	Test Result
7			
8			

Conclusions

While standard prober architecture remains the standard choice for most wafer products, a different approach based on multiple mobile probe cards can solve many tough challenges in testing, allowing for a complete test at wafer level of the most complex and innovative technologies.

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