SWTEST

PROBE TODAY, FOR TOMORROW

2024 CONFERENCE

Digital Lithography Enhances Fine Pitch Probe Cards Performance

EVG®

FUJIFILM

Ksenija Varga

EV Group

- EV Group: Introduction & Technologies
- Digital Lithography in Fine Pitch Probe Cards Manufacturing
- Methods, Materials and Procedures
- Results & Discussions
- Conclusions & Outlook
- Follow–On Work

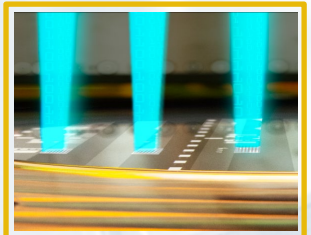

EV GROUP
EVG
EV GROUP
FORSTINGER

Leading supplier of wafer processing equipment for the MEMS, nanotechnology & semiconductors markets.

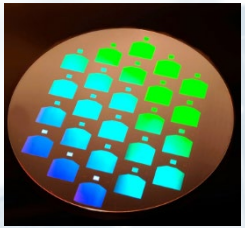
Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1300 employees worldwide.

Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China, Taiwan & Malaysia.

Advanced Resist Processing EVG®150 Series



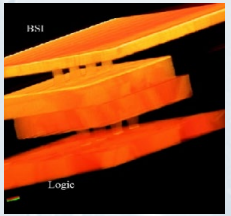
DIGITAL LITHOGRAPHY LITHOSCALE®



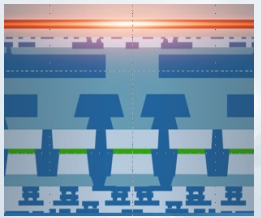
Nanoimprint & S&R Mastering HERCULES®

Wafer Level Optics & Photonics Packaging EVG®7300

METROLOGY EVG®40NT



3D Integration & Bonding Technologies



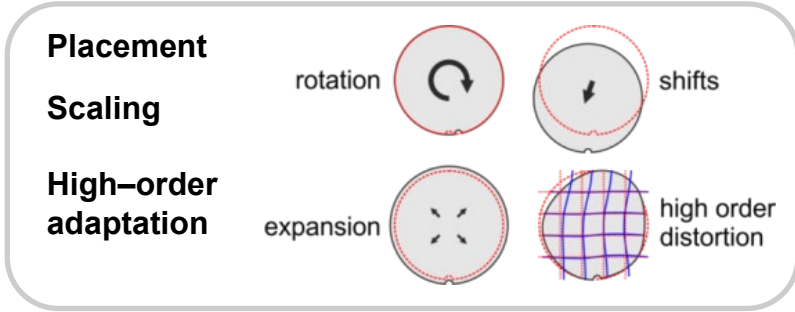
IR Laser Release Technology EVG®880

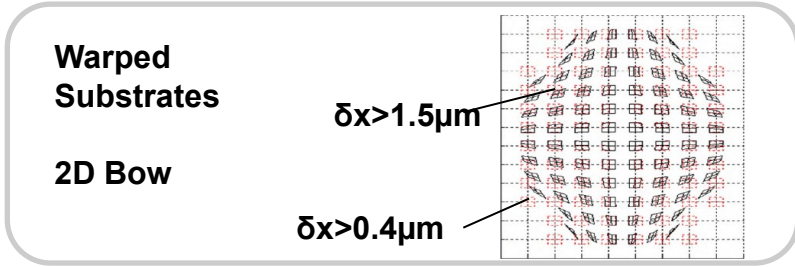
PATTERNING REQUIREMENTS

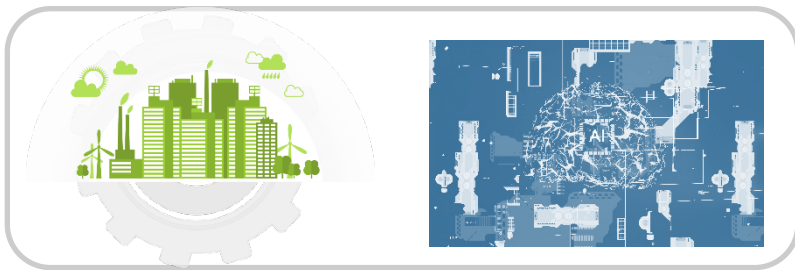
- **Several RDLs**, small via opening <5 µm, steep via profiles.
- **Adaptive lithography** with “on–the–fly” distortion compensation.
- **Warpage handling** in complex packages.
- **Economic benefits**.

MATERIAL REQUIREMENTS

- Dielectric polyimides enabling high–resolution patterning.
- PFAS–Free Formulation, Sustainability.





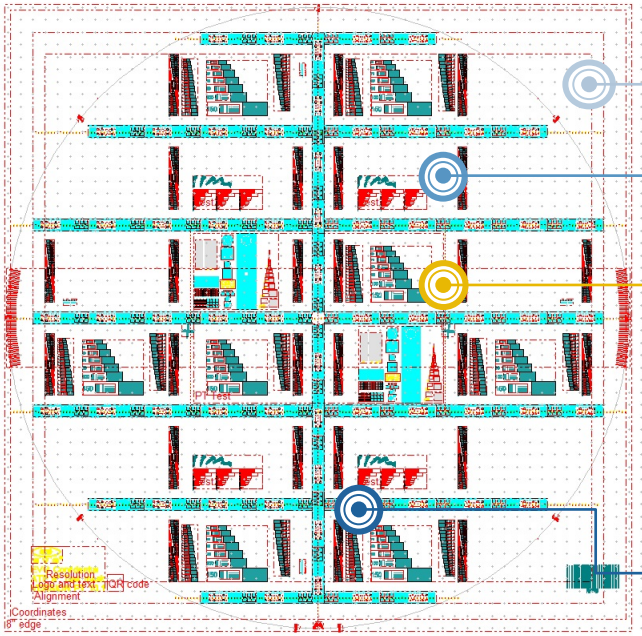


- EVG's **Maskless Exposure Technology.**
- **High Resolution Polyimide** Dielectric Materials: newly developed, low temperature cure by Fujifilm.
- **Substrates**: 200mm both, Si and PVD Cu wafers.
- **Metrology**: CD SEM for top/bottom via measurement & SEM cross–sections.

EXPOSURE MATRIX
DOSE/FOCUS/WAVELENGTH

PROCESS	PARAMETERS
Wavelengths [nm]	375, 405
DOSE RANGE [mJ/cm²]	LTC 9320–E76B next gen Si substrate 300–1050 Cu substrate 225–975 LTC 25000 Si and Cu substrates 300–1050
FOCUS RANGE [µm]	From –14 to +6 above dielectric surface → In 2 µm steps
Post Exposure Processing	TARGET FT = 5 µm Hard Bake at 100 °C for 60 s Cure at 230 °C for 3h → Followed by O_2–plasma descum to remove residues in contact and bond pads. Target removal of 2000A.

EVG TEST LAYOUT



Alignment pattern

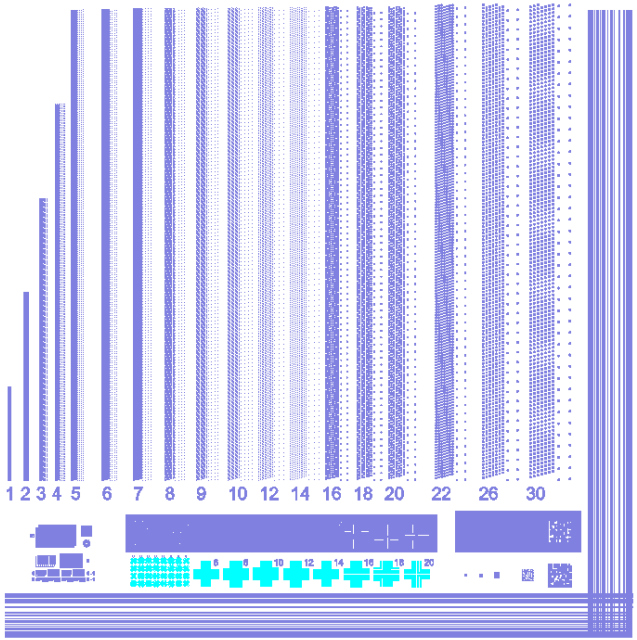
New test structures

Standard L/S test pattern

Various additional test patterns Die Annotations

DENSE VIA 1:1

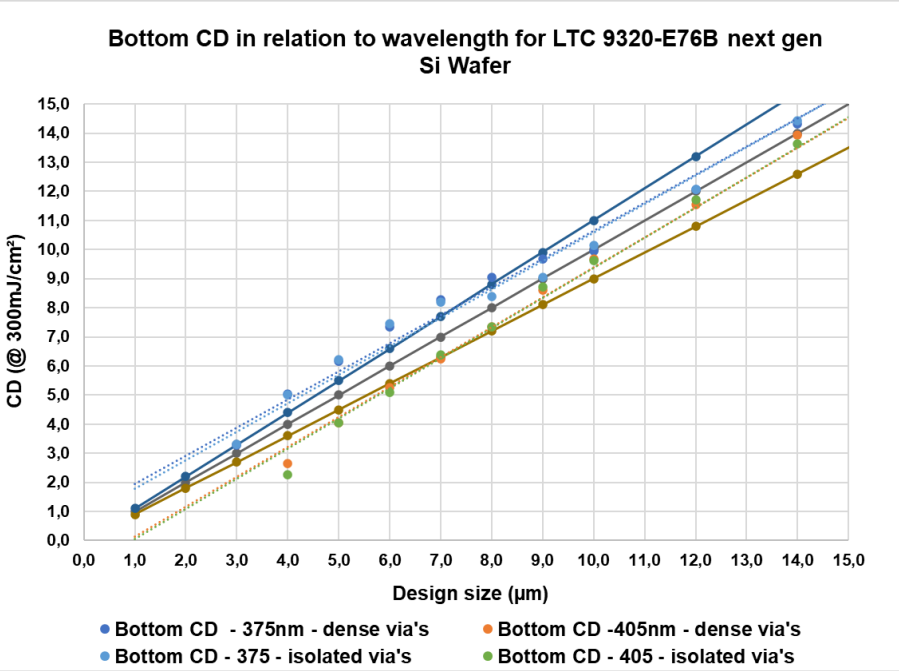
ISOLATED VIA 1:5



L/S Patterns

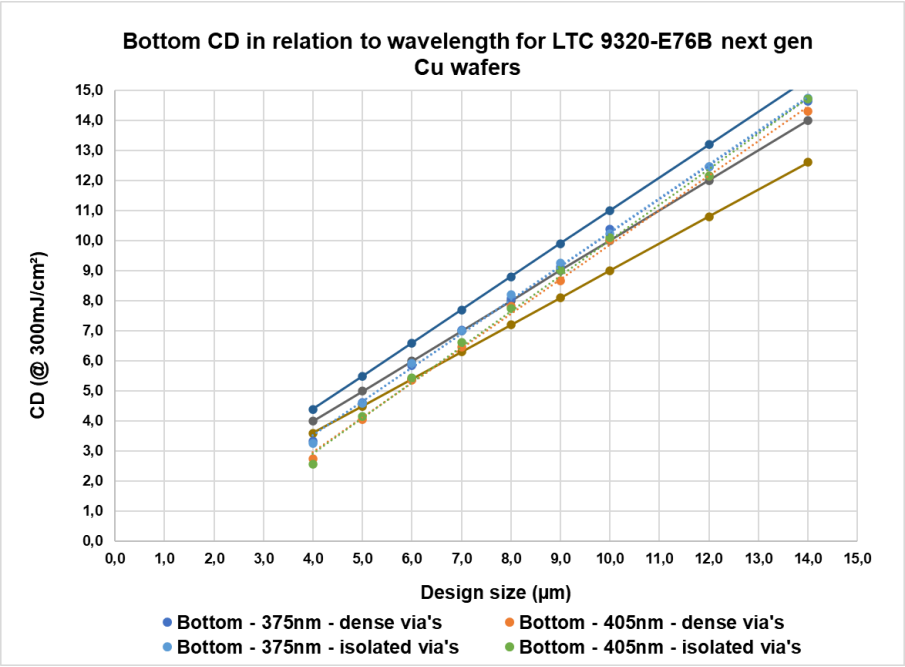
DataMatrix Codes

LINEARITY INVESTIGATION at λ≈375nm and 405nm Si Wafers



- Small via size: slight difference in measured bottom CD to digital design size.
- **The bottom CD of via exposed at 405 nm is lower than via exposed at 375 nm, for the dense via design**.
- Linear interpolations indicate fluctuations and unveil a slight non–linearity of the response.
- The lower resolution limits are affected by the offset in exposure due to over and under–exposure effects.

LINEARITY INVESTIGATION at λ≈375nm and 405nm Cu Wafers



- **The advantage of digital systems**:

→digital corrections & layout compensation processes can be performed more efficiently compared to the corrections required in mask–based systems.

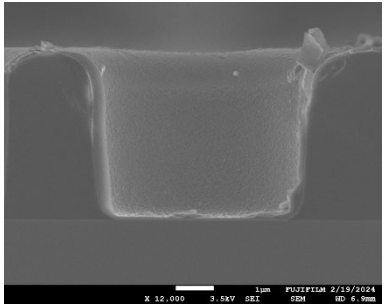
- **Real time adaptations of process parameters is allowed**.
- Lower resolution on plated Cu:

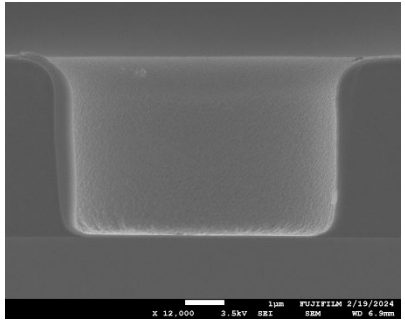
→due to substrate granularity

→leading to poorer pattern definition through light scattering and interaction in the exposure area.

PI Dielectric: LTC 9320 E76B next gen INFLUENCE of EXPOSURE at λ≈375nm on VIA PROFILES

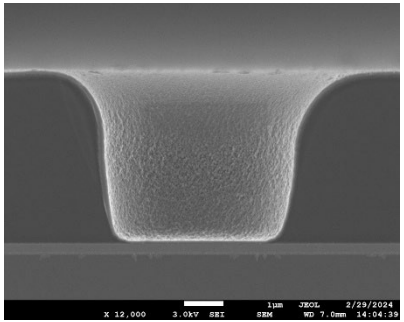
Si Wafer

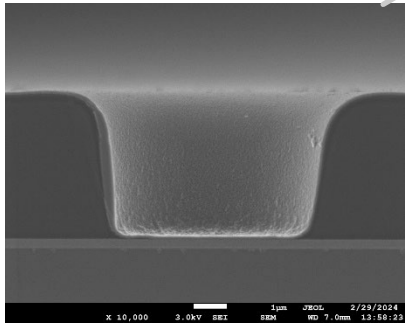




Dense via's 4 µm (left) & 5 µm (right).

Cu Wafer





Isolated via's 4 µm (left) & 5 µm (right).

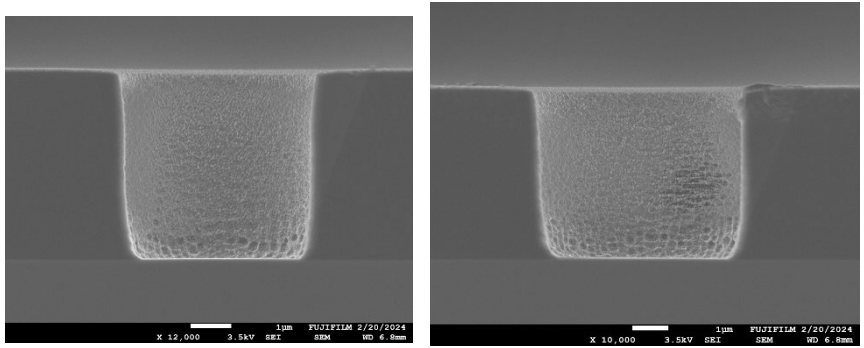
- **Si wafers**

→ **Very steep via profiles** are resolved for the bottom via CD of 4 µm (angle=100.3°) and 5 µm (angle=98.5°).

- Via size labeling is defined by the exposure equipment's design settings (layout resolution values).

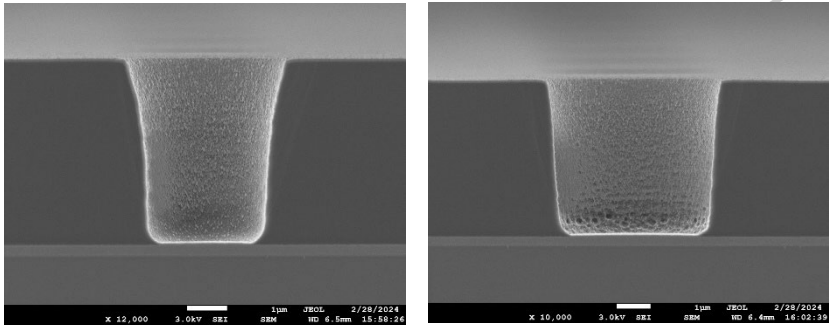
PI Dielectric: LTC25000 INFLUENCE of EXPOSURE at λ≈375nm on VIA PROFILES

Si Wafer



Dense via's 5 µm (left) & 6 µm (right)

Cu Wafer



Dense via's 4 µm (left) & 5 µm (right)

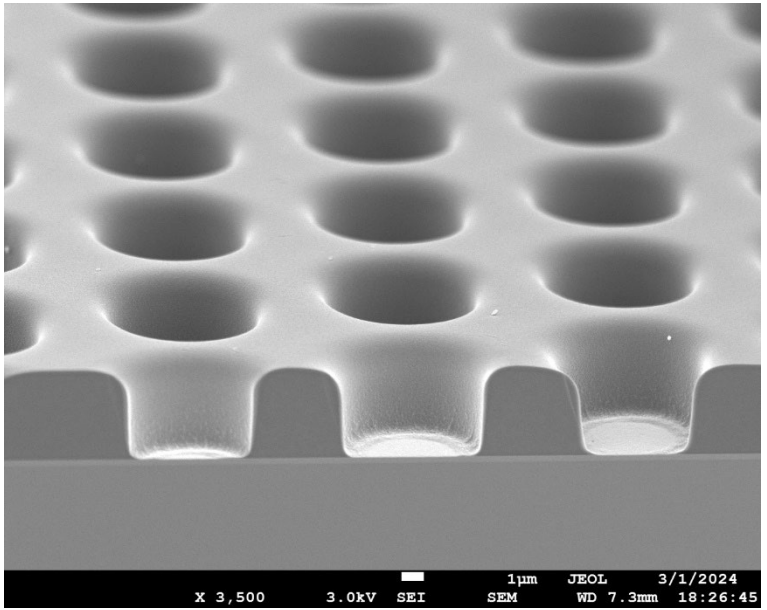
- The side wall profiles obtained on patterned PI on the Cu substrates reveal very similar profiles like those obtained on Si substrates.
- The targeted minimal footing was achieved with the optimized digital processing parameters

→ obtained from the test exposure matrix.

TOP TILTED VIEW of SEM CROSS–SECTION IMAGE of DENSE VIA

→ EXPOSED at 375nm for high resolution PI on Cu–wafer.

→ **Steep via opening accomplishes homogenous metallization in subsequent integration processes**.



PI Dielectric LTC 9320–E76B next gen

BOTTOM VIA OPENING = 5 µm

FT = 5 µm

Digital Lithography | Conclusions & Outlook

- The objective of developing **lithographic patterning for use in probe cards** has been successfully achieved.
- Both next gen polyimide dielectrics, LTC versions developed by Fujifilm demonstrated **<5 µm via diameter** capability.
- **Steep via profiles** of PI facilitate improvement of integration processes and achievement of high electrical properties.
- Versatility of **mix–and–match exposure** wavelengths allows for the exploration of novel materials processing techniques.

Digital Lithography | Conclusions & Outlook

- EVG's digital lithography equipment, LITHOSCALE®, is designed to facilitate **rapid R&D prototyping** & expeditious **transition from to HVM**.
- LITHOSCALE® plays significant role in the **digital transformation of lithography** in semiconductor testing equipment.

- **Traceability in Semiconductors**.
- Automotive & Security Applications.
- Enabled by **Die Annotation Software Feature** on LITHOSCALE®.
- Proven readable **DataMatrix Codes** in dimensions 50×50 µm squares with specialty RGB resists.

Thanks for your Attention!

- Contact us with any questions …

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