Optimizing Design of a Probe Card using a Field Solver

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Field solvers used: Ansoft's Maxwell 2D Extractor, Maxwell Q3D Extractor, Maxwell Spicelink

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Design Challenges

- Increased bandwidth of digital test signals
- Increasing buss widths
- Design cycle times shrinking
- New board technologies being introduced
- New design methodology needed:
  - increased productivity
  - robust designs, correct the first time
  - incorporating high speed effects

An Example Applied to a Conventional 256 Pin Probe Card

New methodology:

- perform design tradeoff analysis with virtual prototypes
- use parasitic extraction and simulation to evaluate impact of physical design on electrical performance

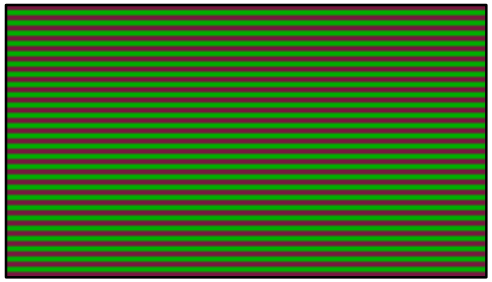
Features to evaluate

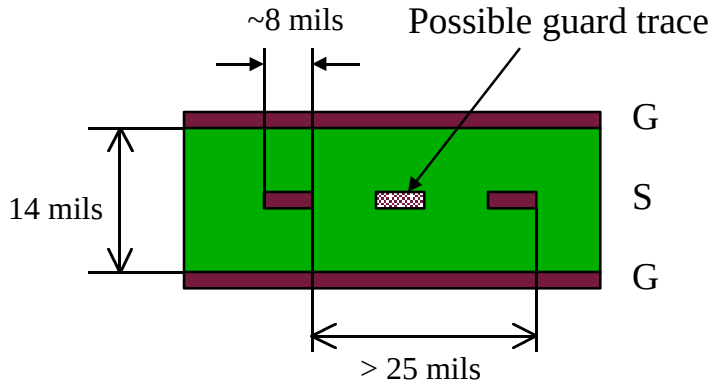
1. Optimize the design of the fan out from the pogo pin pad to the needle pad

2. Shorten needles

Board Stackup

- Typical 8 layer Stack up:
  - G
  - S
  - G
  - VCC
  - VCC
  - G
  - S
  - G





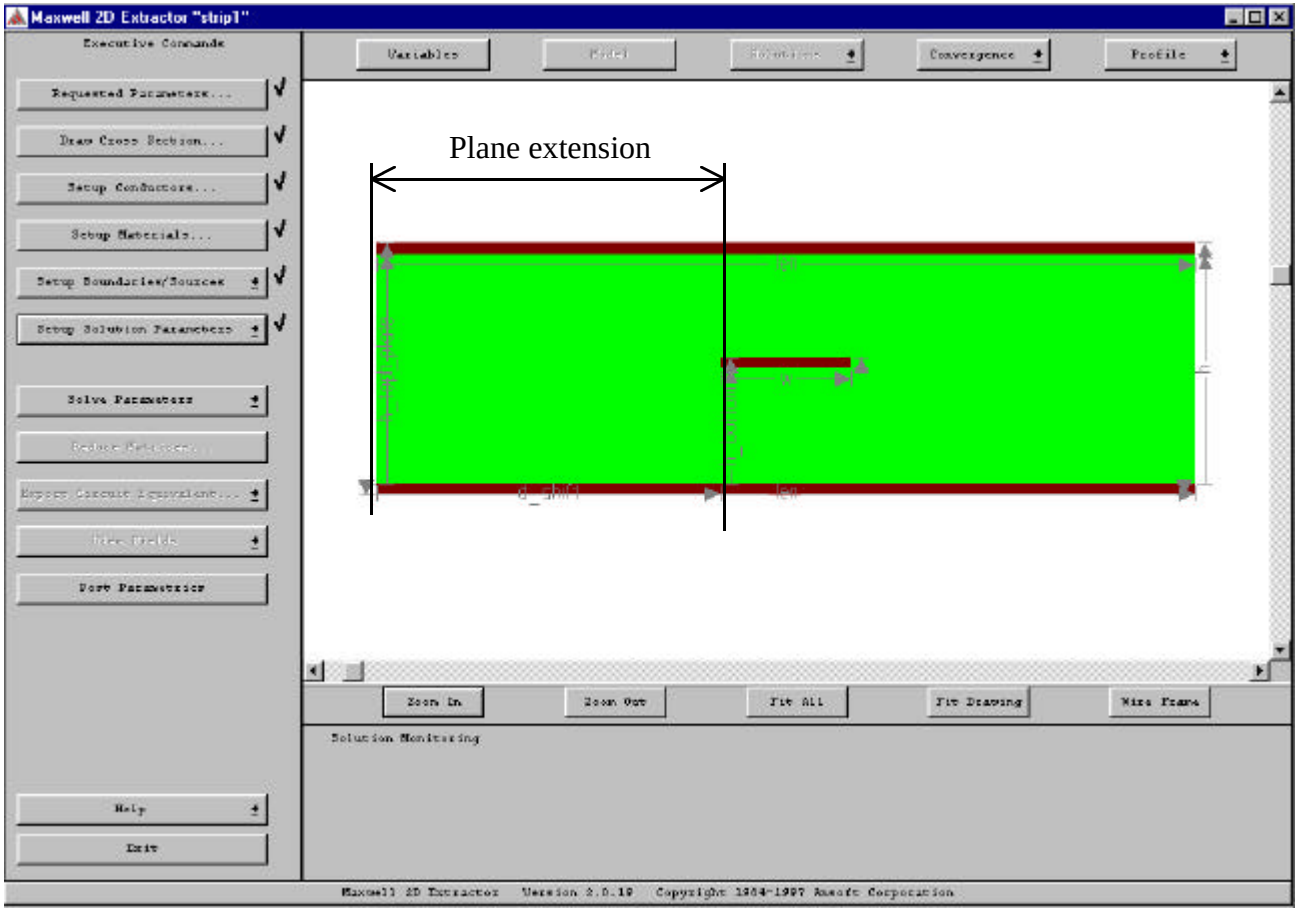
Issues to analyze:

- ✓ How wide should the ground planes extend for accurate analysis?
- ✓ What line width should be used for 50 Ohms
- ✓ What is cross talk as spacing between traces increases?
- ✓ What is effect on cross talk from central guard trace: electrostatic or ground conductor

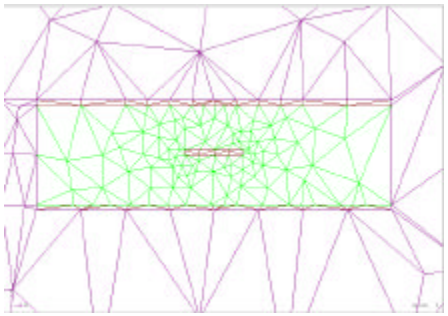
Parameterized Stripline Model

Problem Setup in Ansoft's Maxwell 2D Extractor:

sweeping distance from edge of plane to trace



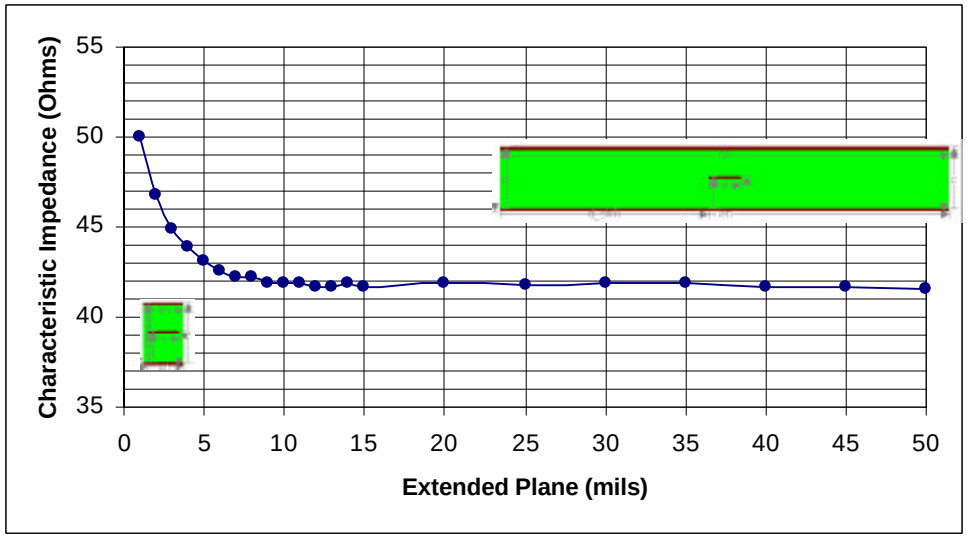
Effect on Extent of Ground Planes



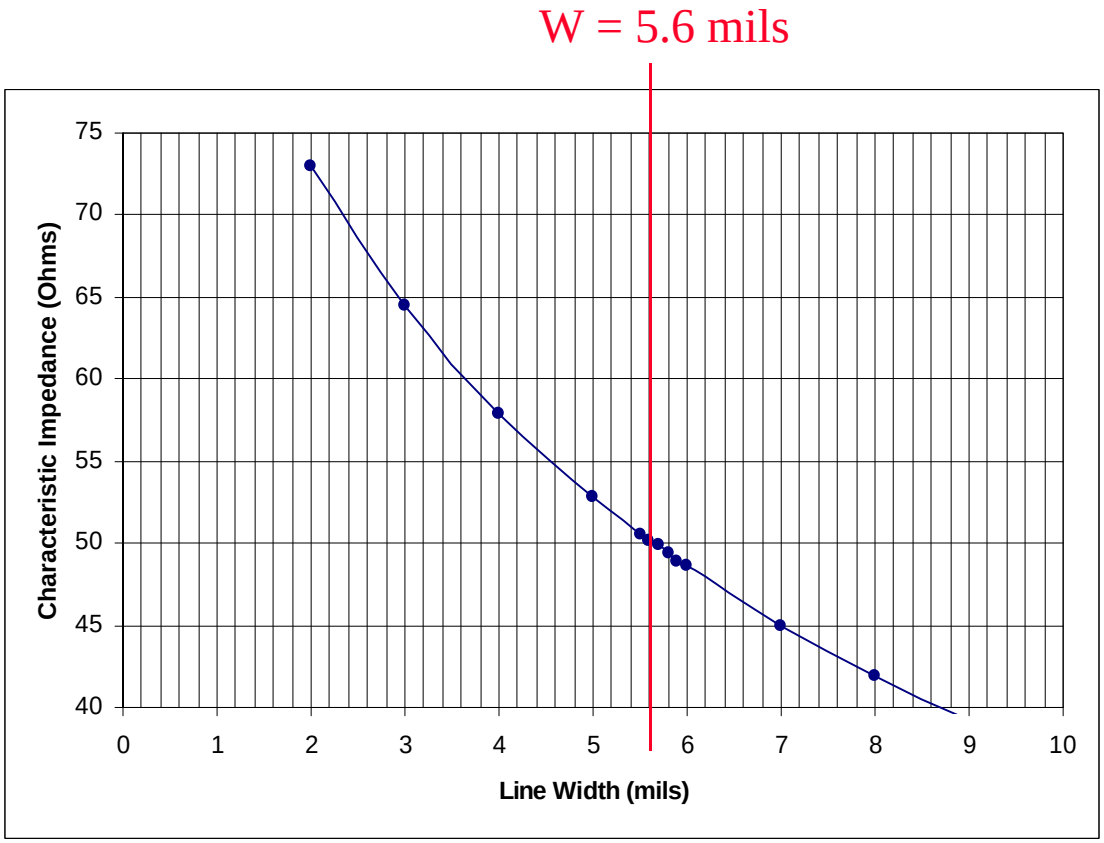
Automatic adaptive mesh

More than 10 mils on either side is not needed:

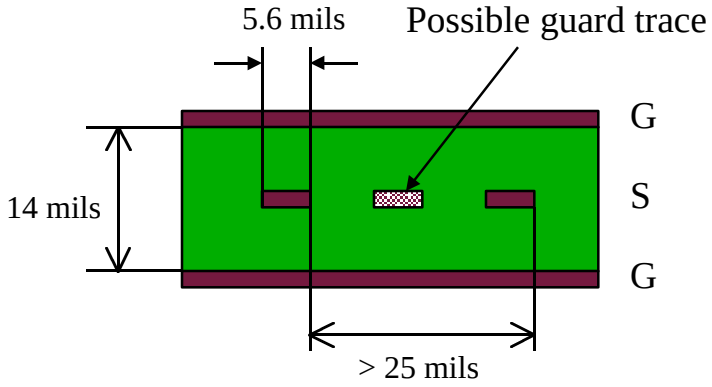
rule of thumb- *in stripline, fringe fields extend on the order of 2/3 the dielectric thickness*



Optimized Line Width for 50 Ohms

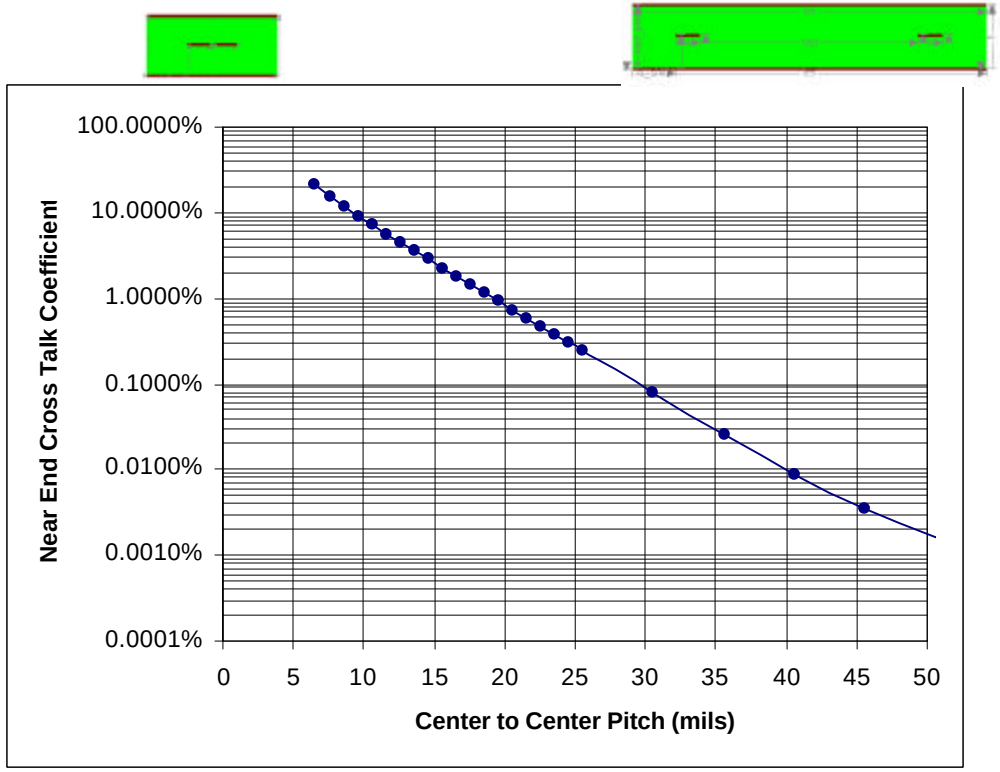


Final design rules



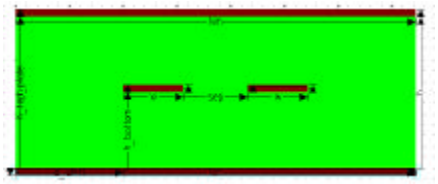
(dielectric constant = 4.0)

Cross Talk Between Two Traces



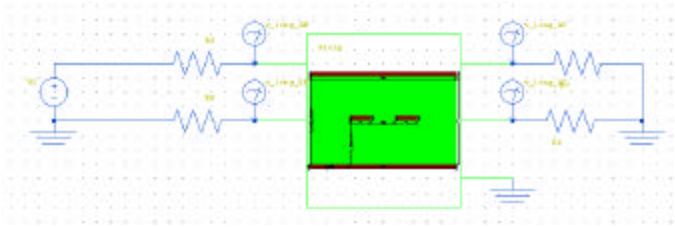
Pitch	**k_{ne}**
12 mil center	5.1%
15 mil center	2.5%
20 mil center	0.73%
25 mil center	0.27%
30 mil center	0.09%
50 mil center	0.002%

Cross Talk Behavior



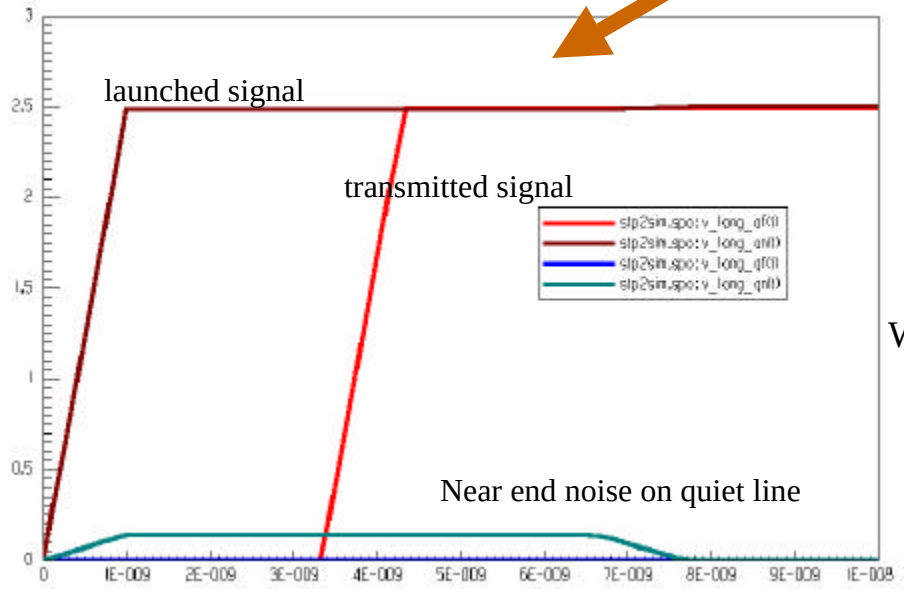
Pitch is 12 mils
k_{ne}(sat) = 5.1%

Export SPICE Deck



Build SPICE circuit,
with 0.5 m (19.5 inches, TD = 3.25 nsec) long trace
with 1 nsec long rise time

Simulate

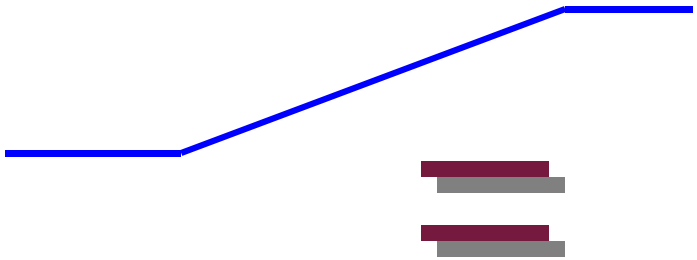


$$k_{ne} = \frac{V_{quiet\,(sat.)}}{V_{active}}$$

When 2 TD > rise time $V_{noise} = k_{ne} \; x \; V_{active}$

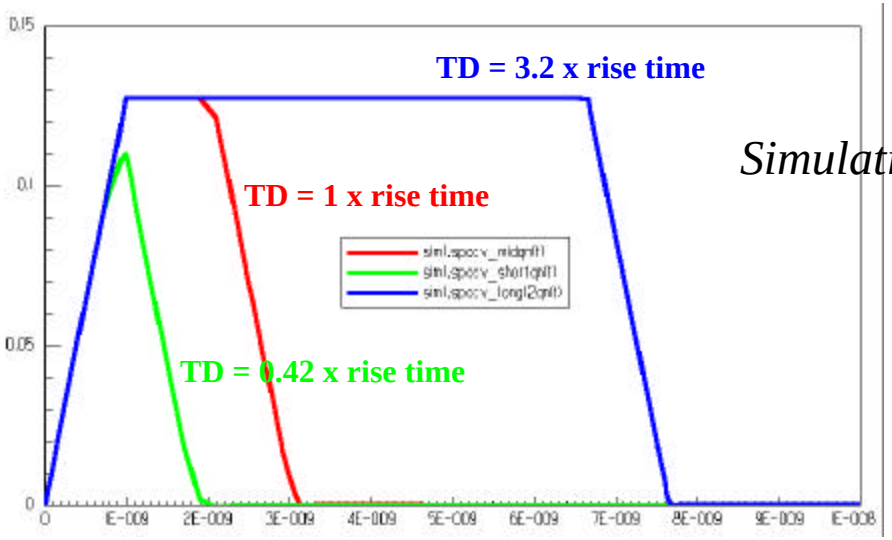
0.127v = .051 x 2.5v
0.127v, simulated

When TD < 1/2 Rise Time



$$V_{noise}(sat) \approx k_{ne} x V_{active} x \left(\frac{2TD}{\tau} \right)$$

Length = 2.5 inches, TD = 0.42 nsec, rise time = 1 nsec



Simulation of 12 mil pitch stripline

Estimate: V_{noise} = .051 x 2.5v x 0.84 = 0.107v

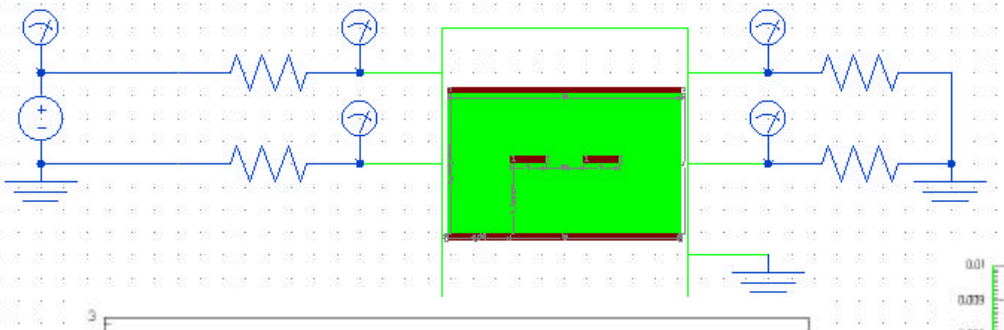
Cross Talk for 25 mil Pitch

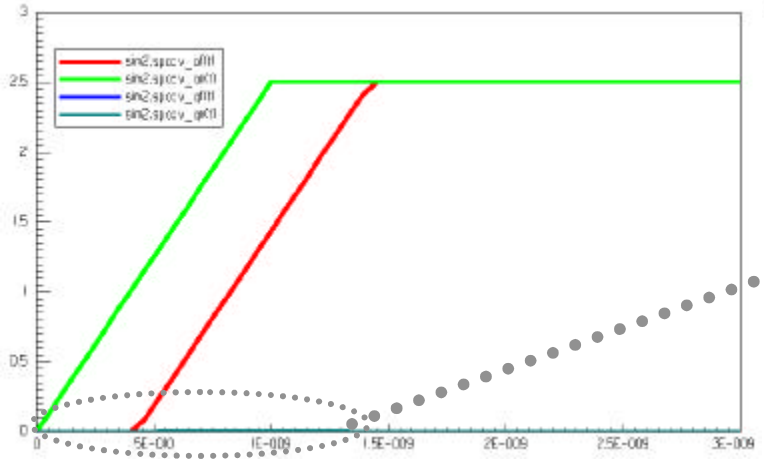
@ 25 mil pitch k_{ne} = 0.0027

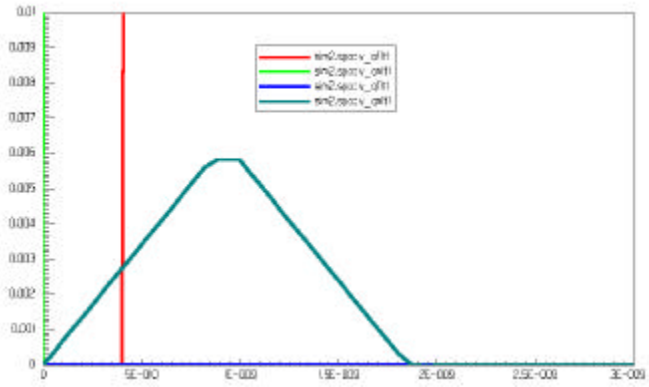
Length = 2.5 inches, TD = 0.42 nsec

$$V_{noise} \approx k_{ne}(sat) x V_{active} x \left(\frac{2TD}{\tau} \right)$$

V_{noise} = 0.0027 x 2.5v x 0.84 = 0.006v



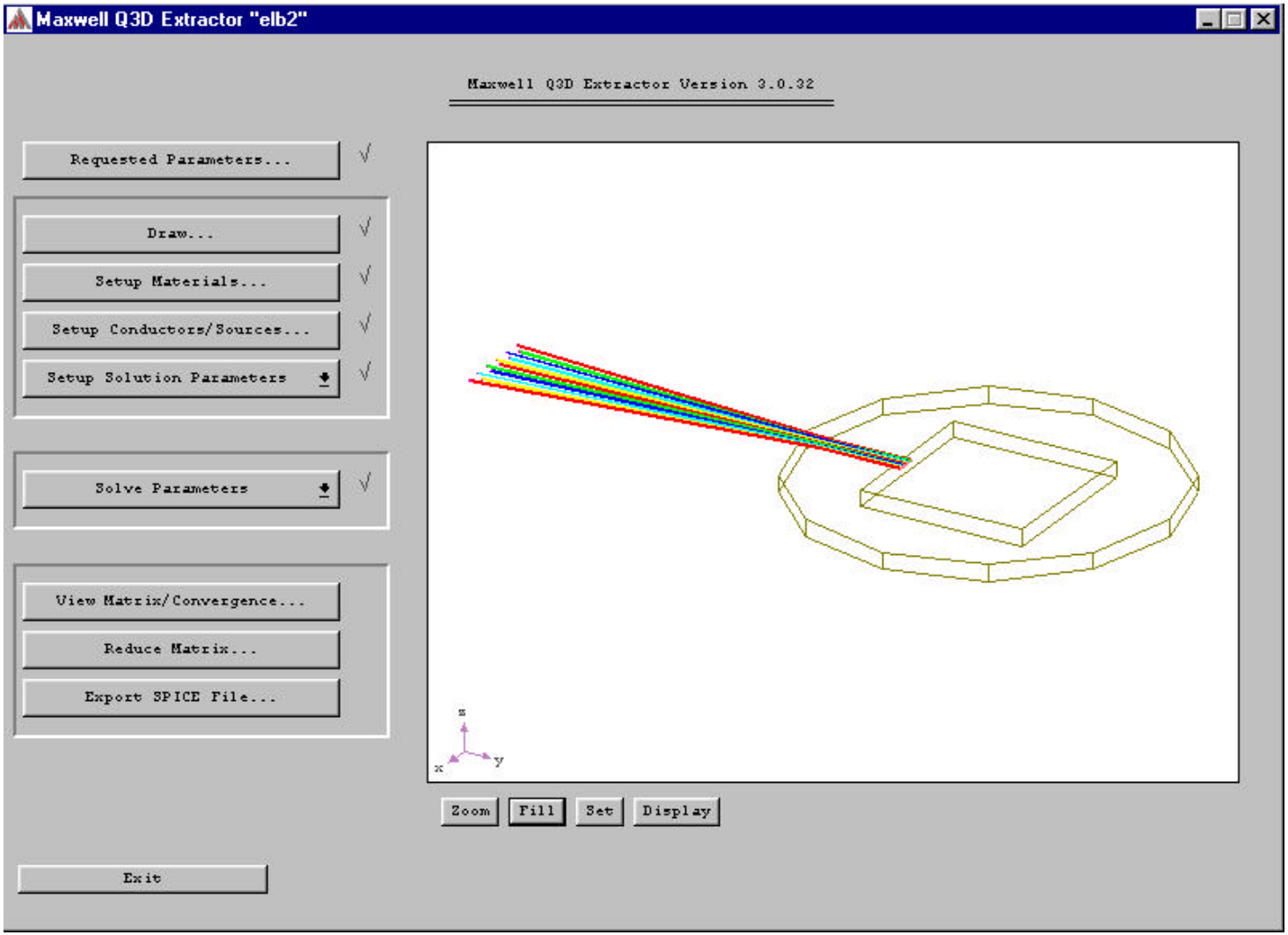




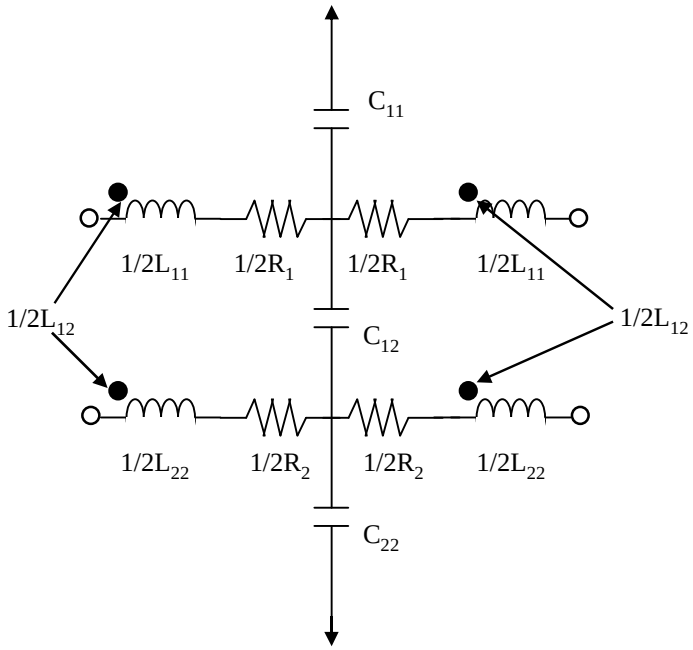
Simulated cross talk @ 25 mil centers is ~ 6 mV
cross talk @ 50 mil centers < 0.06 mV

3D Modeling of Needles

11 needles
5 mil diameter,
6 mil pitch at tip,
50 mil pitch at base,
epoxy ring
max length = 1 inch



Circuit Model for Needles



$$\begin{matrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{matrix}$$

Diagonal elements = self inductance
Off-diagonal elements = mutual inductance

$$\begin{matrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{matrix}$$

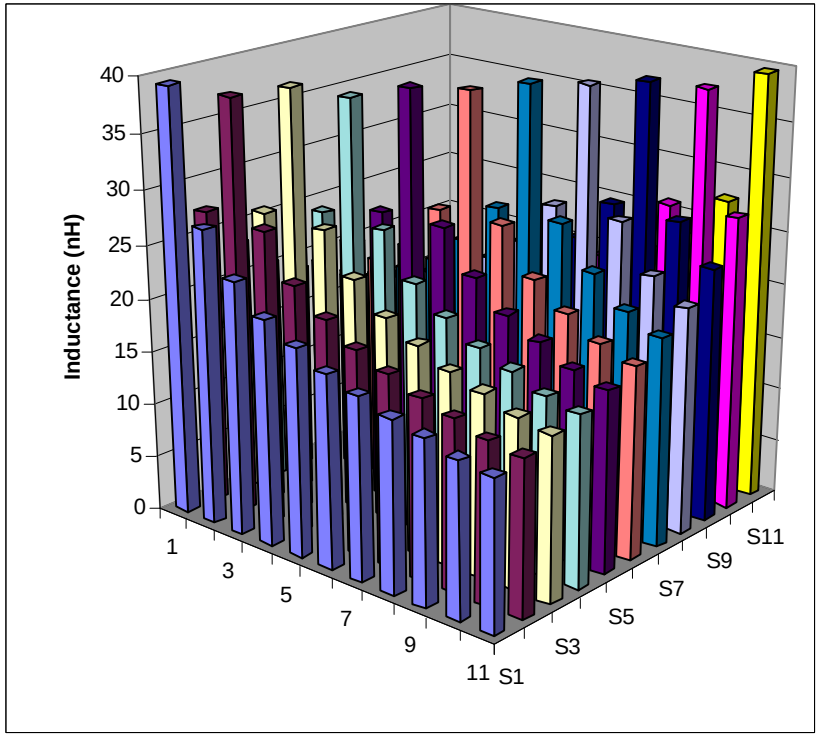
Maxwell Capacitance matrix:

Diagonal elements = loaded capacitance
Off-diagonal elements = negative coupling capacitance

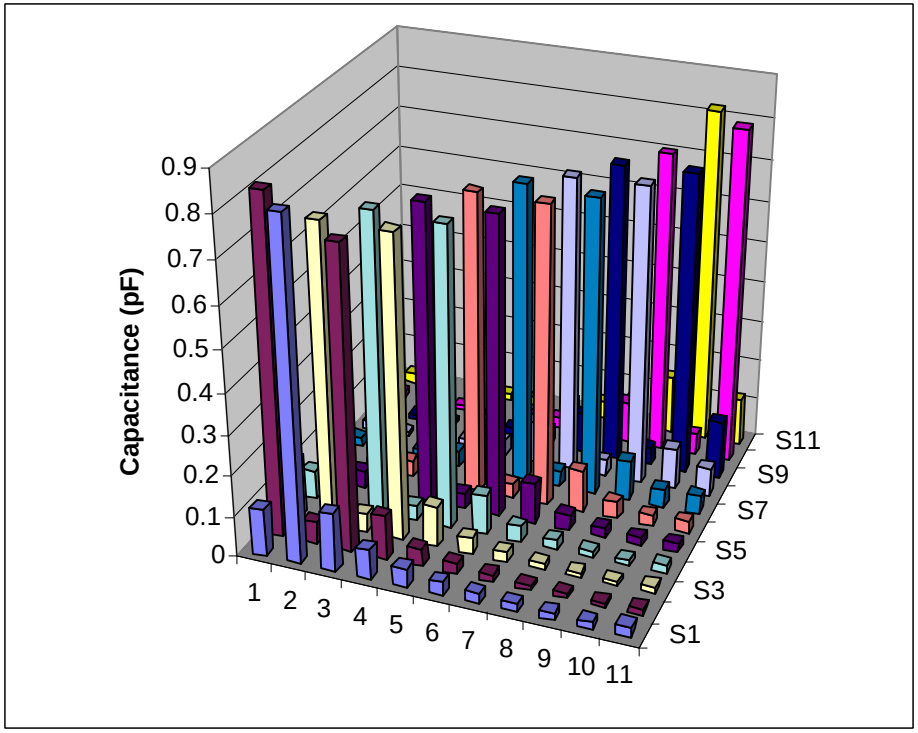
SPICE Capacitance matrix:

Diagonal elements = capacitance to ground
Off-diagonal elements = coupling capacitance

Extracted Matrix Elements for Long Needles



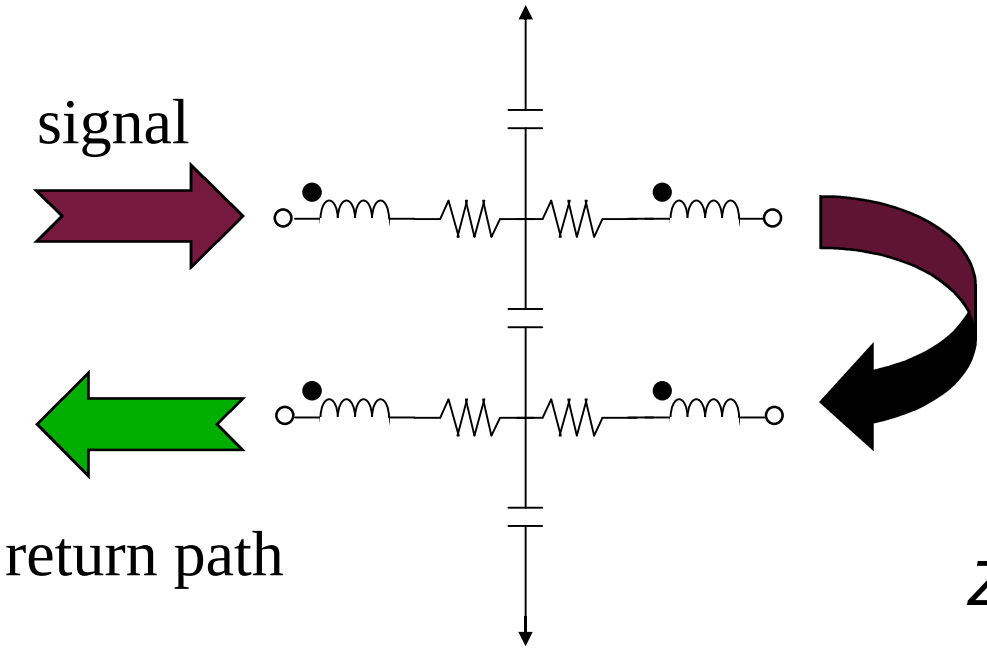
Inductance



Capacitance

L_{11} = 39 nH
L_{12} = 27 nH

Effective Characteristic Impedance for Two Needles



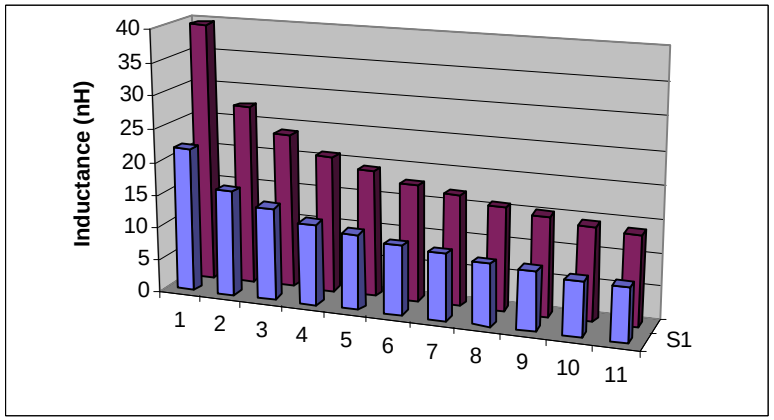
$$Z_0 = \sqrt{\frac{(L_{11} + L_{22} - 2L_{12})}{C_{12}}}$$

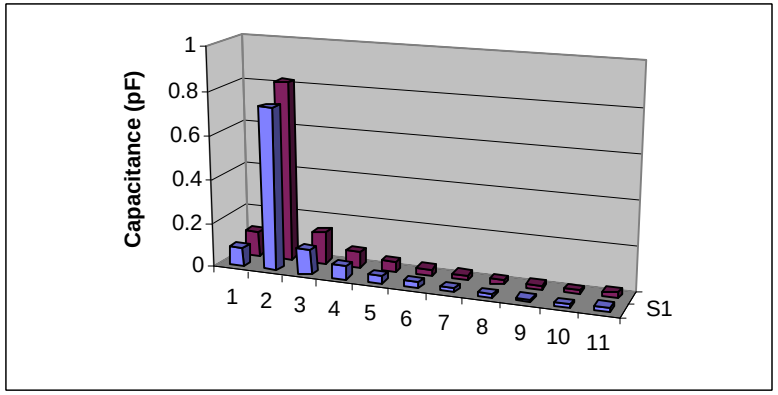
$$TD = \sqrt{(L_{11} + L_{22} - 2L_{12})C_{12}}$$

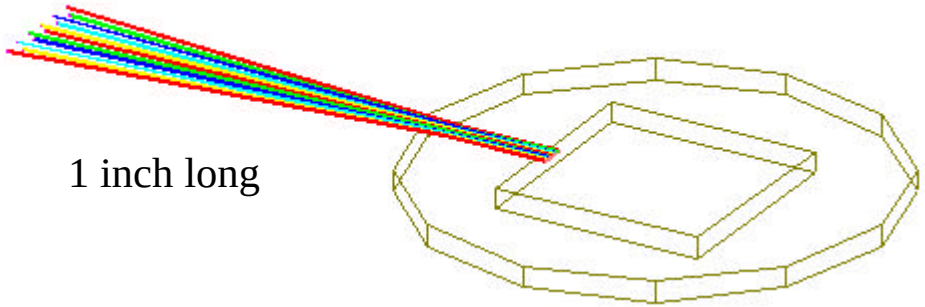
$$Z_0 = 173 \ \ Ohms$$

$$TD = 0.139 \ \ n\,\mathrm{sec}$$

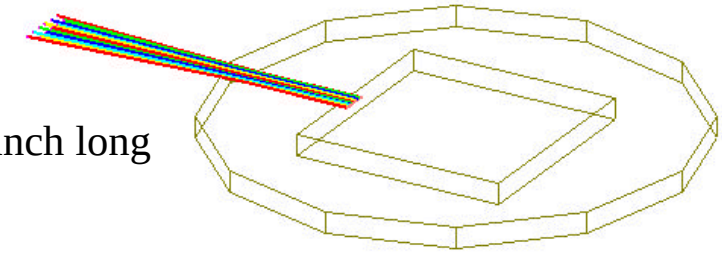
Comparison for Half Pin Length







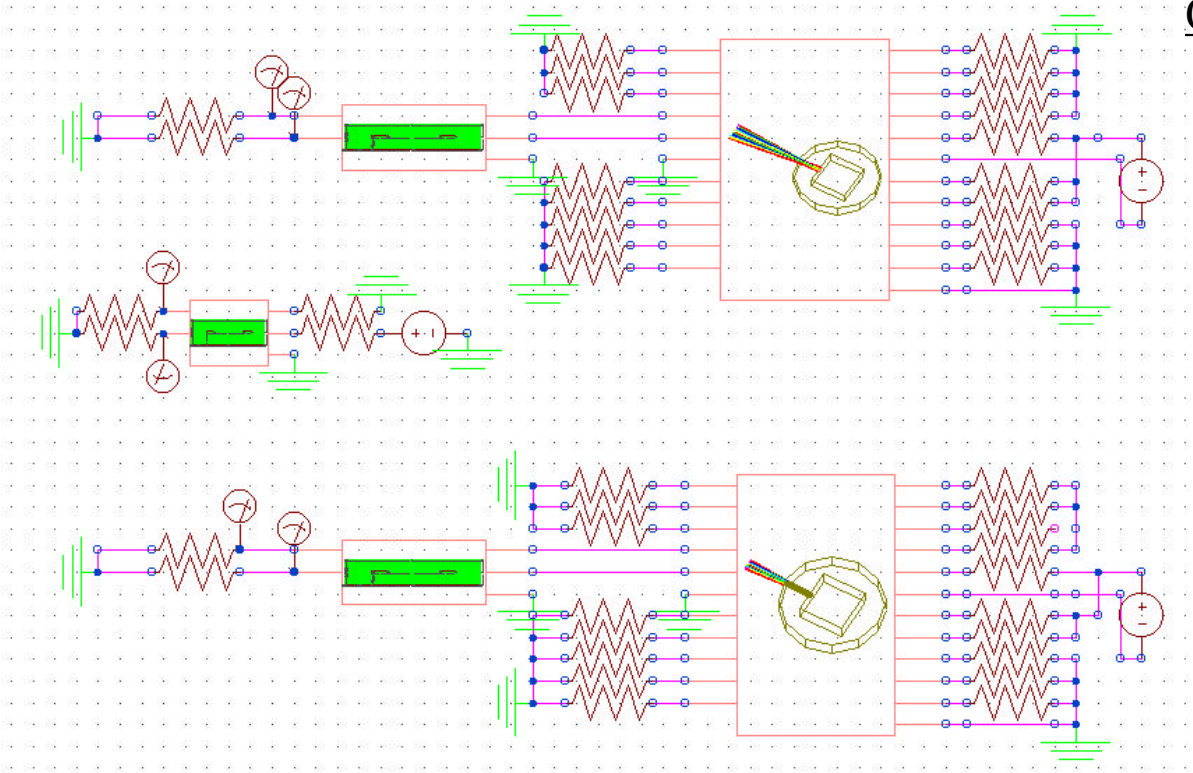
1 inch long



0.5 inch long

	Long	*Short*
Z_0	173 Ohms	122 Ohms
TD	0.139 nsec	0.09 nsec

Simple Circuit Model



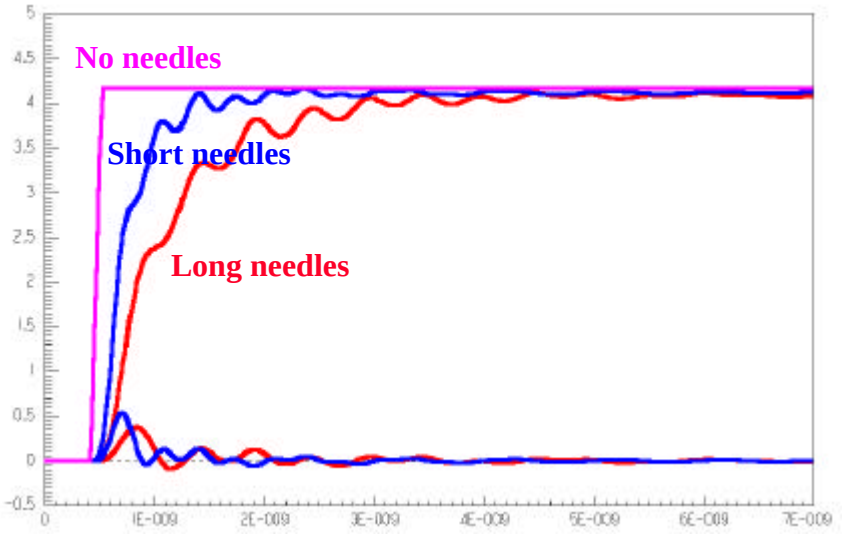
Compare three cases:

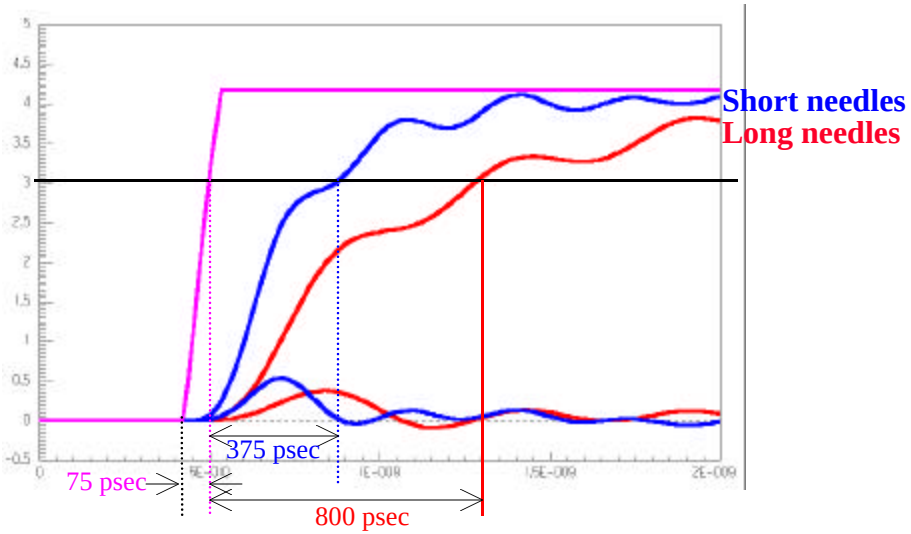
- no probe needles
- 0.5 inch long probe needles
- 1.0 inch long probe needles

Conditions:

- 3 drivers switching simultaneously using same ground pin
- 10 Ohm drivers into 50 Ohm lines
- all other lines tri-state open
- 100 psec rise time
- quiet line is tri-state open
- ground pin between 1 driven line and 2 driven lines

Simulation Results: Far End Signals





Summary:needles dominate BW and noise performance limitations

- current generation needles have:
  - ~800 psec intrinsic rise time (440 MHz BW)
  - 0.5 v noise on quiet line

- reducing length by 50% results in:
  - ~2x increase in BW: 375 psec rise time
  - coupled noise on quiet line reduced to 0.375v

Conclusions

- 2D and 3D field solvers can be used to create circuit models for the probe card components
- Circuit models and simple simulations can identify significant and insignificant factors
- Even at 25 mil pitch, cross talk is so small, no need for guard traces
- Largest source of noise, bandwidth limitation are in the needles
- Short needles are better than long needles
- Specifics of performance also affected by device driver models, # of SSO, which can be combined with probe card models for application specific simulations