# RF Wafer Probing Experiences and their Application to High Speed Digital ICs

**Presented by Ken Smith**
**Membrane Business Unit Manager**
**Cascade Microtech Inc.**

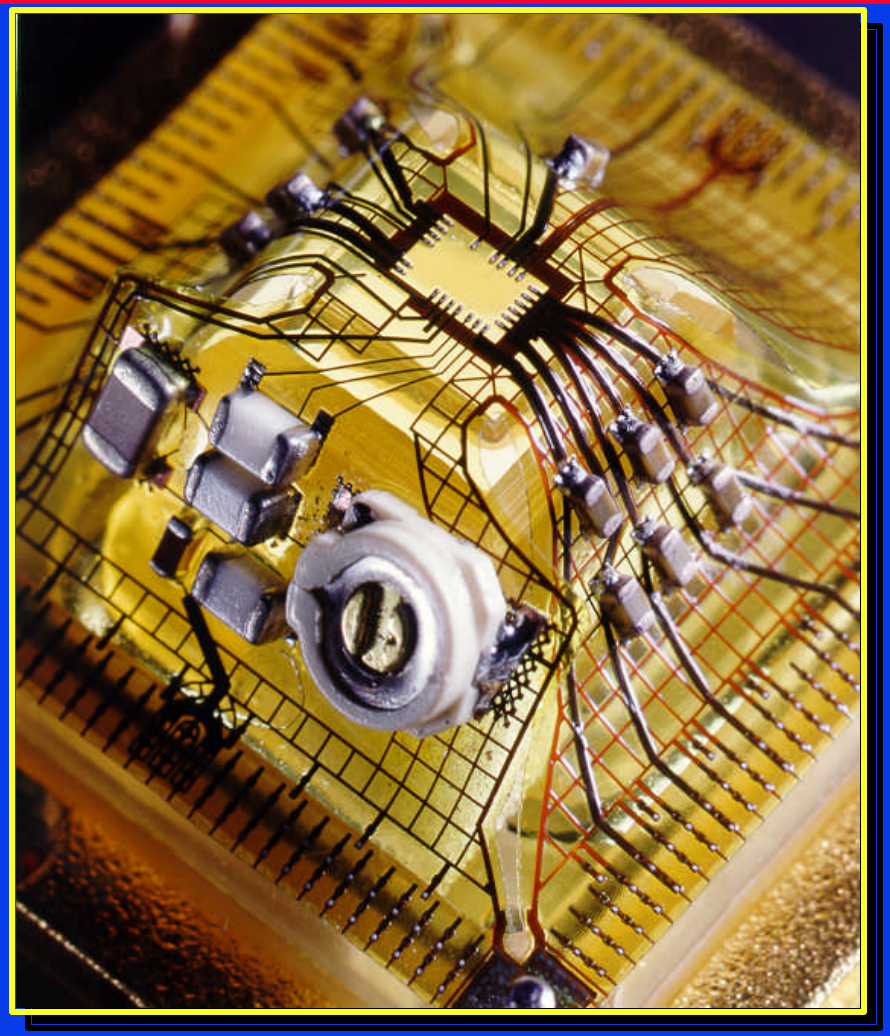
*Advanced Microelectronic Probing Solutions*

CASCADE™ MICROTECH

# Something for Everyone

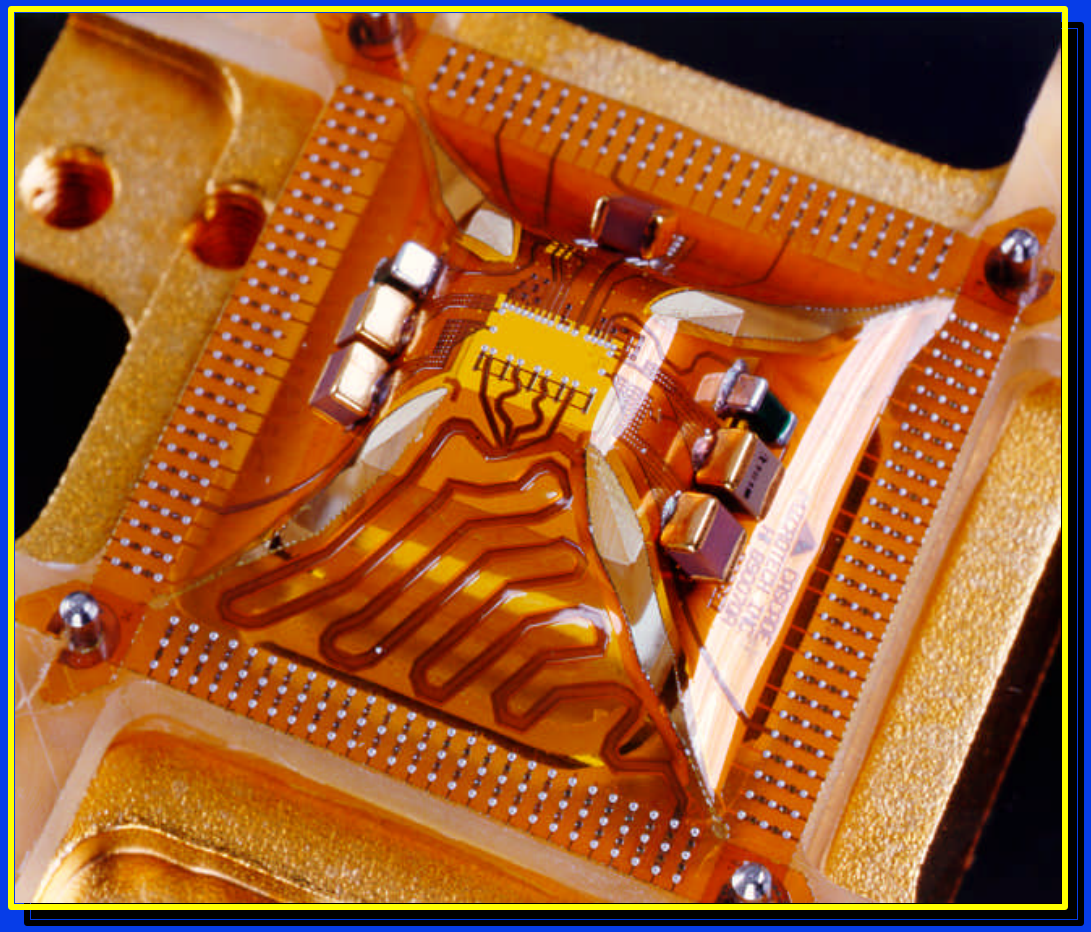
- Leading edge RF applications
- How RF experience applies to HS Digital
- HS digital applications
  - Key issues
  - Common understanding
  - Some technology independent solutions
- Keep it fun

# Typically Strange RF Application



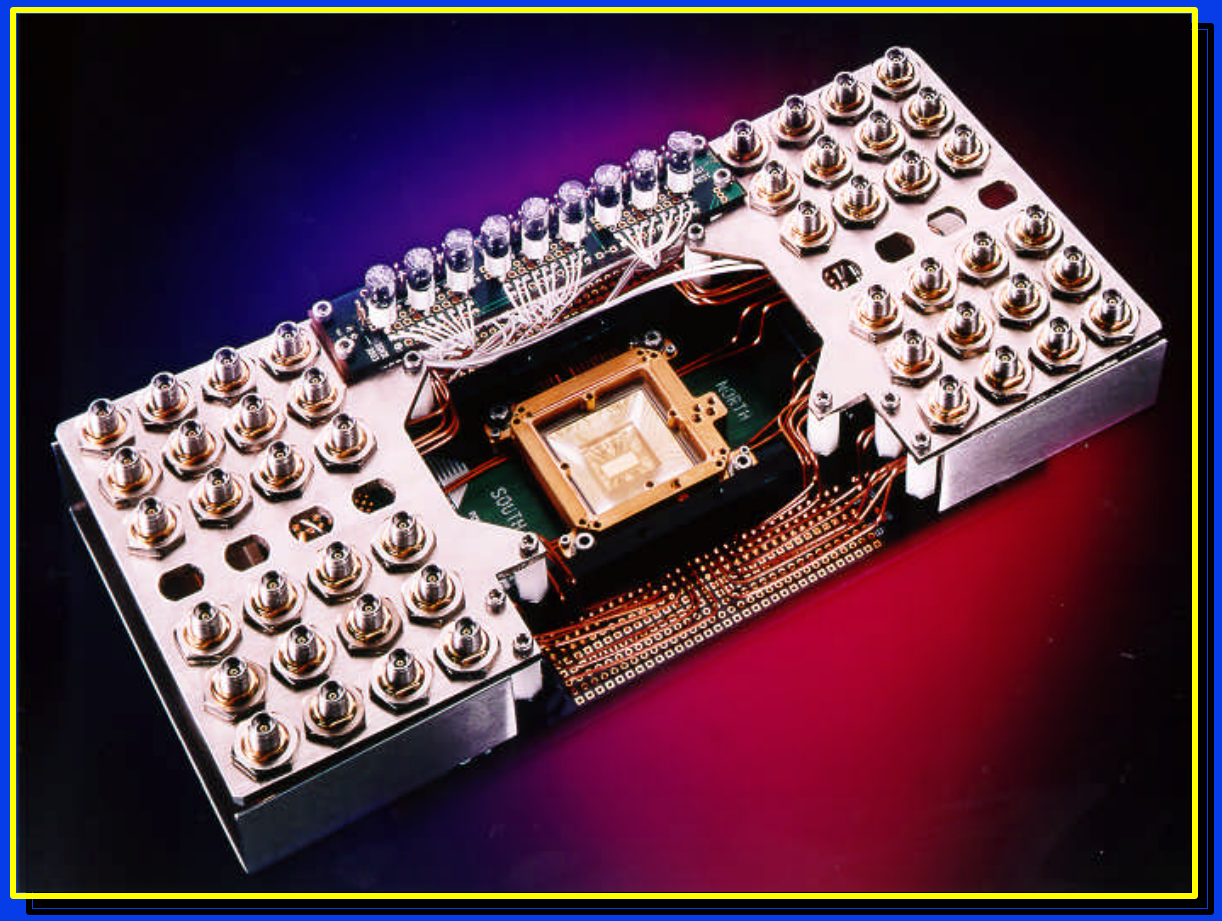
- Bypass capacitors close
- Inductors and termination resistors
- Even a trimmer capacitor!

# 1/4 Wavelength Matching Network



- PCS Power amplifier for CDMA
- Impedance transformation from 2.5 to 50 ohms at 1900 MHz

# Bleeding Edge RF Communications Applications



- 30 RF lines ~ 5 GHz
- 200 AC lines ~ 500 MHz
- 400 I/O solder ball arrays

*Advanced Microelectronic Probing Solutions*

CASCADE MICROTECH

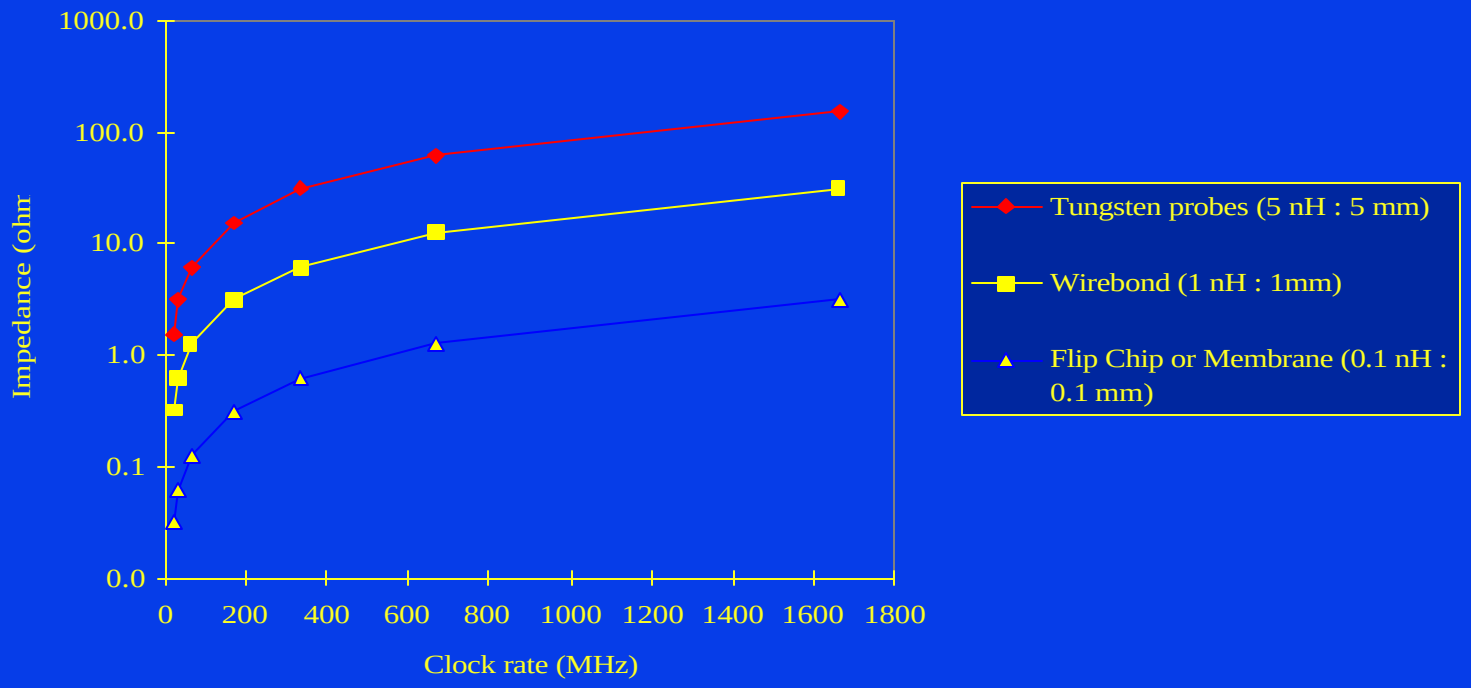
# RF Probe Issues are the same as IC Packaging Issues

- Ground & Power noise
- Crosstalk and impedance matching
- Bandwidth and delay matching
- HS Digital issues are identical except impedance is typically 50 ohms

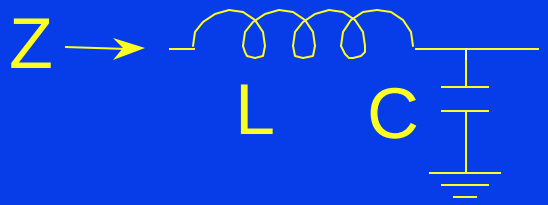
# Ground and Power Noise Model Assumptions

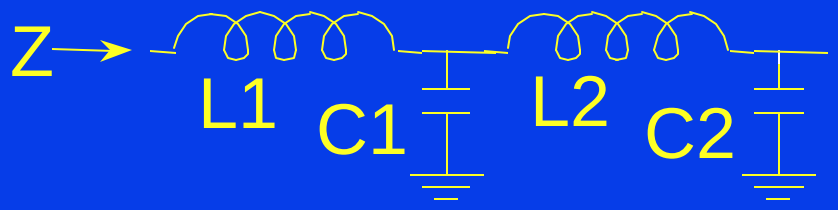
1. Equivalent frequency = 3 x clock rate
2. Rise time = 0.35 / Frequency
3. Simple inductor Z = 2 $\pi$ F * L
4. Inductance ~ 1 nH / mm

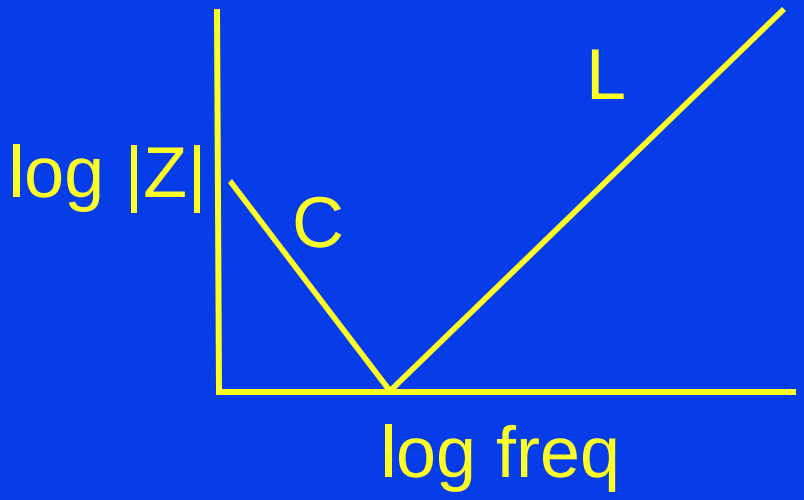
# Impedance of Probes and Interconnects vs Clock Rate

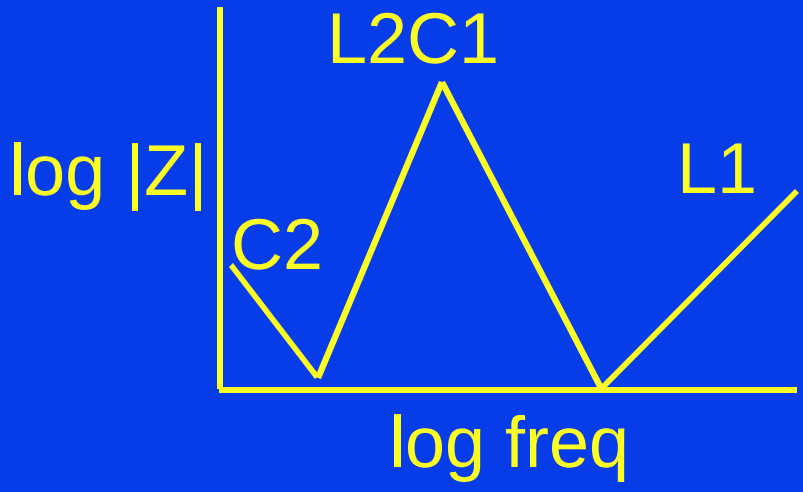


# Beware of Resonances in Power Bypass Networks

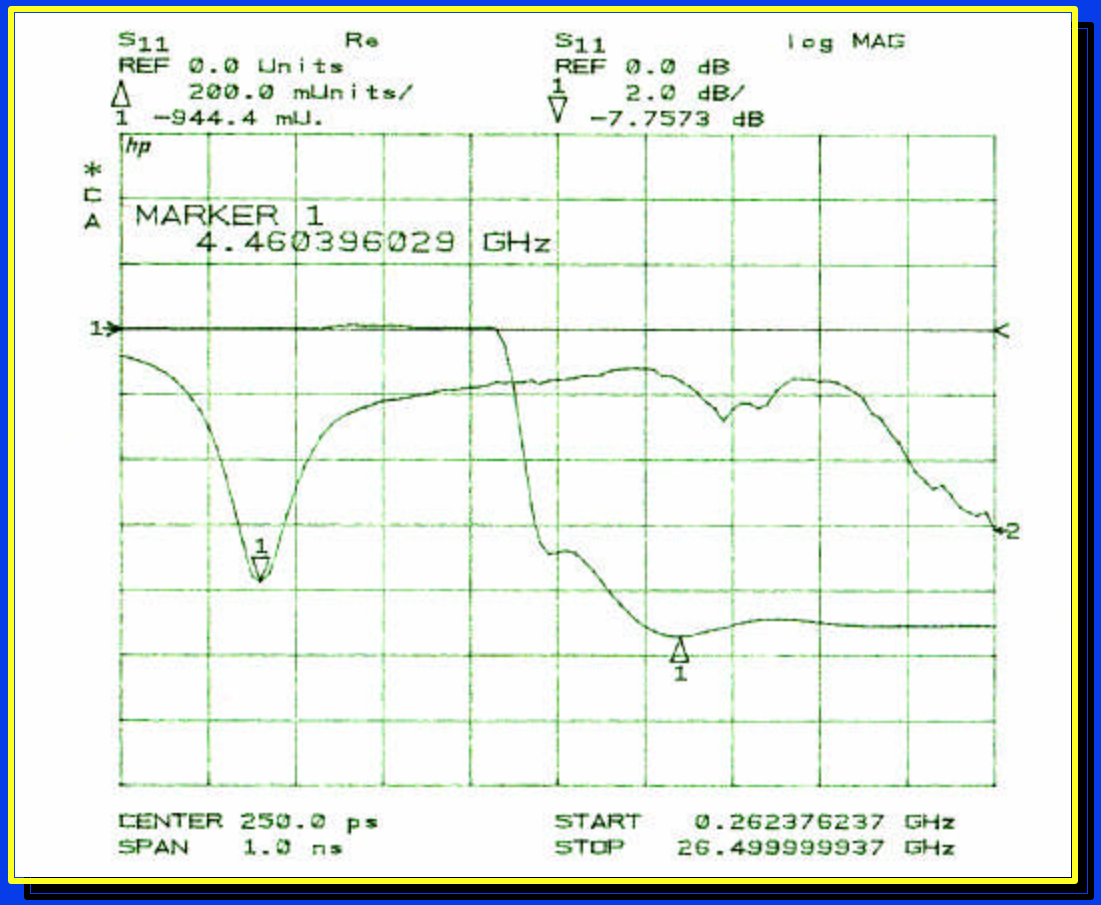


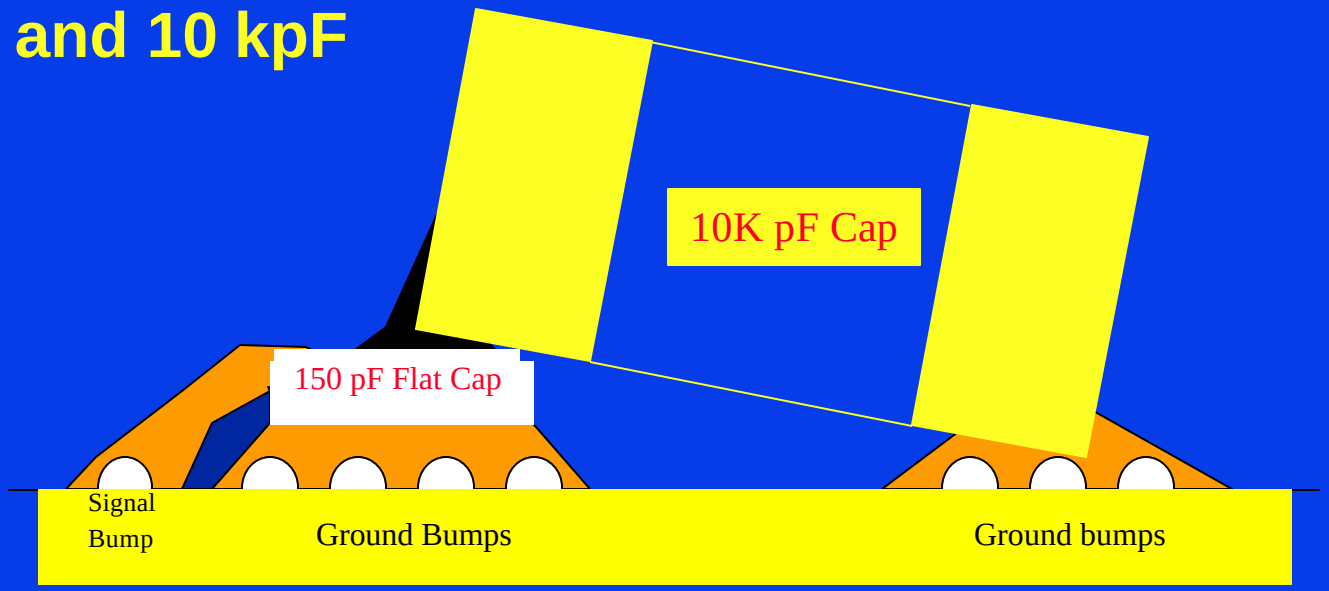
# Response of Power Bypass Structures



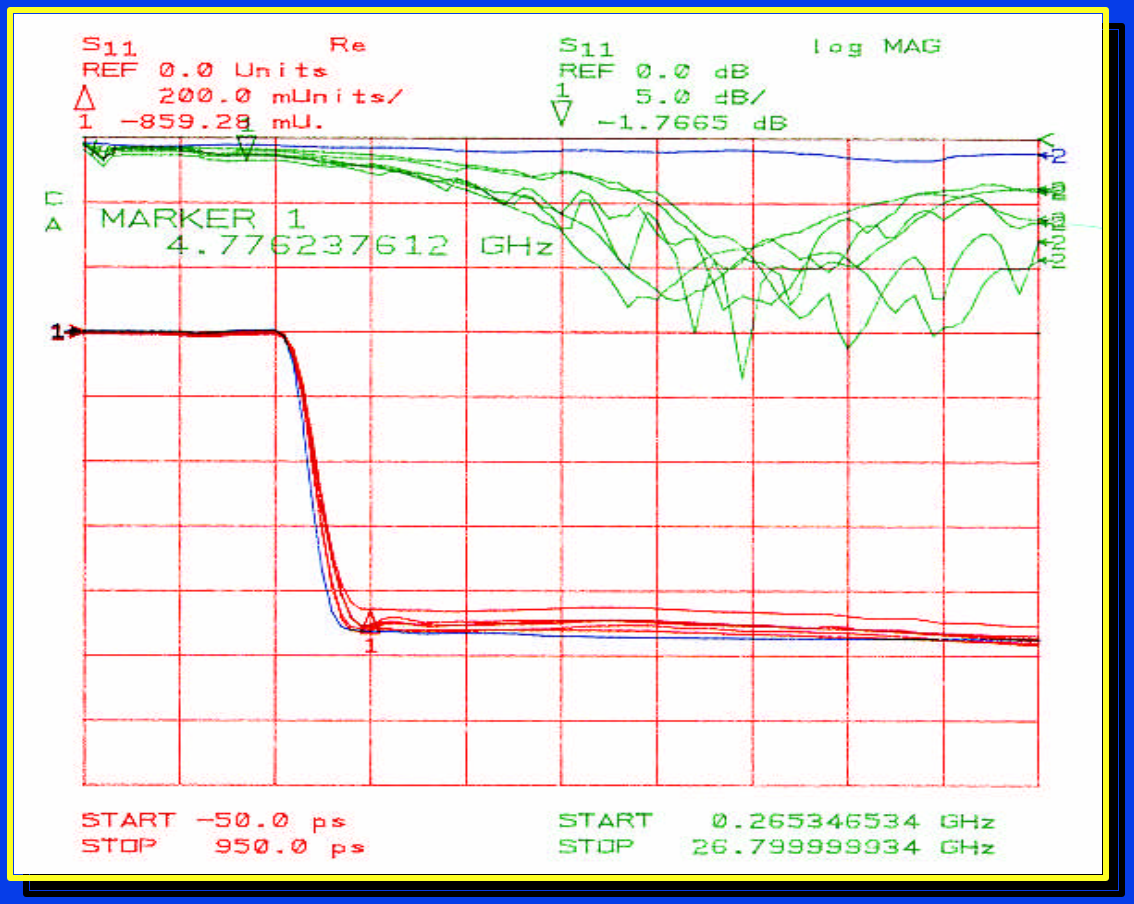

**Time and Frequency response of standard bypass caps and low impedance power lines**

# High Performance Two Stage Bypass Capacitors

- **Self resonant frequency greater than 10 GHz**
- **150 pF MIM and 10 kpF ceramic**



# High Performance Power Structures



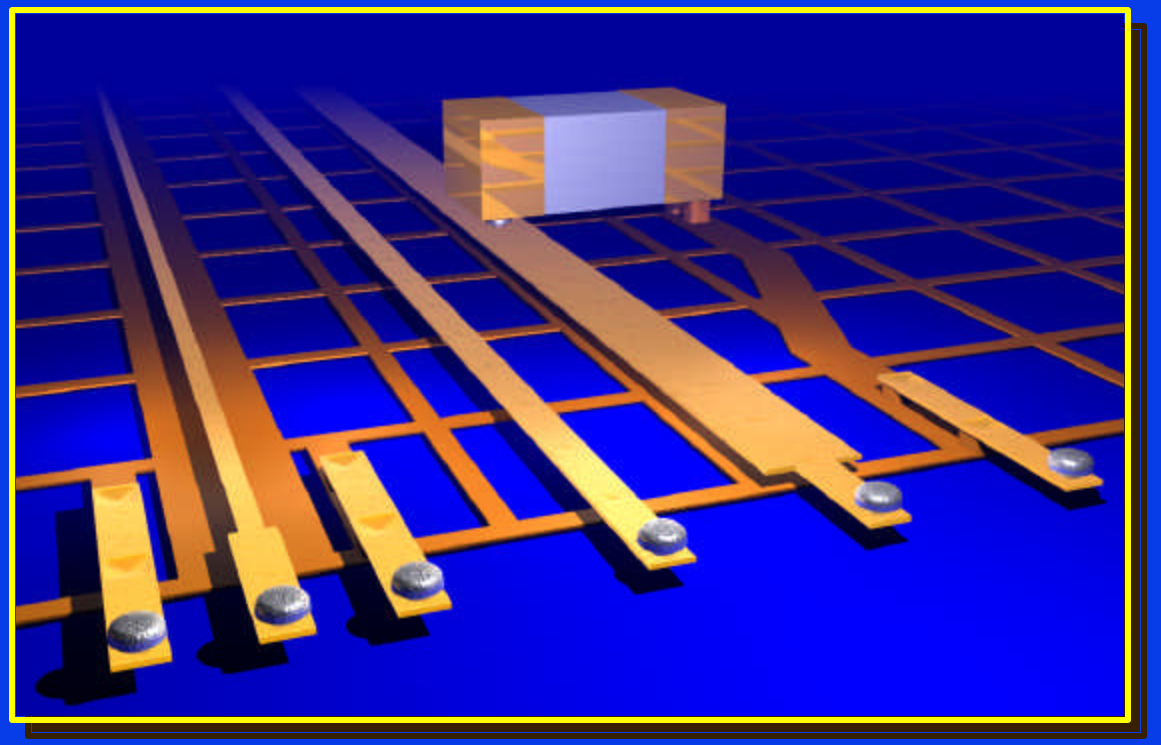

**Time and frequency response of two stage bypass structure**

# General Guidelines for HS Digital Bypass Capacitors

- Minimize power inductance (distance and impedance)
- Minimize ground return inductance
- Select cap sizes in stages to avoid resonance

# Thin Film Signal Trace Model

- Power impedance
- Bypass ground return
- Ground length



# Estimating L and C Parasitics

$$Zo = \sqrt{\frac{l}{c}} \quad \text{and} \quad t = \sqrt{lc}$$

where Zo = characteristic impedance of the line

l = inductance per unit length

c = capacitance per unit length

t = delay per unit length

**L = T Zo** **C = T/Zo**

where L = total inductance

C = total capacitance

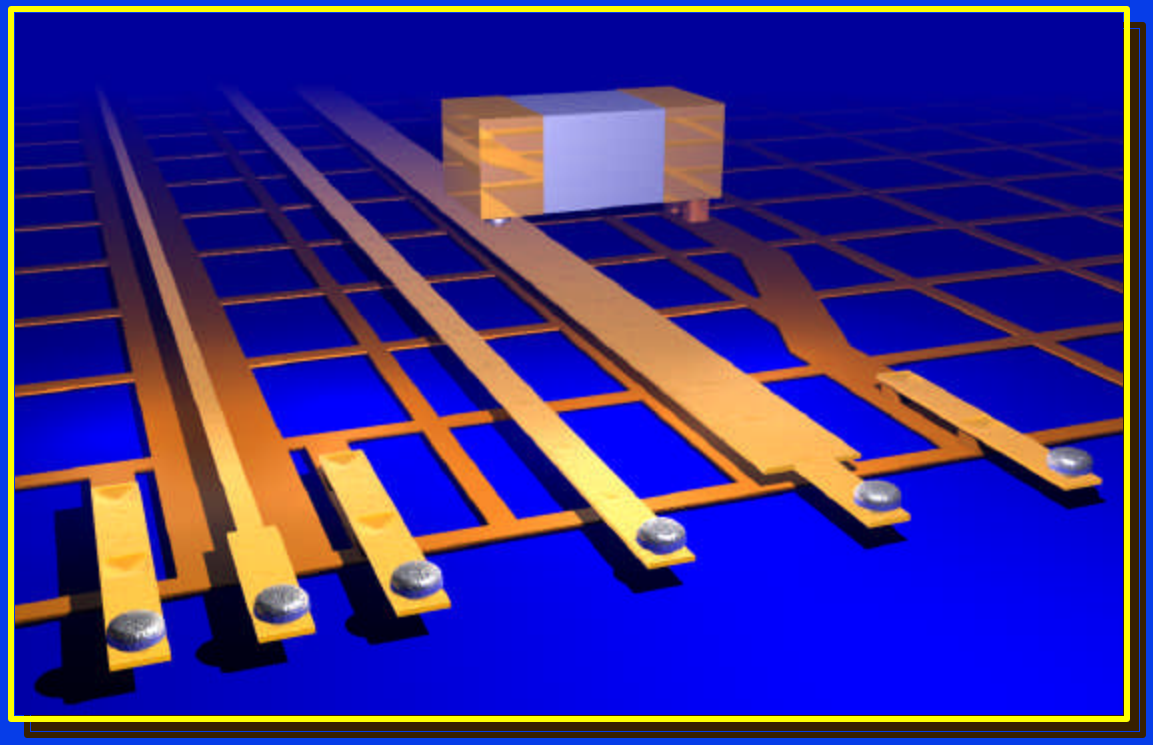
T = total delay

# Crosstalk is Primarily due to Common Lead Inductance

- Shared ground or power paths create a common reference voltage
- Use independent ground and power returns and / or
- Use low impedance ground and power returns

# Crosstalk Model

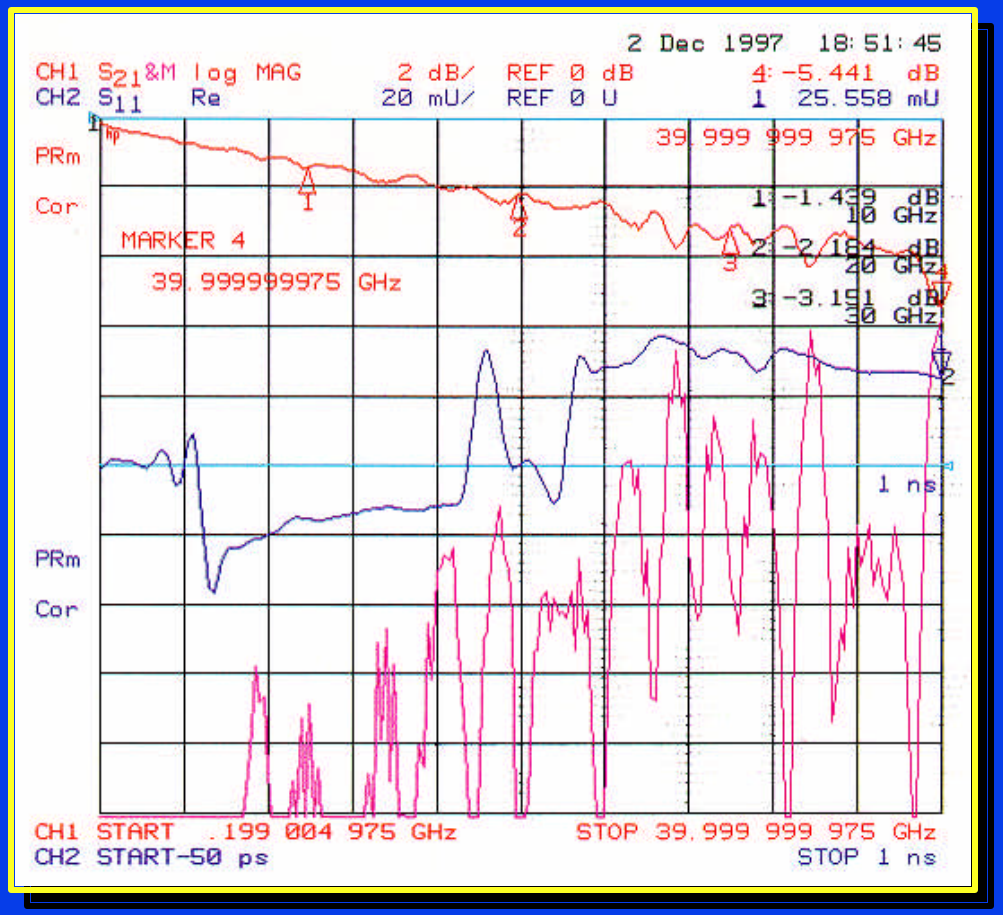
- Independent grounds
- Ground length short
- Low inductance grounds



# Bandwidth or Rise Time Limitations

- Resistive or radiated losses (insertion loss: S21)
  - Skin effect
  - Poor ground coupling
- Reflected losses (return loss: S11)
  - Impedance mismatches
  - Ground inductance

# Peak RF Membrane Performance to Date




- Insertion loss (S21)
- Return loss (S11)
- 4 dB @ 38.8 GHz
- Super control on mechanical dimensions & transitions

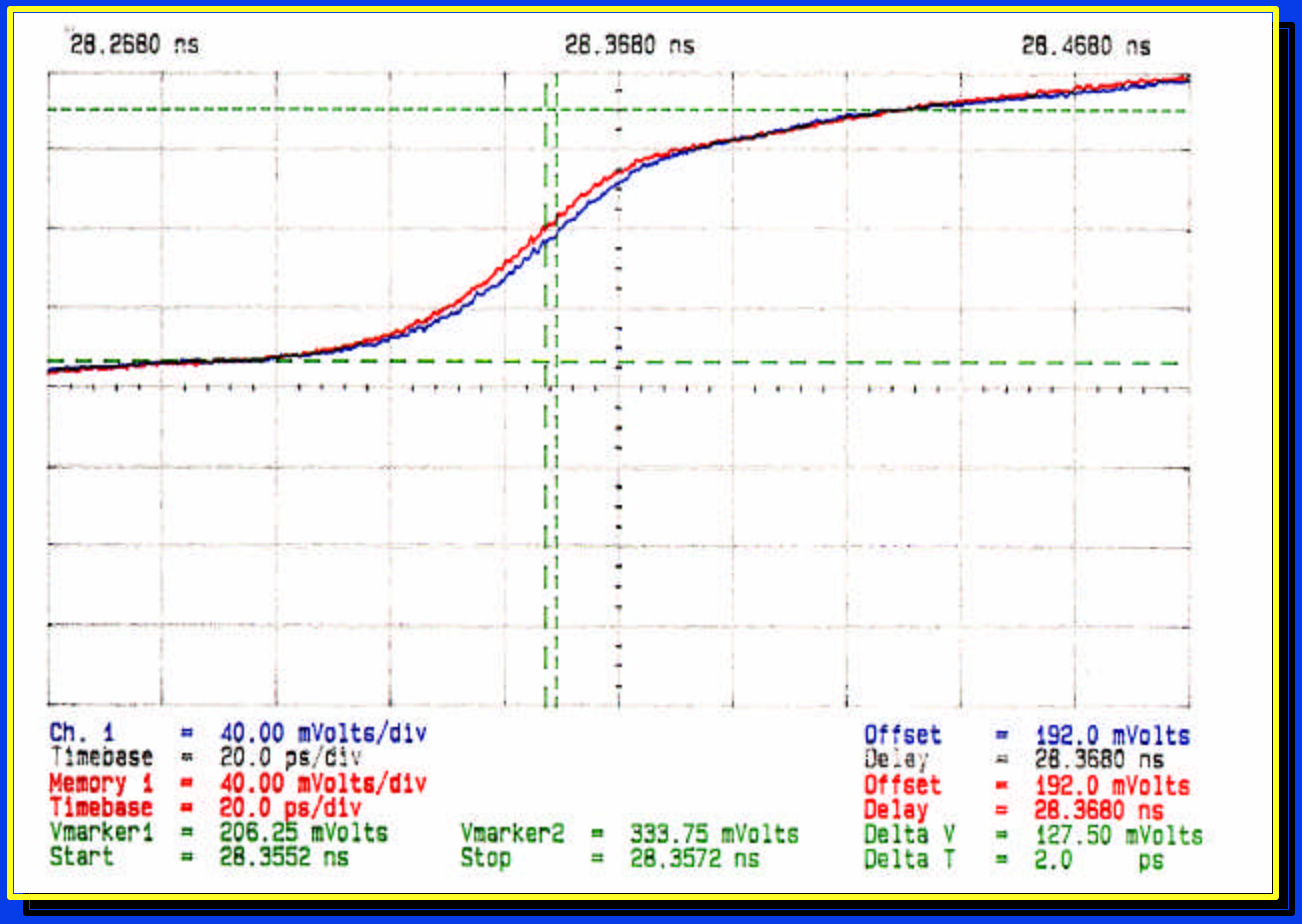
# How to Minimize Signal Losses

- Skin effect:  wide, short conductors
- Ground coupling:  capture fields, “think antenna”
- Impedance mismatches: current flows in the space between conductors
- Ground inductance:  wide, short ground returns

# Signal Line Delay Matching

- 10% to 100% of one rise time is a typical spec.
- Communications bit error rate is most demanding
- Velocity determined by effective dielectric constant and ground return path
- Microstrip is faster than stripline, but more lossy
- Gridded grounds are slower and dispersive
- Skin effect rolls off leading edge and effects 10-90% rise time

# Delay match measurements

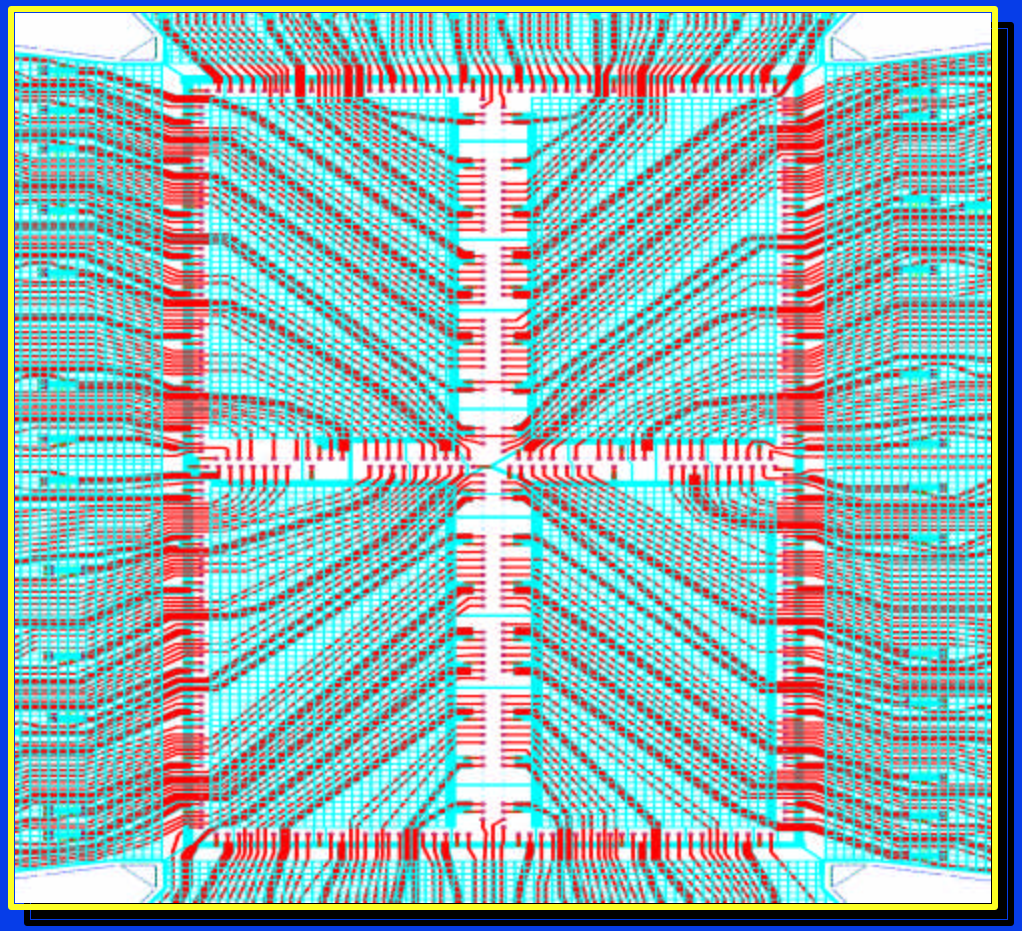



- Cables get expensive
- Calibration can help, especially if not differential

# Some High Speed Digital and High Pin Count Applications

- Fast SRAM
- Chip Scale Packages
- LCD Drivers
- MCM Bare Board Test
- High speed ASICS & Microprocessors

# VLSI Pyramid Probe

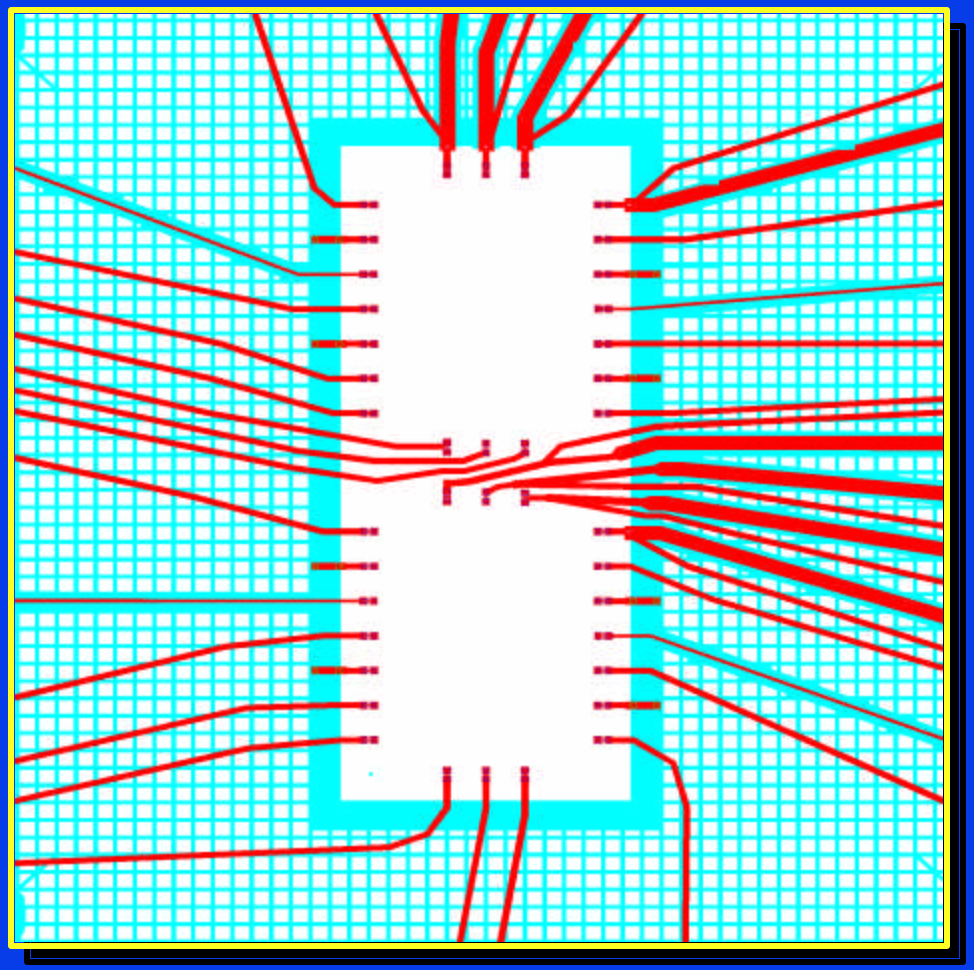


- 2 x 2 FSRAM array
- Max. die size - 44.2mm
- 1040 I/Os

*Advanced Microelectronic Probing Solutions*

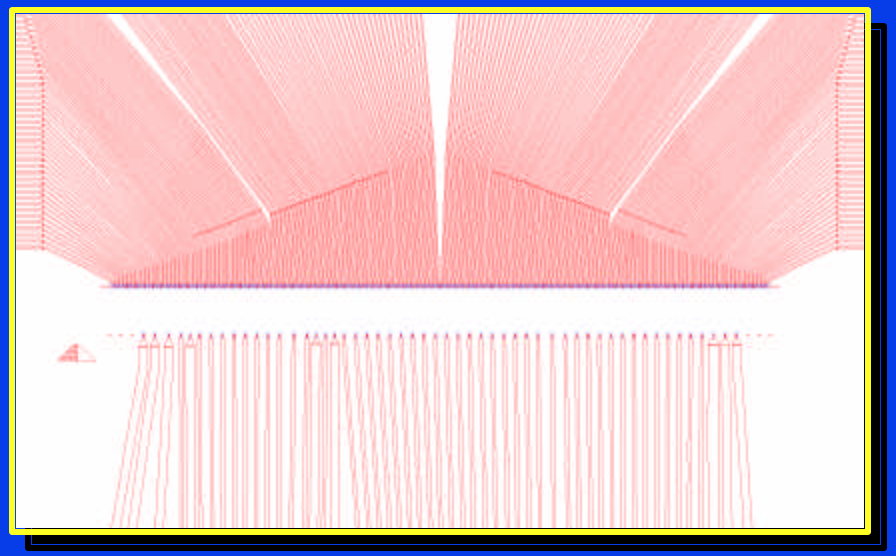
CASCADE MICROTECH

# RF Functional Test of Chip Scale Packages



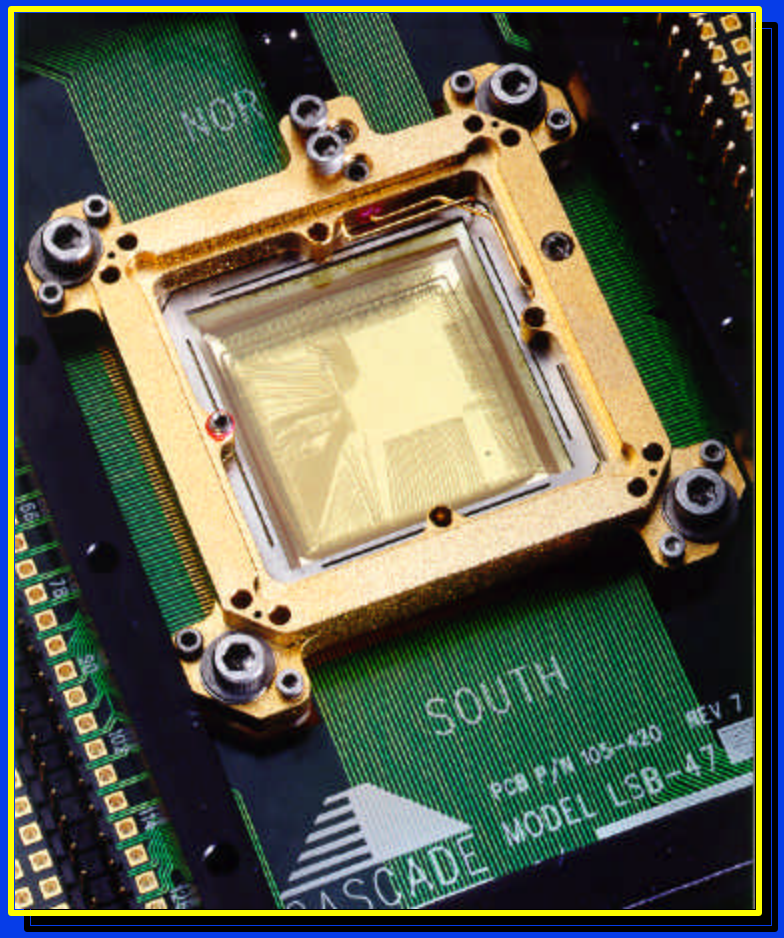
- **Multi-die testing of a CSPs on tape substrate**

# Pyramid Probe for LCD Drivers



- Probing gold bumps for TAB
- 64 micron pitch

# MCM (Multi Chip Module) Probe

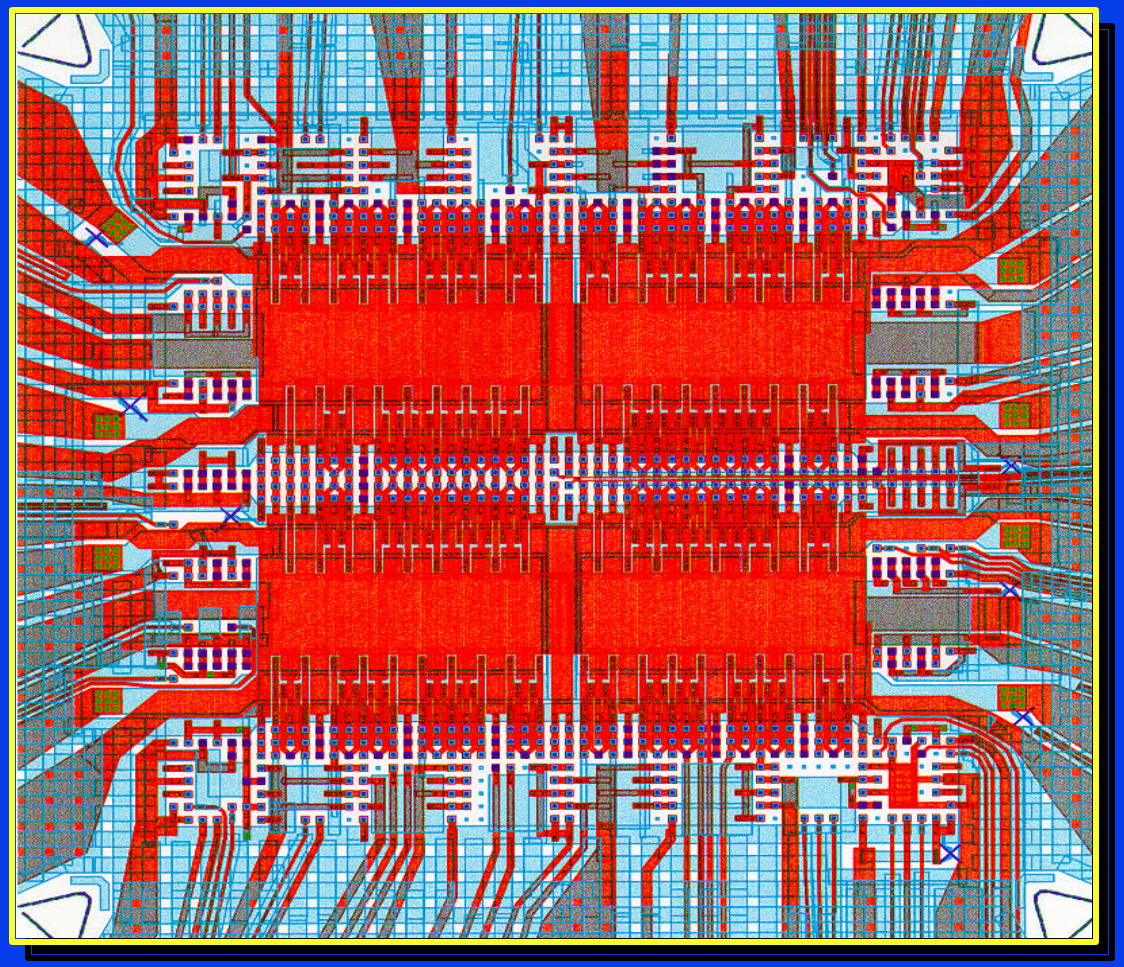



- 500 plus pads
- Full area array combined with peripheral pad pitches down to 65 microns
- No pad damage for higher wirebond yields

*Advanced Microelectronic Probing Solutions*

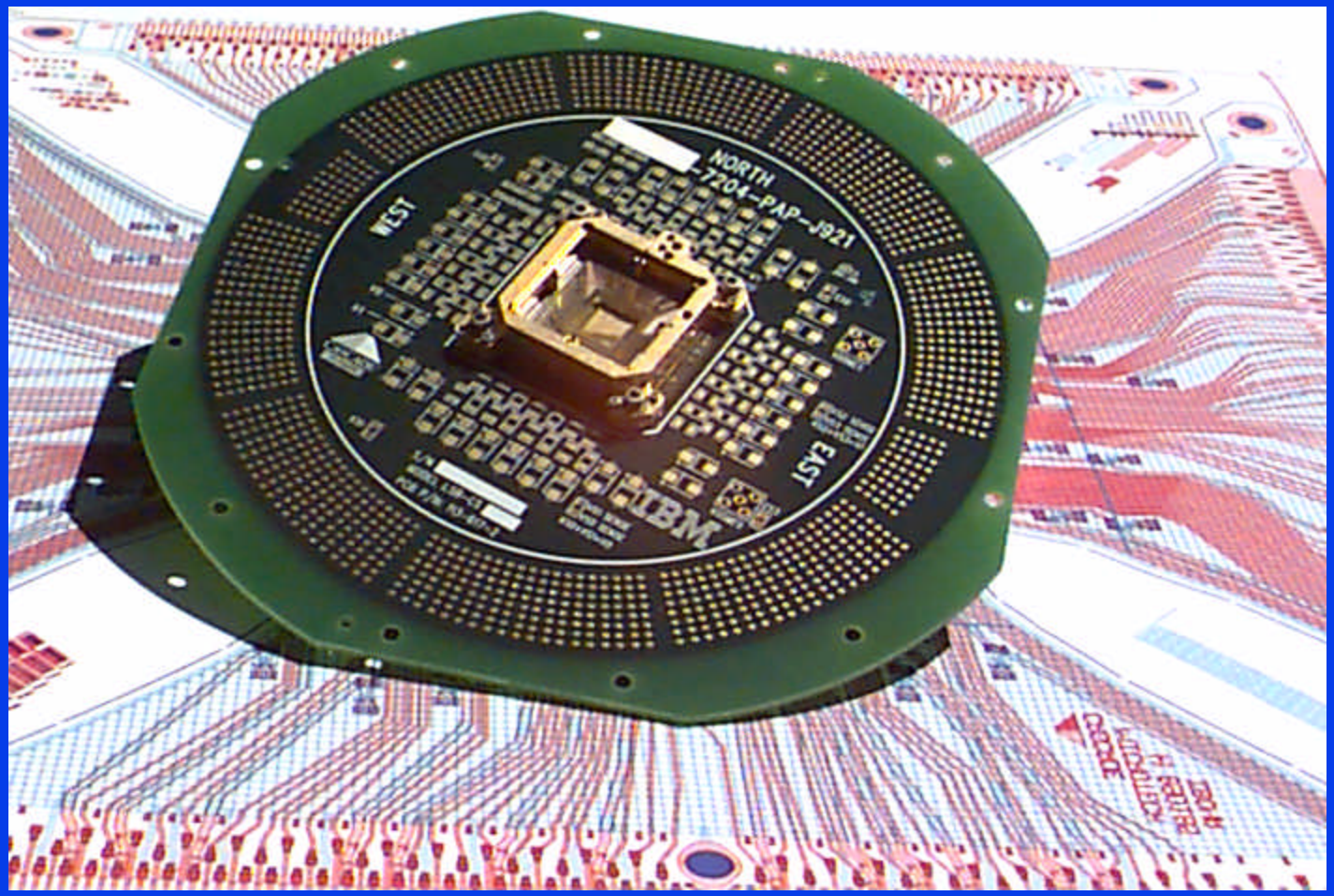
CASCADE MICROTECH

# 100+ Watt ASIC for Cray / Silicon Graphics



- Interlaced power and ground planes
- 2 GHz at-speed test
- Minimal IR drop on supplies

# Something that looks a little like a probe card (J921)




*Advanced Microelectronic Probing Solutions*

CASCADE MICROTECH