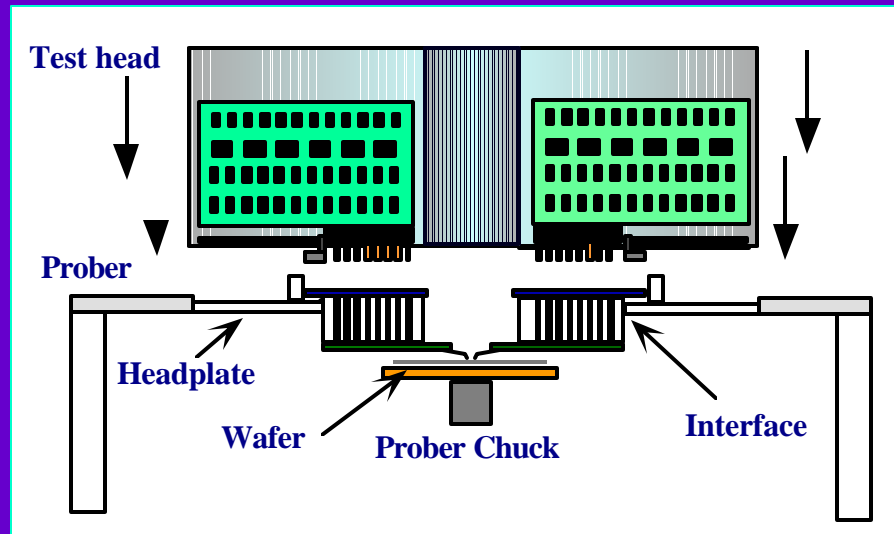


A New Tester-Prober Interface Paradigm: Direct Docking

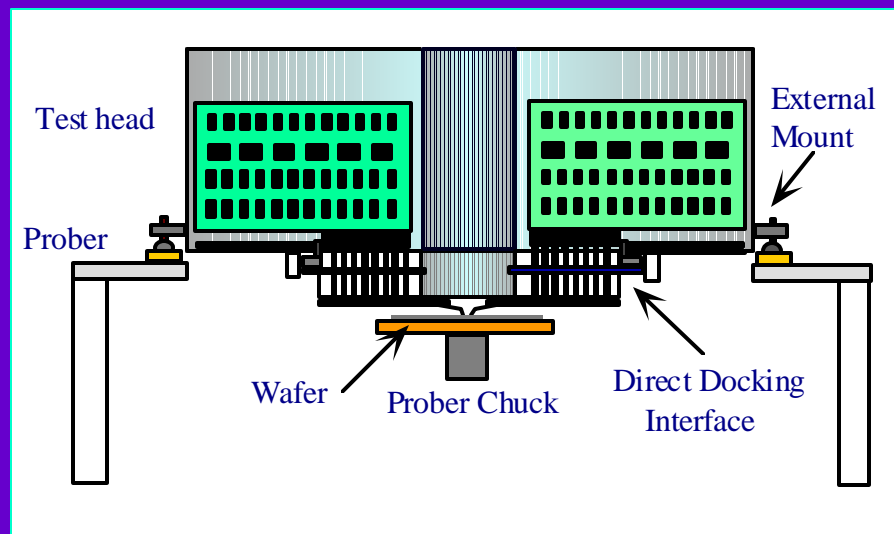
Doug Lefever, Motorola
Roger Sinsheimer, Xandex

What is Direct Docking?

Conventional System



Direct Docking System



What is Direct Docking?

Two Differences

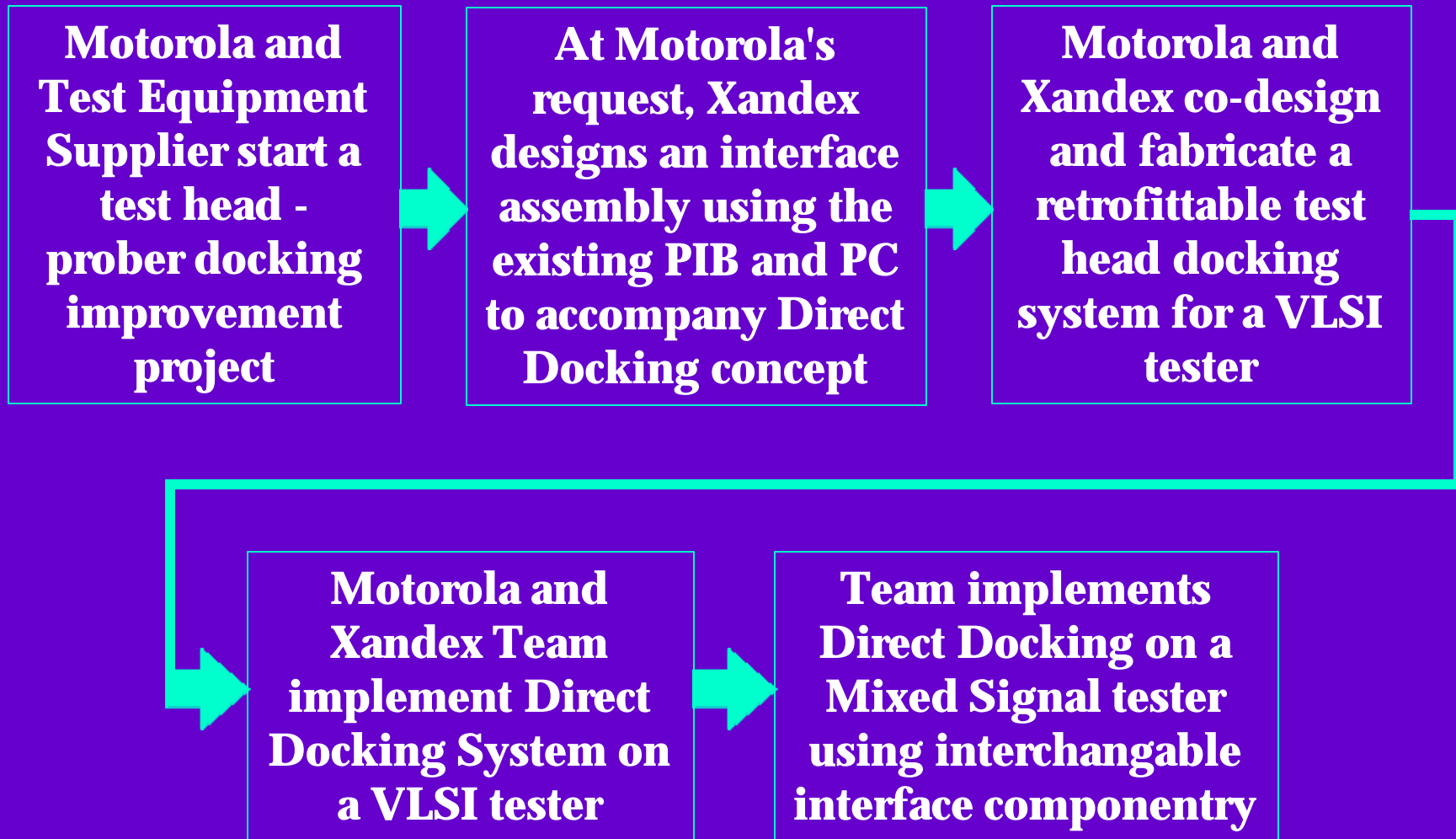
Conventional System

- Interface components reside in prober head plate
- Attachment of test head to prober located at interface

Direct Docking System

- Interface assembly attaches solely to test head
- Attachment of test head to prober is externally located

Project Background

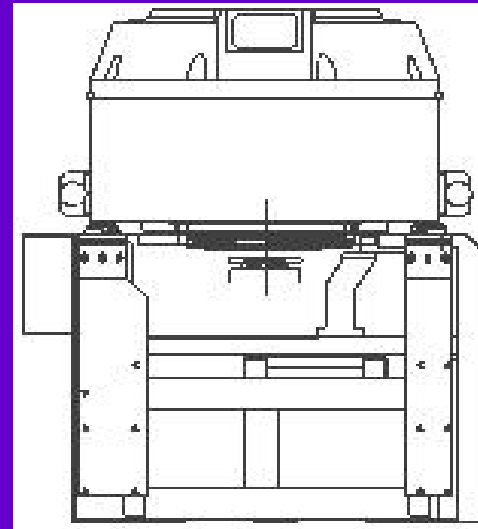


Project Background



**VLSI Direct
Docking System**

side view



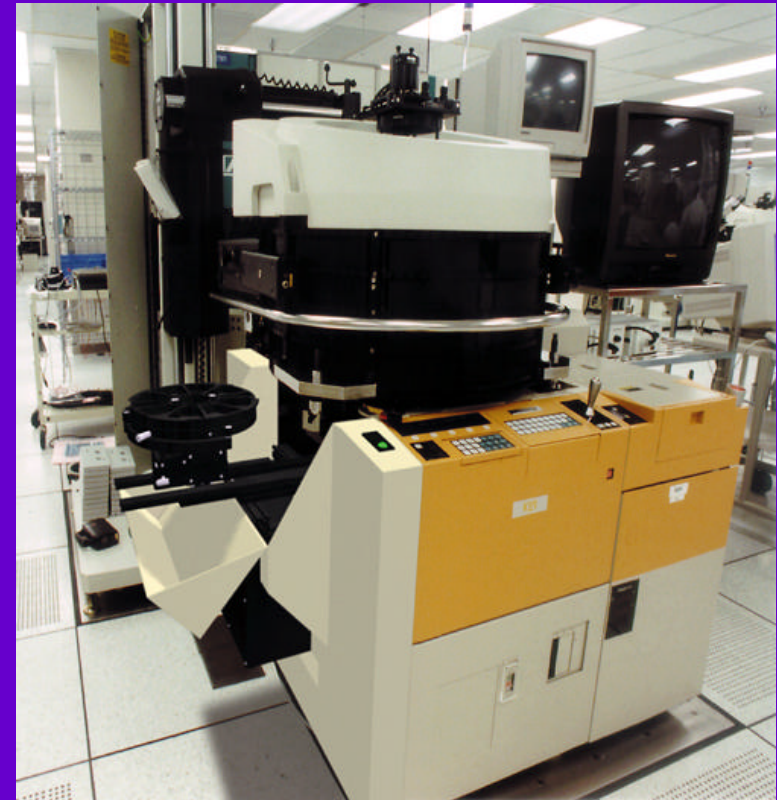
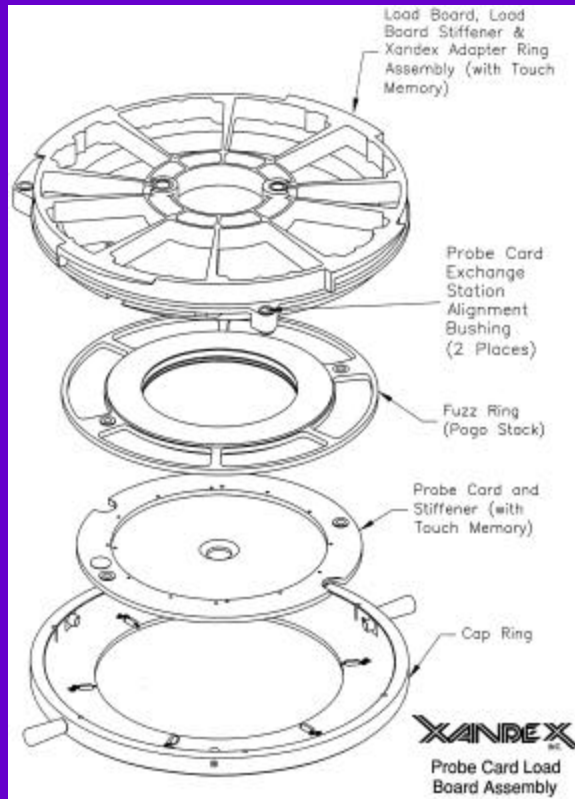
**Mixed Signal Direct
Docking System**

Motivation

- Set-up times and interface wear
- Probe card deflection from transferred forces of interface
- Vibration
- Shorter electrical paths from test head to DUT
- Compatibility across tester and prober platforms

Set-up Times & Interface Wear

Premise: Eliminating docking/undocking of test head for card changes will improve set-up time and reduce interface wear.



Set-up Times & Interface Wear

Results:

Set-up time

	Time (min) to change PC	Time (min) to change PIB and PC
System A	2.1	3.0
System B	5.9	11.0
System C (APC)	2.4	4.3
Direct Docking	0.75*	1.7*

Interface wear

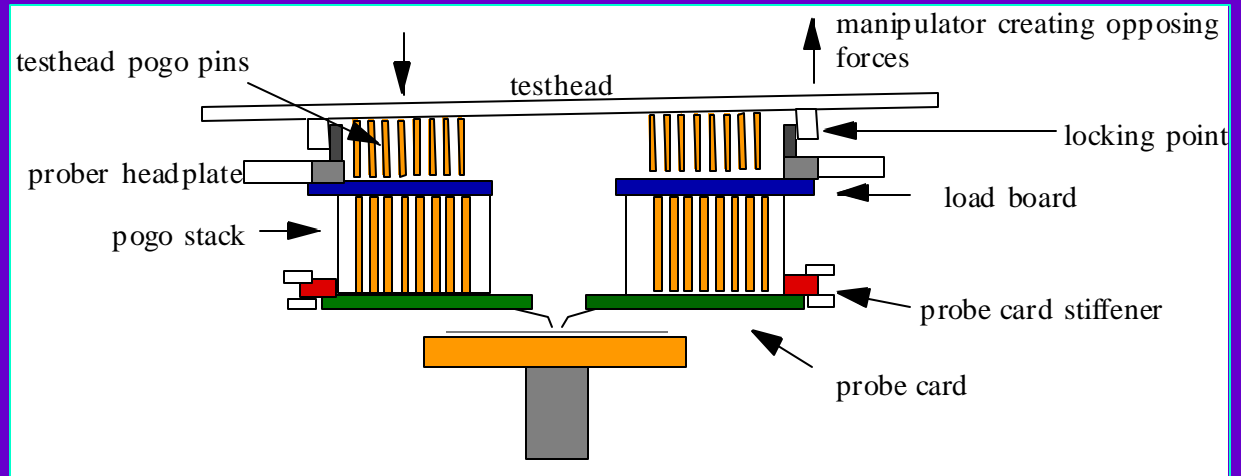
Conventional System average	3.5 months
Direct Docking System	6.8 months

* Direct Docking System times estimated, not measured on production floor

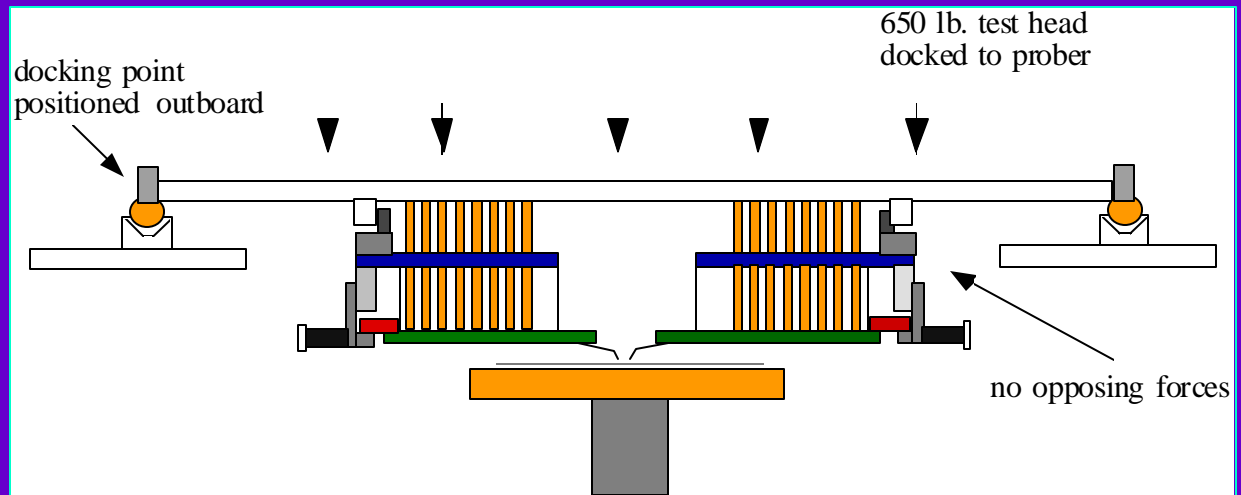
Board Deflection

Premise: De-coupling interface from prober head plate removes probe card deflection from transferred forces.

Conventional system



Direct docking



Board Deflection

Results:

Effect of No Offset
(level & balanced)

	Average ? from Undocked Position (µm)			
	Quad 1	Quad 2	Quad 3	Quad 4
System A	9.0	10.2	11.7	11.0
System B	15.2	22.1	24.0	17.7
Dir. Dock Sys.	1.6	3.5	2.0	3.0

Effect of Planarity
Offset

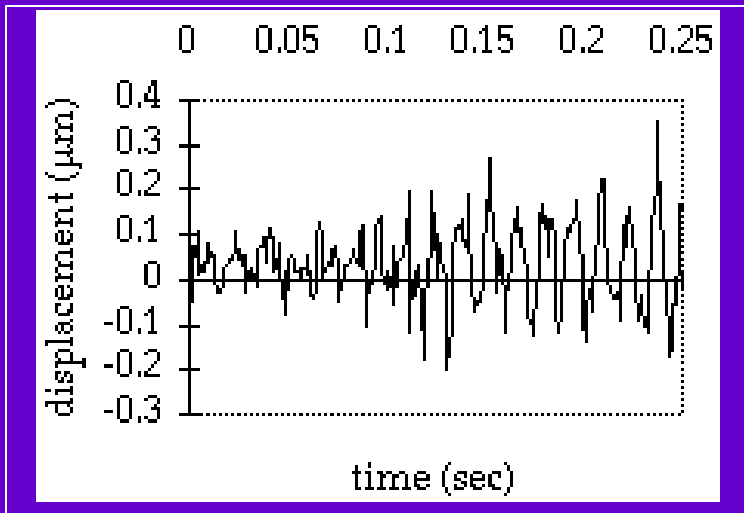
	Average ? from Undocked Position (µm)			
	Quad 1 (2,4,6 deg.)	Quad 2 (2,4,6 deg.)	Quad 3 (2,4,6 deg.)	Quad 4 (2,4,6 deg.)
System A	(10.2,13.4,14.1)	(9.2,9.8,10.8)	(12.9,15.1,18.3)	(8.3,10.6,12.2)
System B	(14.3,13.8,12.9)	(20.0,18.6,16.2)	(26.1,28.2,29.1)	(19.8,23.5,29.8)
Dir. Dock Sys.	(1.2,1.3,0.9)	(3.0,3.6,4.2)	(2.4,2.3,4.0)	(3.7,3.1,3.1)

Effect of Counter-Balance
Offset

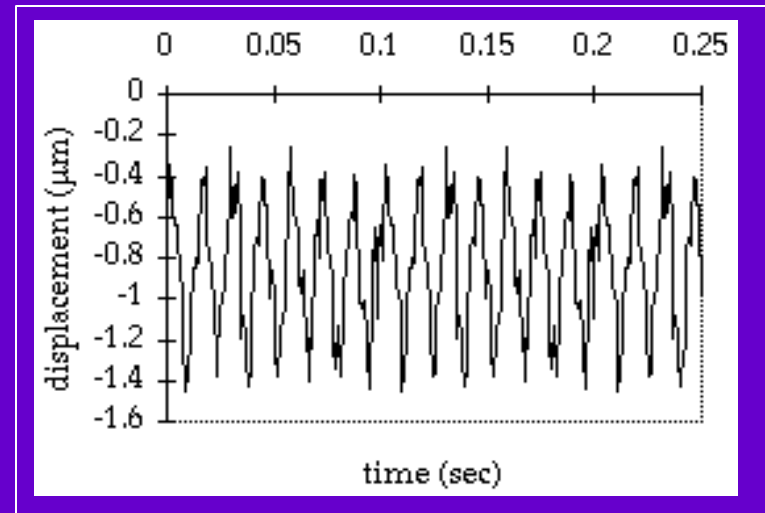
	Average ? from Undocked Position (µm)			
	Quad 1 (+5,+10,-5,-10 lb.)	Quad 2 (+5,+10,-5,-10 lb.)	Quad 3 (+5,+10,-5,-10 lb.)	Quad 4 (+5,+10,-5,-10 lb.)
System A	(9.2,9.9,14.4,19.1)	(10.2,10.6,15.2,19.1)	(11.6,12.2,18.4,20.3)	(10.1,11.9,15.5,18.9)
System B	(16.0,17.4,18.2,22.2)	(18.2,22.0,23.1,27.2)	(17.2,24.2,28.1,32.2)	(18.2,19.1,26.0,30.3)
Dir. Dock Sys.	(2.0,2.7,3.1,2.5)	(1.6,3.9,2.4,2.7)	(1.7,1.0,0.8,2.2)	(3.2,2.1,1.8,3.2)

Vibration

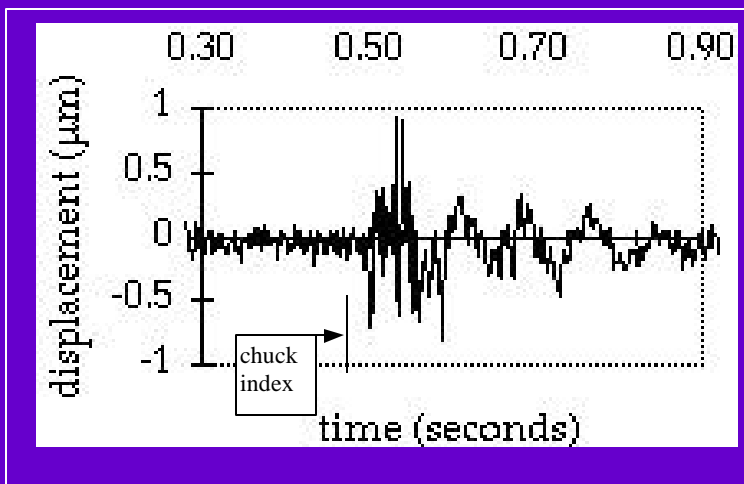
Conventional Static X-direction Vibration



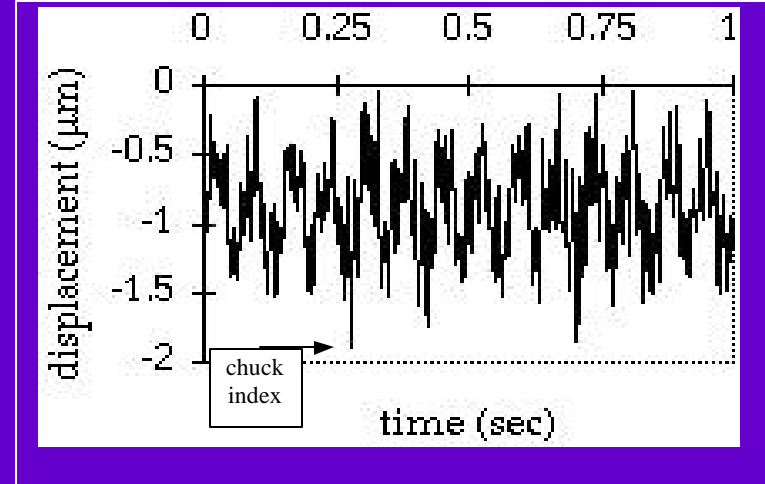
Direct Docking Static X-direction Vibration



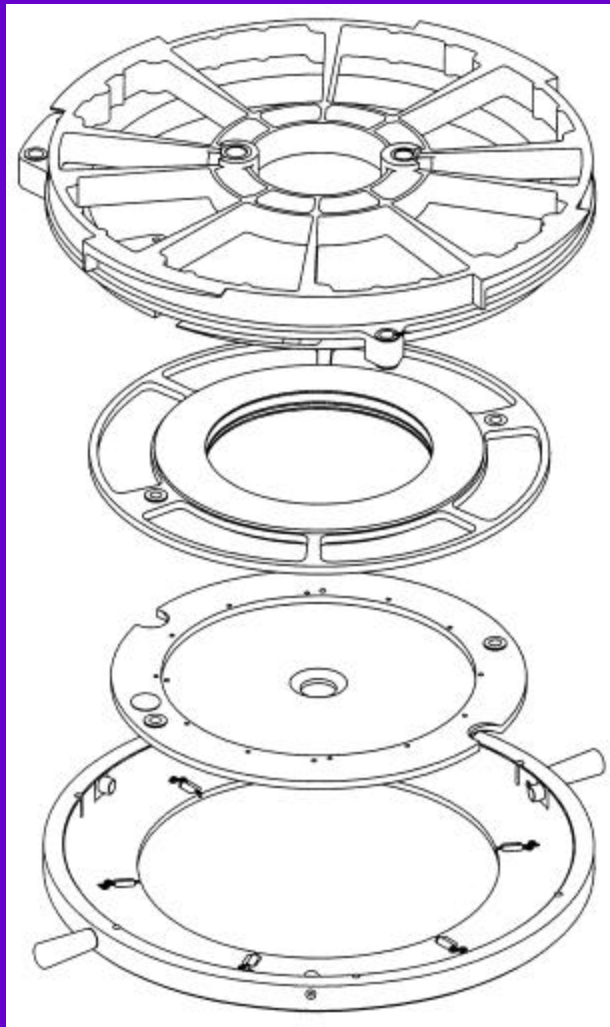
Conventional Dynamic X-direction Vibration



Direct Docking Dynamic X-direction Vibration



Electrical Paths from Test Head to DUT



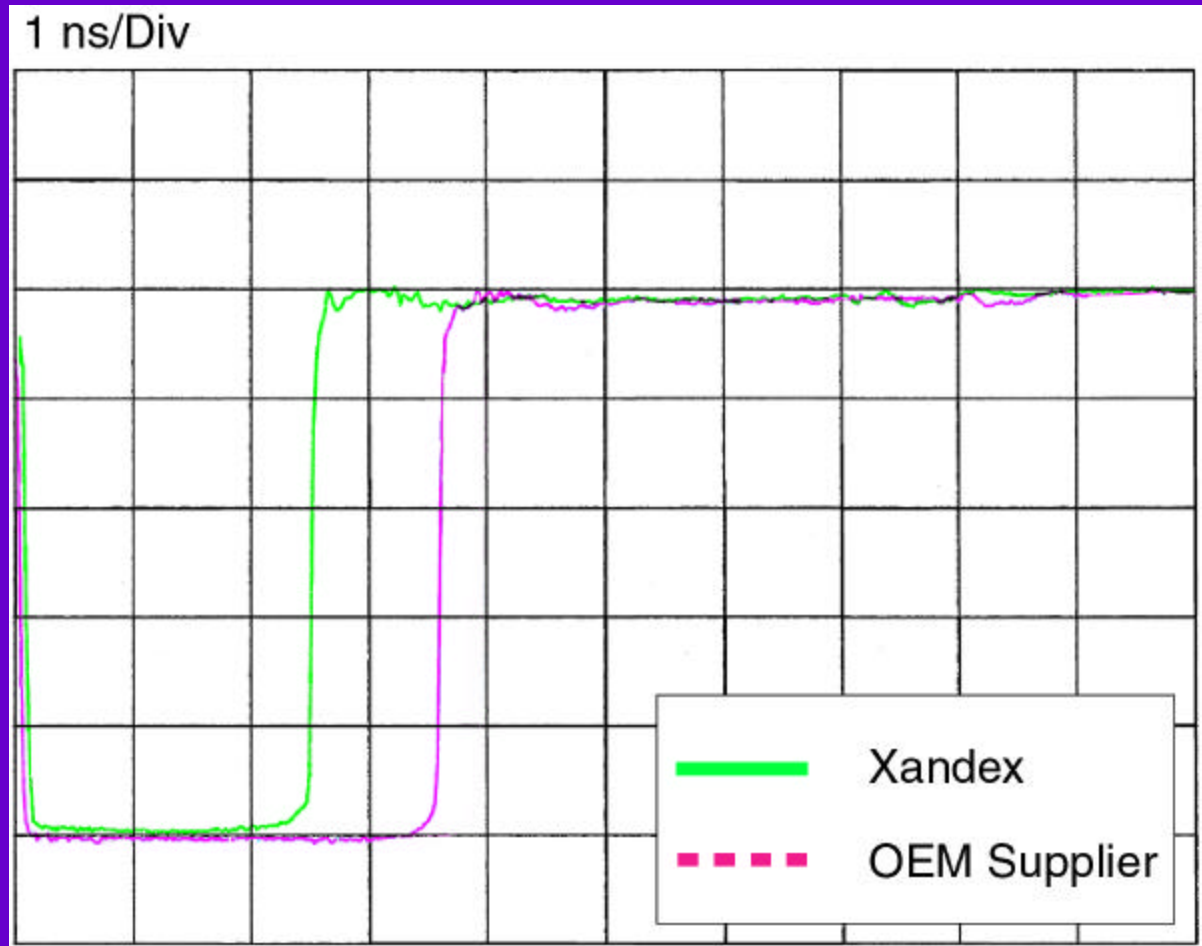
Premise:

Careful balancing of air to dielectric ratio and shortening of physical length in pogo tower will result in improved impedance matching and reduced inductance.

Electrical Paths from Test Head to DUT

Results:

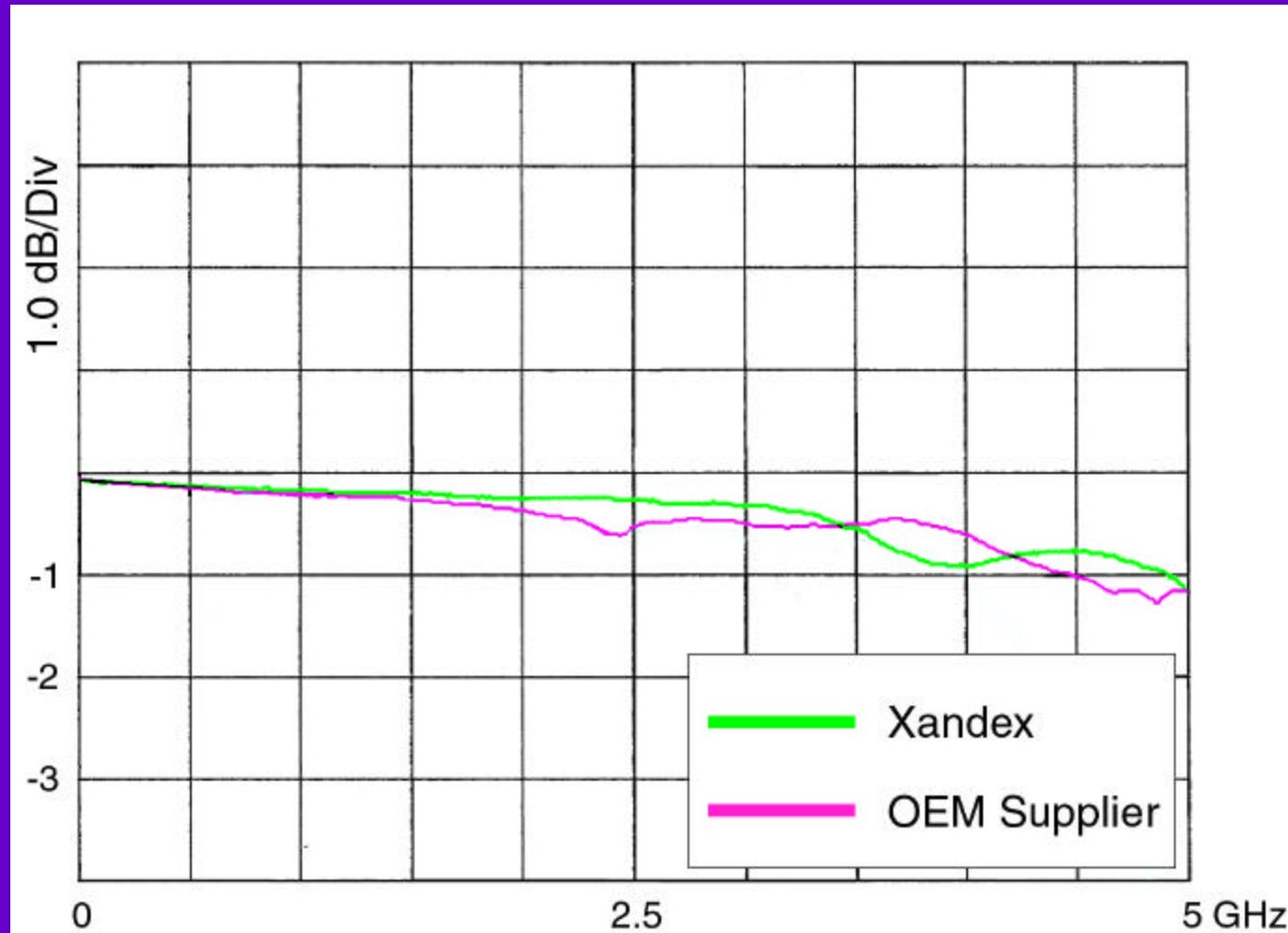
Step
Response



Electrical Paths from Test Head to DUT

Results:

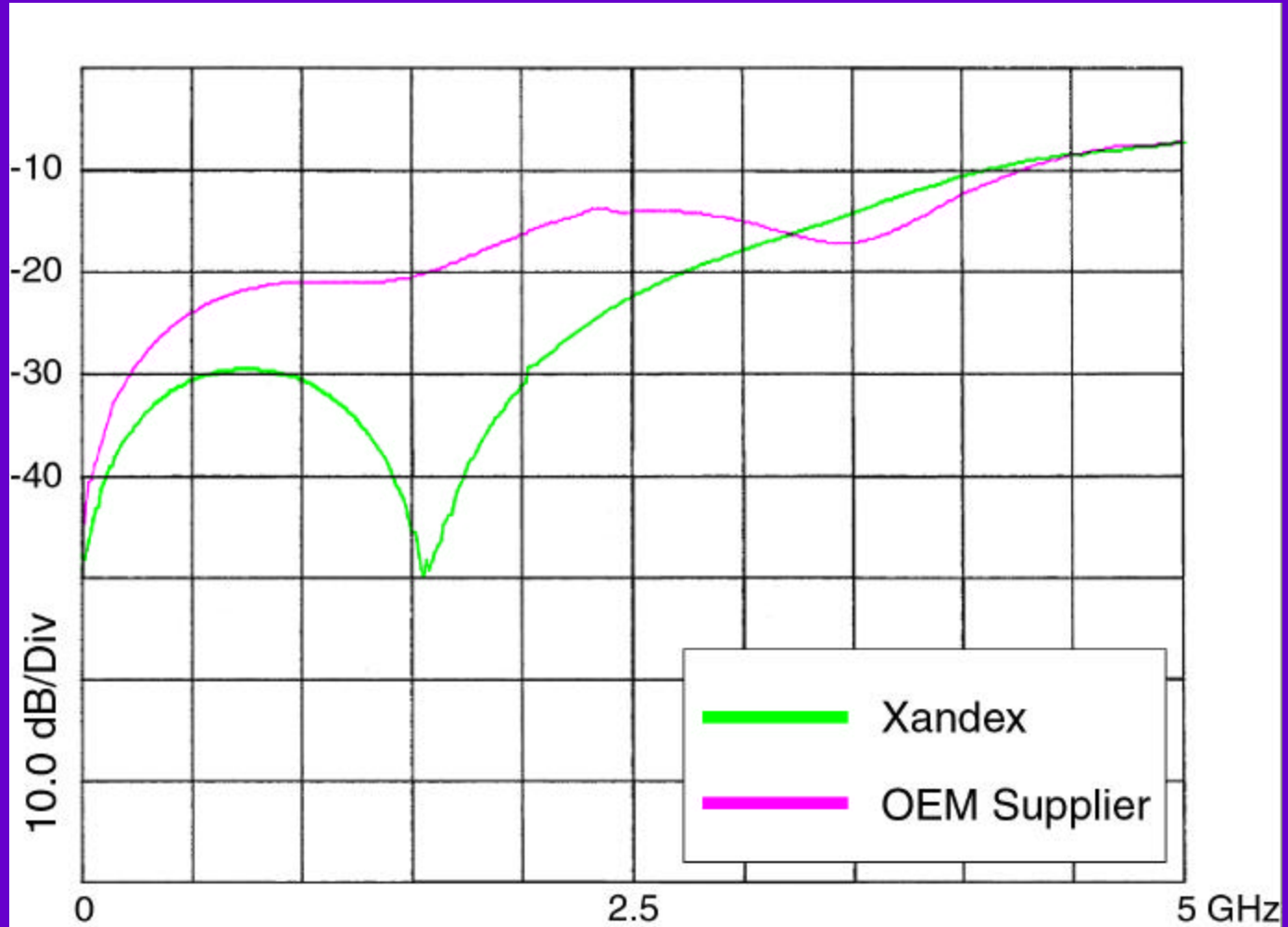
Frequency
Response
(S12)



Electrical Paths from Test Head to DUT

Results:

Return
Loss
(S11)



Compatibility across Tester & Prober Platforms

Premise: For wafer sort floors with multiple tester and/or prober platforms, standardizing interface components can result in ease-of-use, ease-of-training, and manufacturing versatility.

Tester A

- Probe card A
- PIB A
- Interface fixture A

Tester B

- Probe card B
- PIB B
- Interface fixture B

Tester C

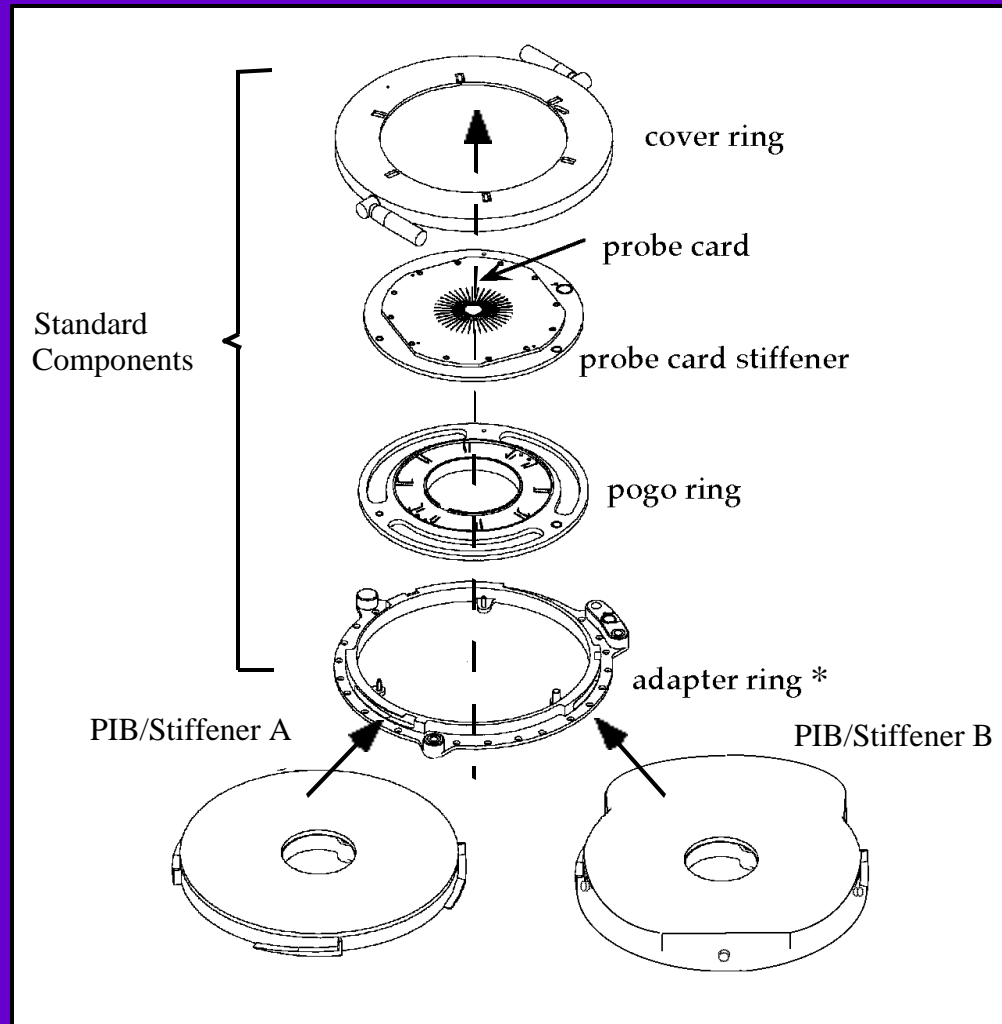
- Probe card C
- PIB C
- Interface fixture C

Tester A,B,C

- Standard Probe Card
- PIB remains tester specific (A,B,C)
- Standard Interface Assembly Components

Compatibility across Tester & Prober Platforms

Results:



* adapter ring requires unique bolt hole patterns for attachment to PIB stiffener

Conclusions

- **Set-up time:** Speedy PIB and/or PC changing will lead to increased throughput.
- **Interface Wear:** Reduction in interface-related maintenance issues results in less tester downtime and increased throughput.
- **Board Deflection:** Elimination of probe card deflection improves reliability of probe-pad contact and eliminates z-contact set up problems resulting in increased throughput.

Conclusions

- **Vibration:** Cleaner static signal will allow for isolation/dampening which in turn will lead to improved contact technology development. Reduced displacement during indexing may allow for less chuck settling time and increased throughput.
- **Electrical path:** Improved electrical signal response might improve yield, should improve lot-to-lot standard deviation.
- **Interface Compatibility:** Manufacturing versatility and ease-of-use resulting from hardware standardization can improve throughput.