Overview of WLBI system approaches

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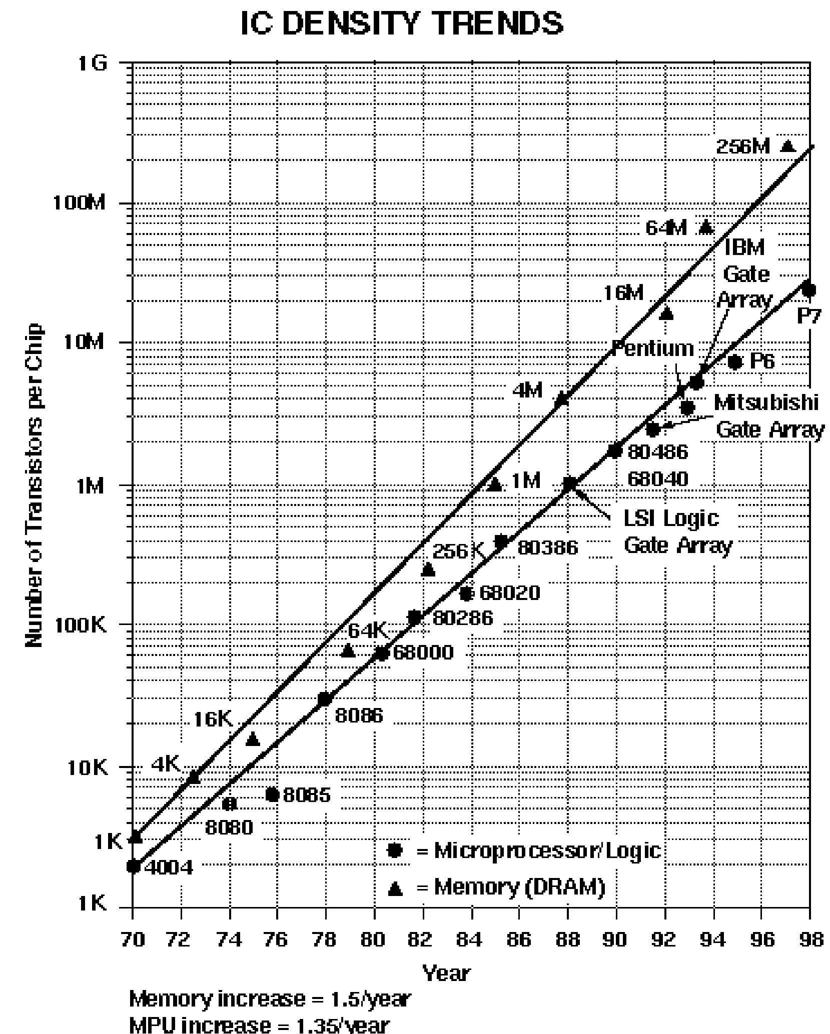
Trends in the Electronics Industry

- **IC Technology**
  - —Higher pin count
  - —Higher power
  - —Higher speed
- **Major Drivers**
  - —Cost/Performance
  - —Quality
  - —Time-to-Market
  - —Product Miniaturization, i.e. lighter, thinner, shorter, and smaller

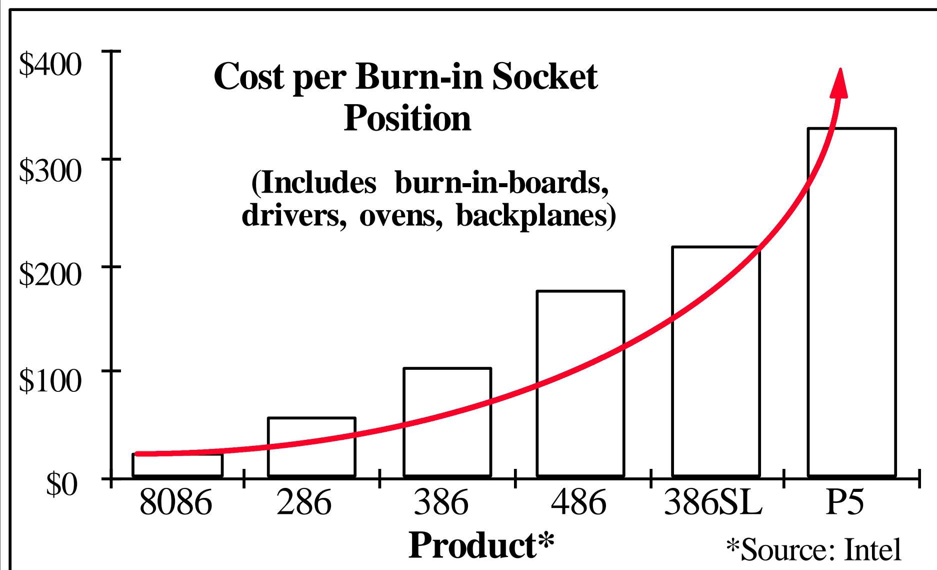


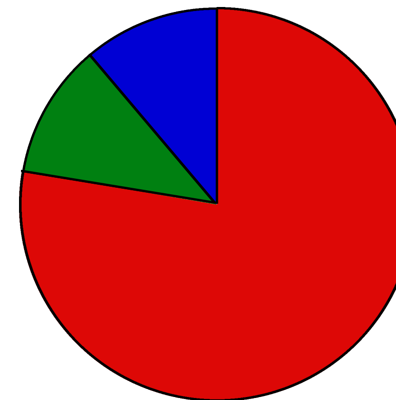
IC quality & reliability

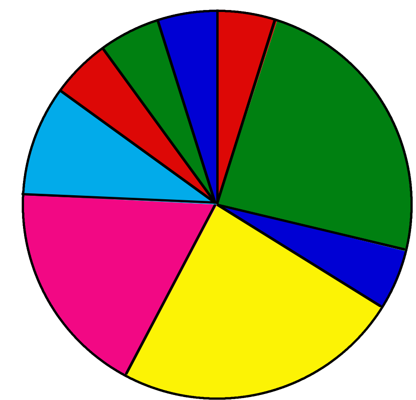
- **Test**
  - —Finds manufacturing defects that cause failure
  - —Not feasible to search for all potential defects
  - —One second on VLSI tester - 2¢ to 15¢
    - » Exhaustive testing all combinations not economically feasible
- **Burn-in**
  - —Stress causes weak devices to fail
  - —Temperature stress
  - —Voltage stress
- **Test during burn-in**
  - —Long cycle functional testing is time-consuming
    - » Trend to offload to lower cost TDBI systems

Burn-in Cost Trend is Not Sustainable

- **Burn-in is a requirement for latest generations of VLSI devices**
  - —**New failure modes emerging due to shrinking geometries**
  - —**Researchers have failed to find an effective alternative**
- **Show stopper for many applications dependent on advanced packaging (i.e., KGD)**







Particles
Oxide Film Defects
Mask Defects
Corrosion
Ion Contamination
Crystaline Defects
Al Voids
Misaligned Vias
Short Circuiting

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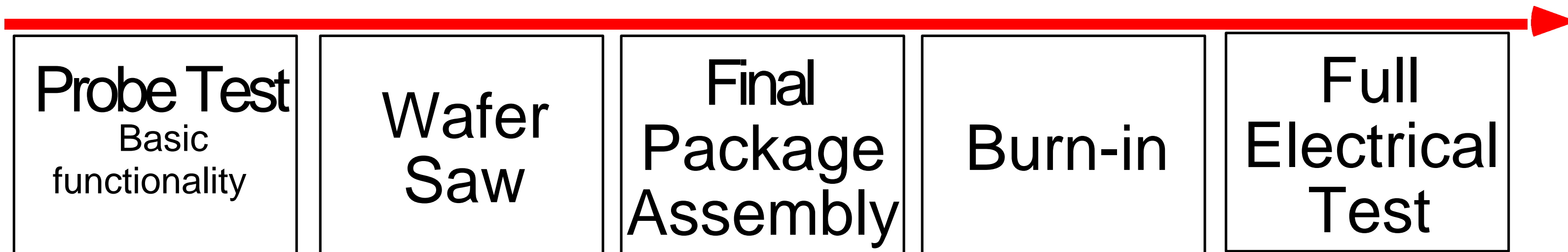
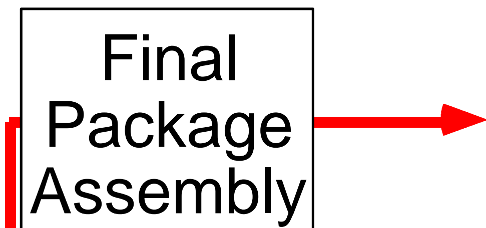
Wafer Level Probing Lowers Burn-in Cost

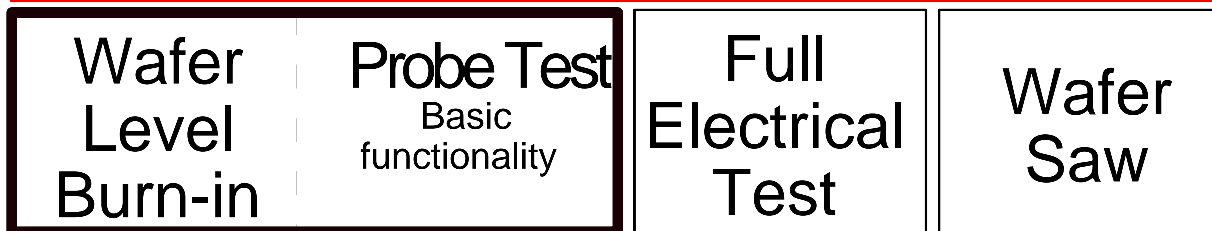
- **MCC cost models predict 50% cost savings for wafer level burn-in wrt current practice**
  - **Other savings also significant**
    - **Reduced IC fab/assembly/test cycle time, lower WIP**
    - **Improved reliability feedback and control**
    - **Enables new paradigm for assembly & test**
- **Full wafer probing for IC burn-in/test is achievable now**
- **Key components of Wafer Level Burn-in/Test (WLBT) system now coming into focus**

IC "Back-end" Processes



Package level burn-in today





Bare Die Market

Full testing and reliability conditioning takes place at the wafer level - new equipment, processes, strategy. Supports bare die as well as existing packaged IC markets.

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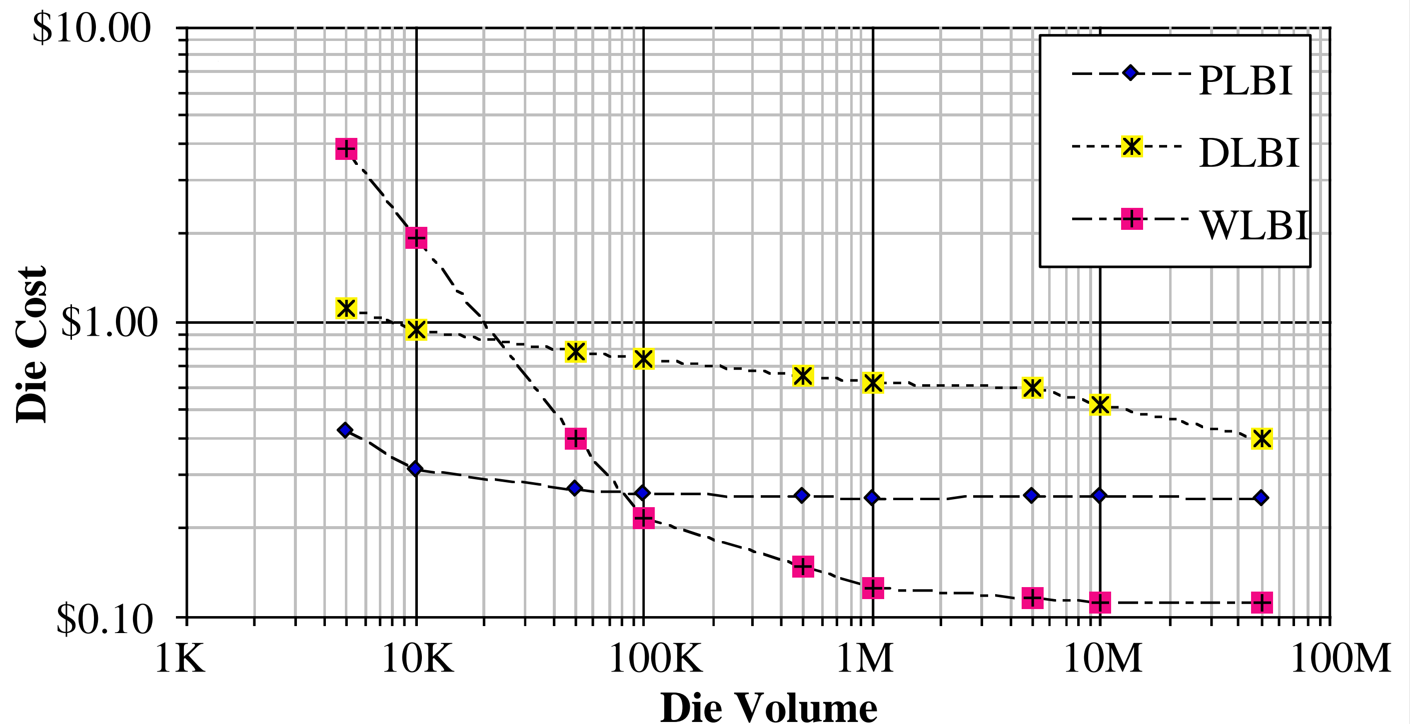
WLBT Cost Comparison

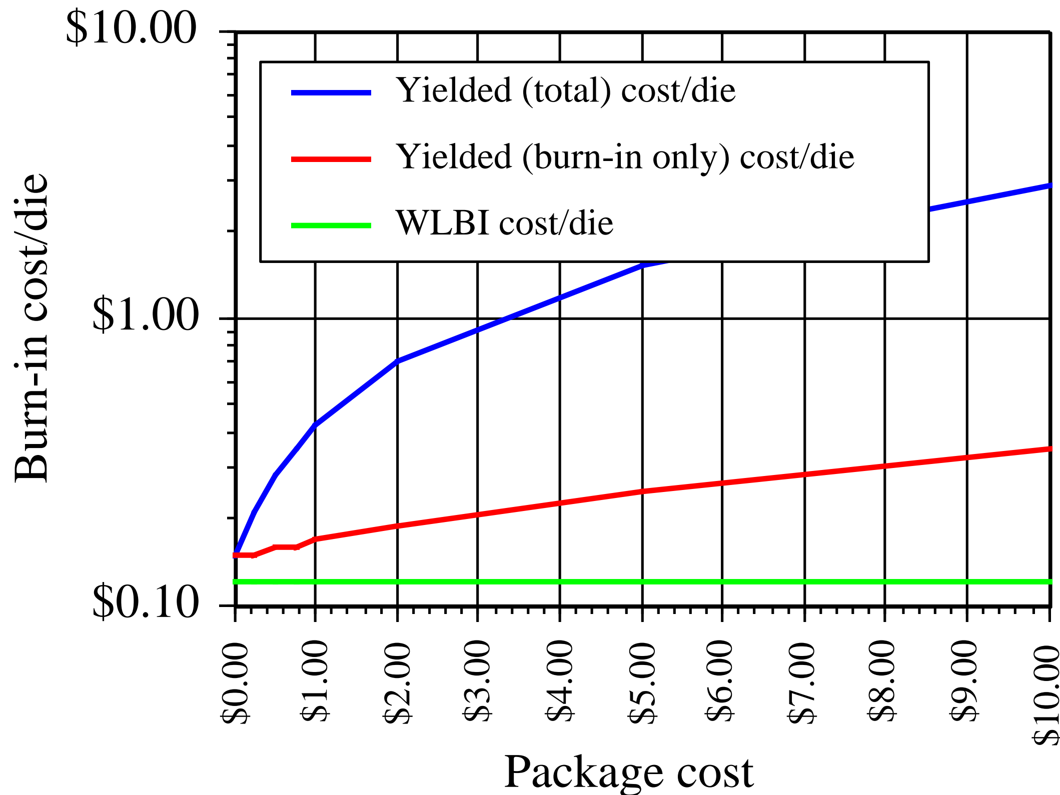
- Fixed quantity of product each year
- 1 Meg FSRAM product
- Have sufficient capacity to keep product moving

<u>Assumptions</u>

- 1.5 year product life
- 15 hour burn-in (+ 4 additional hours ramp up/down, etc)
- $10K/WLBT probe + $10K/probe fixture



WLBI Cost Saving



- **Graph shows cost of scrapping packages**
- **Assumes 80% final test yield, 2% burn-in fallout**

IC Product	Final Test Yield
8-Bit MPU	95%
20,000 Gate Array	90%
4M DRAM	95%
16M DRAM	90%
64M DRAM	75%
4K GaAs SRAM	80%
32-Bit MPU (386)	90%
32-Bit MPU (P54C)	75%

- **Typical Final Test Yields**

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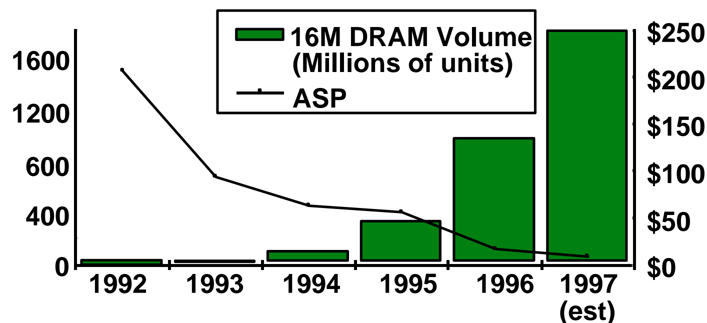
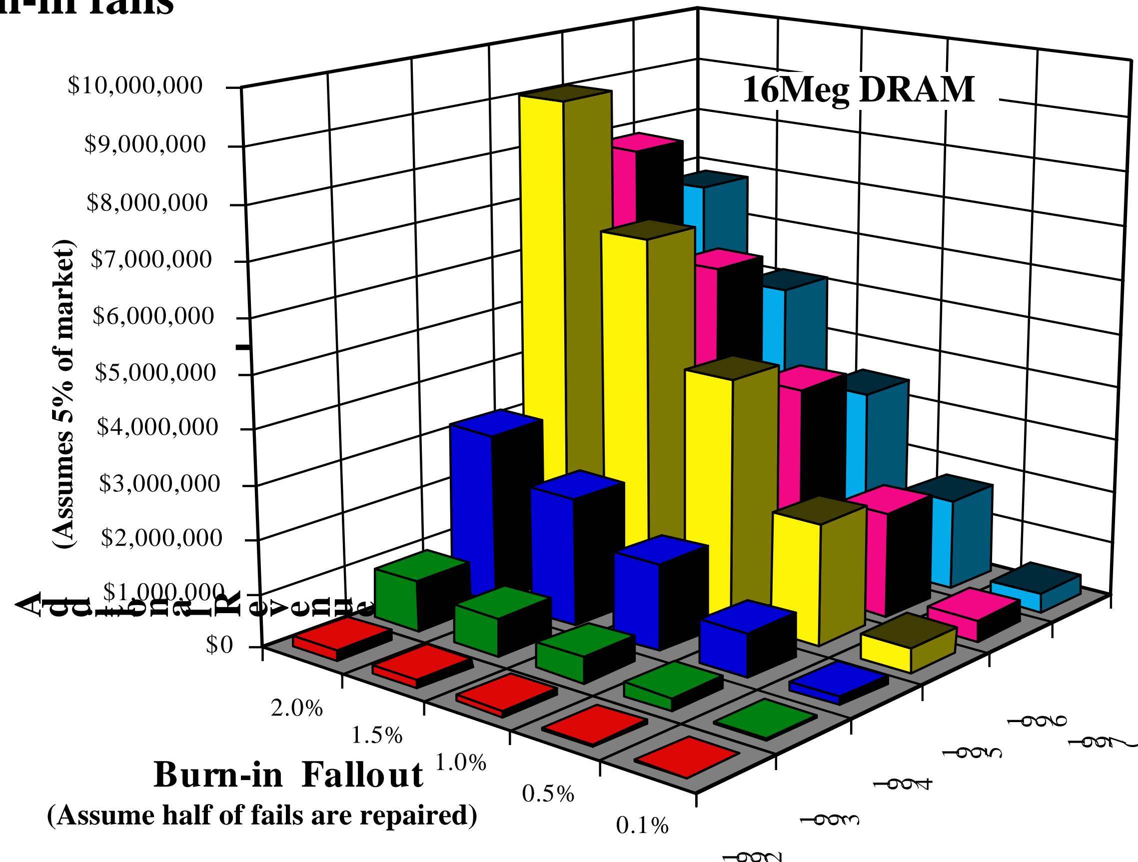
WLBT Value Added

- Laser repair of burn-in fails is feasible after wafer level burn-in, but not available after pkg burn-in
- Assumptions
  - 50% repairability of burn-in fails
  - Distribute ASP of repaired die over population produced that year





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Additional WLBT Benefits

- Fully Automatable
  - —Reduce load/unload time
  - —WLBT fits into highly automated IC assembly processes
    - » Potential for inventory reduction
    - » Cycle time improvements
- Keep from packaging (or shipping) weak devices
  - —Yield loss at WLBT recoverable by laser repair
  - —Early identification of "rogue" lots
  - —Enabler for "single insertion" test/screening
    - » All die fully conditioned at wafer level
    - » Solution for KGD (Flip-chip)
- Rapid reliability feedback on wafer/lot basis
  - —Improves time-to-volume
- Eliminate traditional wafer probe step
  - —Massively parallel test during burn-in reduces time spent on expensive VLSI tester

Wafer Burn-in Worldwide

- WBI Technology for Ram's*
  - —Memory Cell DC Stress to screen Bit Failures
  - —Entire RAM Dynamic Stress for remaining failures
- WBI suppliers
  - —Espec
  - —Asia Electronics
- Several captive programs
  - —Some IC manufacturers developing hardware
    - » Cost effective KGD
    - » Reduce cycle time
    - » Improved reliability feedback
    - » Potential for laser repair of DRAM burn-in fails

* Furayama, et al. *Wafer Burn-in (WBI) Technology for RAM's* —IEDM-93

Hypothetical 200mm Wafer Parameters

■ Die:	652
■ Signal Pads:	18,908
■ Power Pads:	2608
■ Total Pads:	21,516
■ Total Power:	650 W

Feasibility Criteria
Target Product

Attribute	Specification
Diameter	200mm
Pad Metallurgy	Aluminum/Sn-Pb
Minimum Passivation Well (Pad) Size	75µ X 75µ
Maximum Passivation Well Depth	8.0 µm
Minimum Pad Pitch	150µ peripheral, 200µ array
Maximum Pad Density	150 pads/cm^2
Maximum z Variation, Pad-to-Pad	1.0µm
Maximum Power Density	5 W/cm^2
Temperature Range	25ÞC - 150ÞC
Maximum Burn-In Time	168 hrs
Clock Frequency	DC - 20 Mhz

Feasibility Criteria
Target Probe Coupon

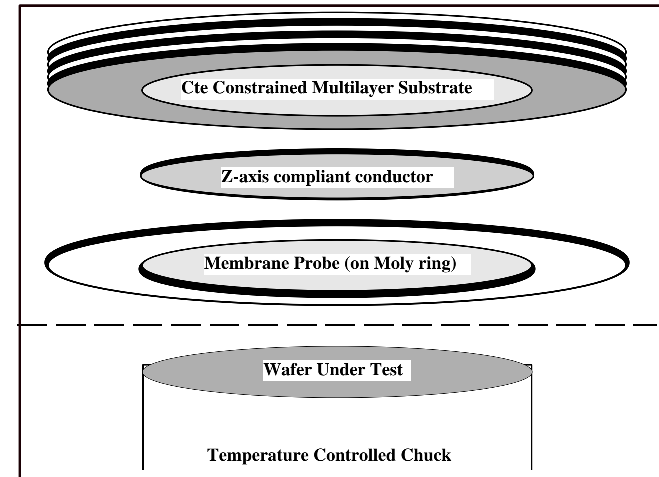
Attribute	Specification
Probe Coupon Diameter	250mm
Dimensional Tolerance	+/-12µm absolute
Maximum Probe Point Size	25µm X 25µm
Maximum Probe Point Current	100mA
Maximum Probe Point Resistance	1.0ž
Minimum Reuses, Same Pad	3
Minimum Lifetime, Reuses	200
Minimum Lifetime, Hours at Temp.	5000
Maximum Isolation Resistor Density	150 resistors/cm^2
Isolation Resistor Values	5kž - 20kž
Max. Isolation Resistor Voltage Drop	7.5V
Max. Unisolated Signal Line Res.	100ž
Max. Voltage Variation, VCC to Grnd	5%
Power Isolation	Must be provided. Max. 3 die/cm^2
Decoupling Capacitors	Must be provided as needed

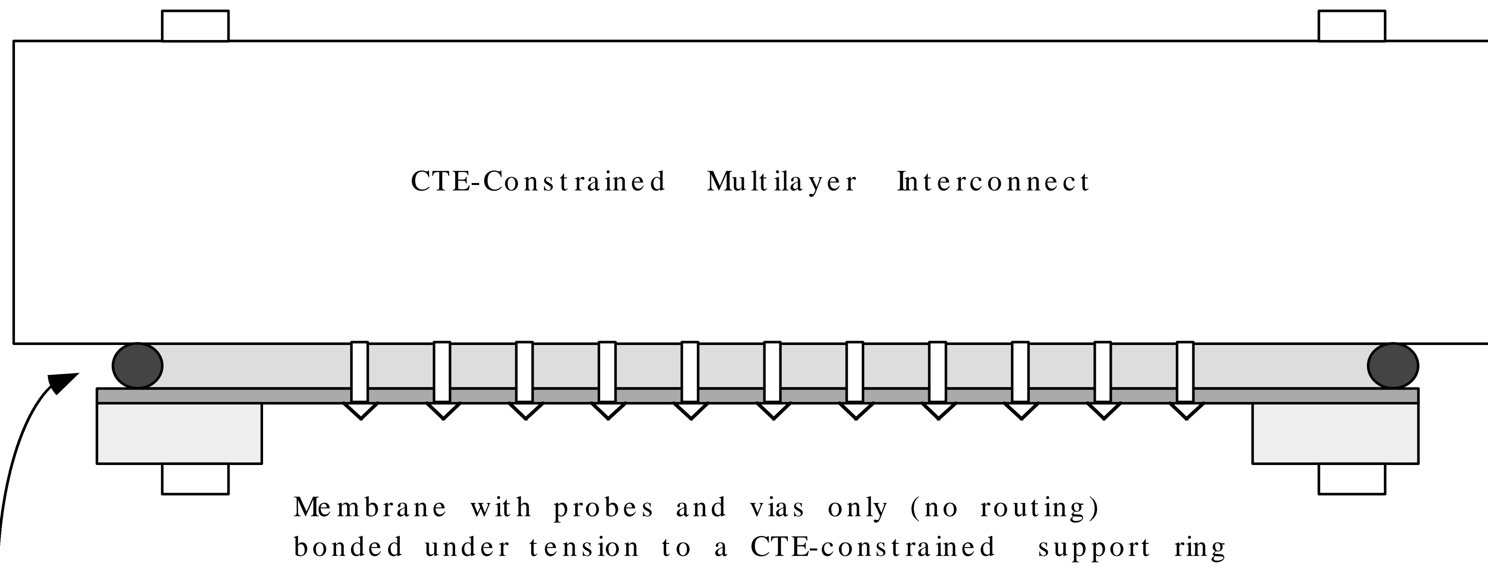
WLBT Challenges

- Probe card
  - —High density interconnect
  - —CTE matching of probe to silicon
  - —Co-planar probe tips
  - —Uniform, “low” resistance contacts to aluminum pads/solder bumps
- Probe card environment
  - —Precise alignment of probe to wafer
  - —Uniform force delivery of probes to wafer
  - —Mechanically decouple probe card from system
    - » Cte matched components independent of non-Cte matched components
  - —Thermal management of junction temperatures
    - » All die subjected to uniform stress
      - V, T, ramp

Three-Layer Probe Isolates Challenges

- Can optimize each piece
  - —Multiple layers for high density routing
  - —Compliant material to "soak up" non-planarities
  - —Robust probe points for probing Al pads





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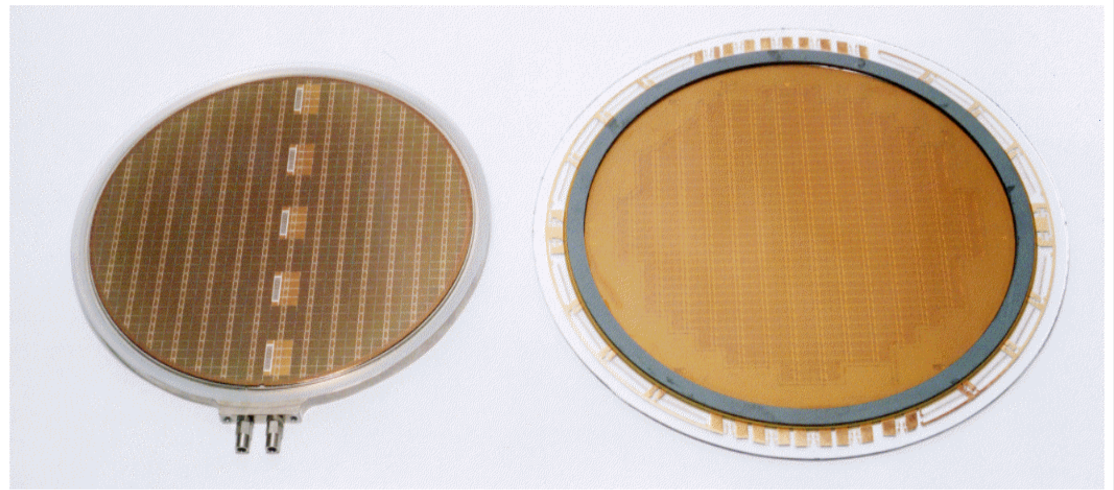
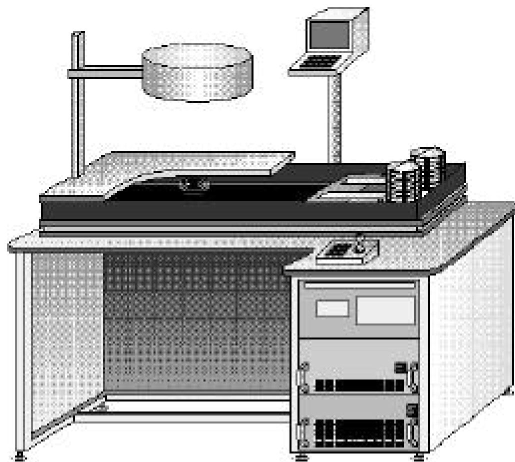
Existence Theorm

- Matsushita Electric Industrial Co. Ltd has developed a 3 layer probe card
  - —Membrane-type probe points
  - —Compliant z-axis conductor
  - —Glass substrate multilayer
- Probe card components Cte-matched to Silicon
- Uses atmospheric pressure for contact force

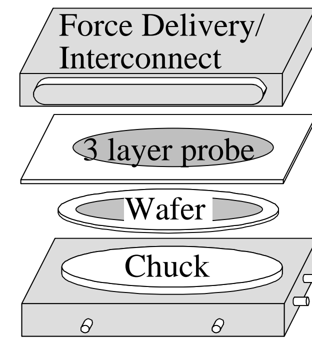


WLBT System

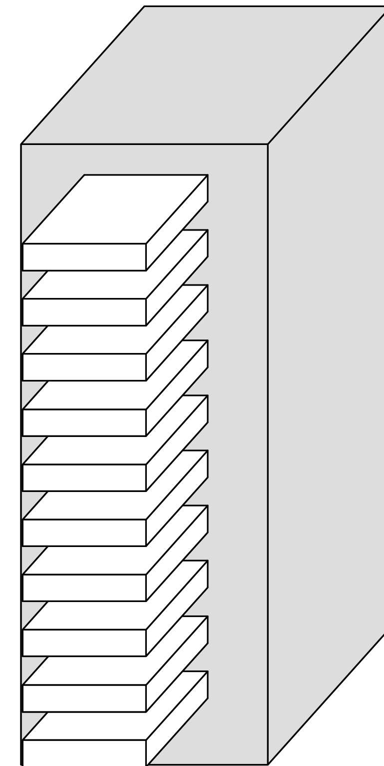
- Wafer cassette incorporating probe card
- Cassette Loader/Unloader based on auto-prober
- Standard wafer-handling equipment
- System development focuses on interface specifications



WLBT Alignment System



Wafer Cassette



Wafer Level Burn-in System

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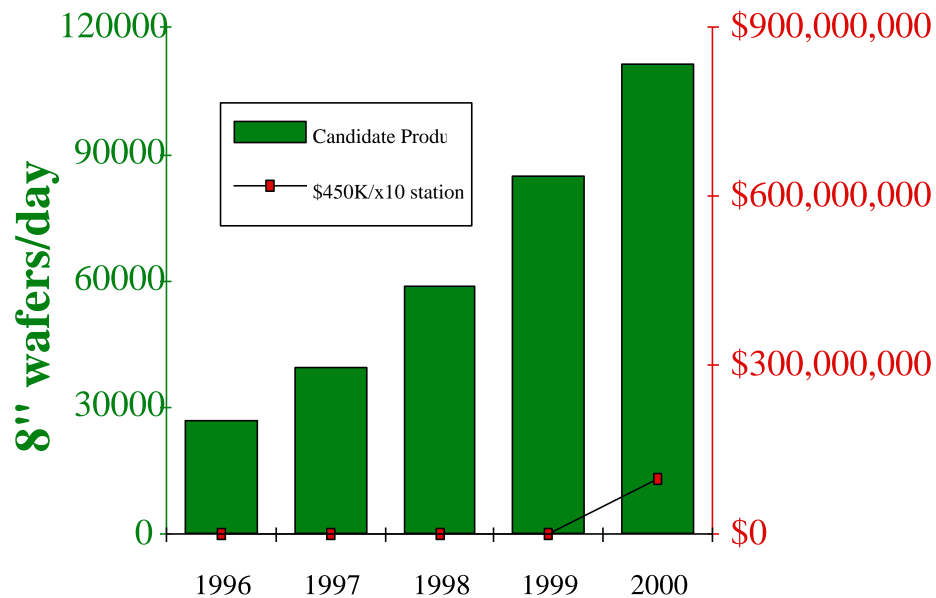
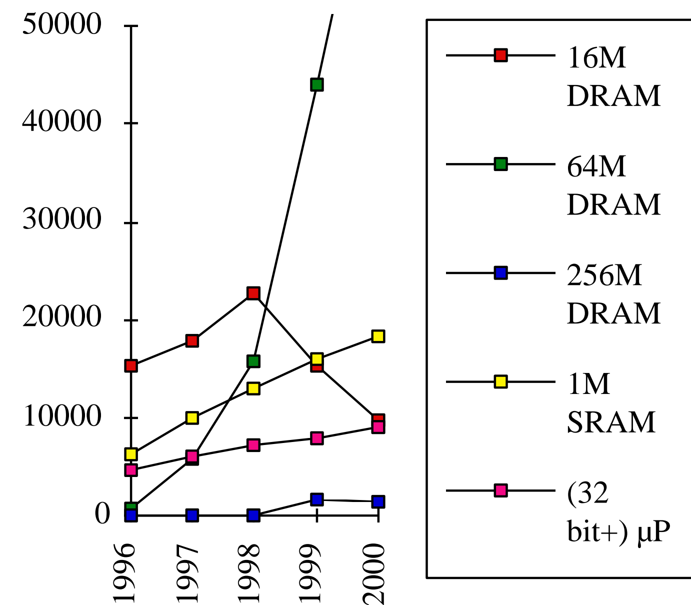
Potential WLBI System market

8" wafers/day	1996	1997	1998	1999	2000
16M DRAM	15353	17890	22696	15293	9753
64M DRAM	674	5721	15825	44033	72849
256M DRAM	0	0	0	1715	1353
1M SRAM	6279	10022	13063	16082	18400
(32 bit+) µP	4789	6082	7173	7940	9058
Candidate Product (wafers	27096	39715	58756	85063	111414
New capacity this year		12619	19041	26307	26351
% WLBI	0%	0%	0.001%	0.050%	2.000%
$450K/x10 station	$0	$0	$26,440	$1,887,478	$98,358,411





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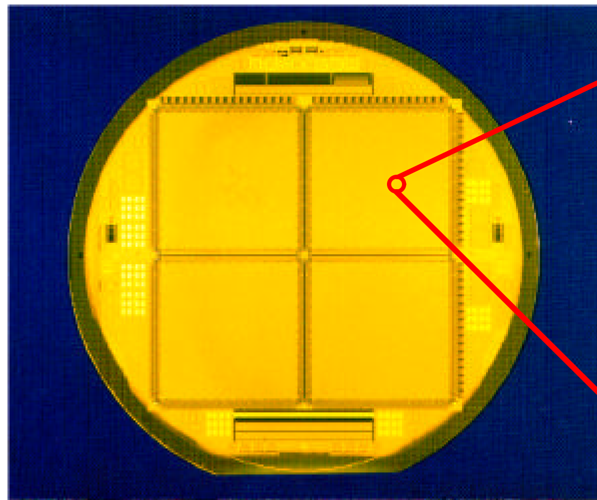
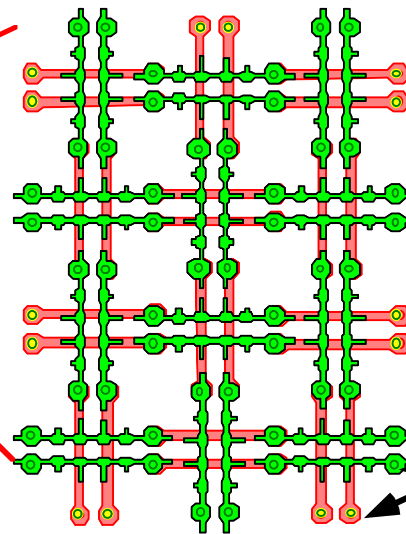
WLBT System Wish List

- Probe Card
  - —<$10K
  - —-500 - 5000 uses
  - —100% yield
  - —Quick Turn
  - —“good” electrical environment
- Cassettes
  - —Controlled environment
  - —One design fits particular wafer size (150mm, 200mm, 300mm, . . .)
- Utilize existing equipment for off-line alignment station and test electronics
  - —Greatly improved equipment utilization

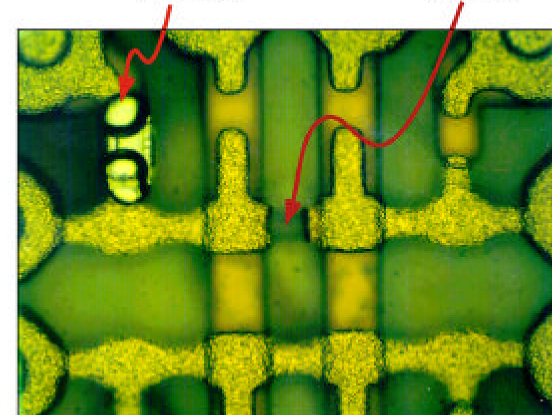
Quick Turn Multilayer Interconnect Using LDW



4.0 inch



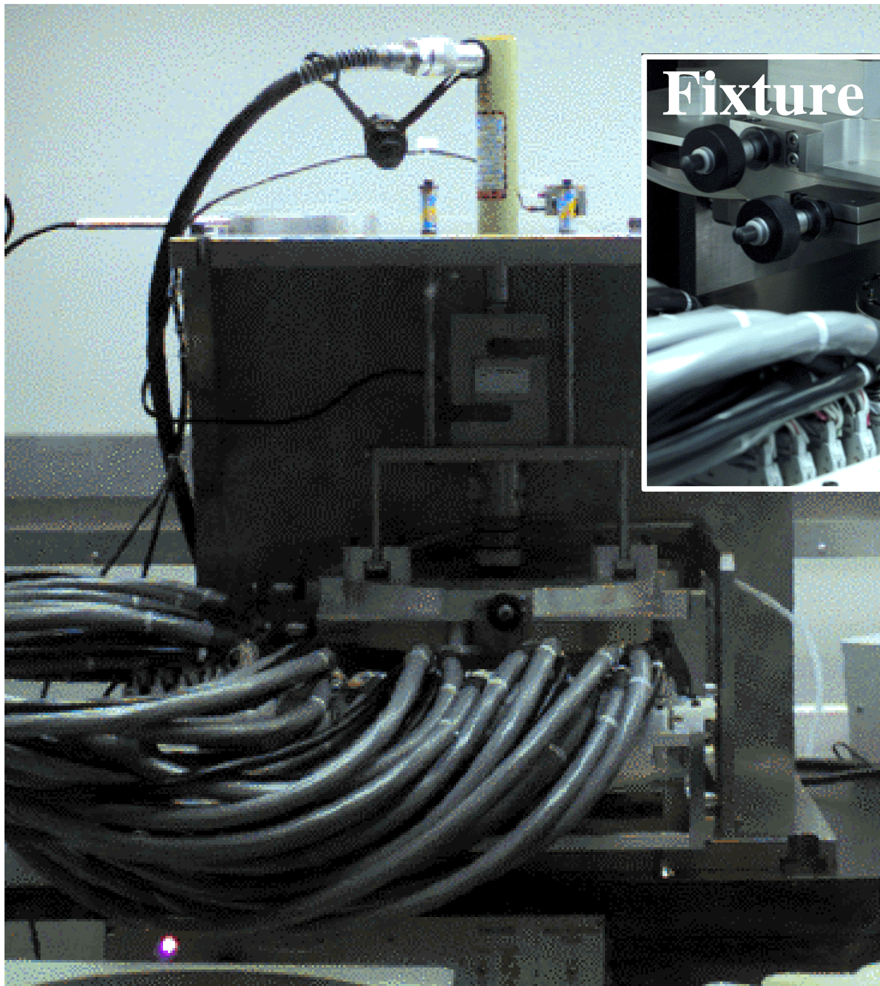
•Four layer design
•Bottom two layers (not shown above) contain a mesh of four programmable reference planes

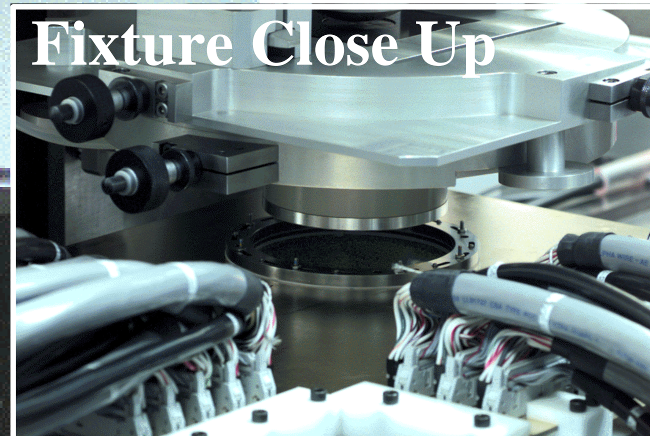


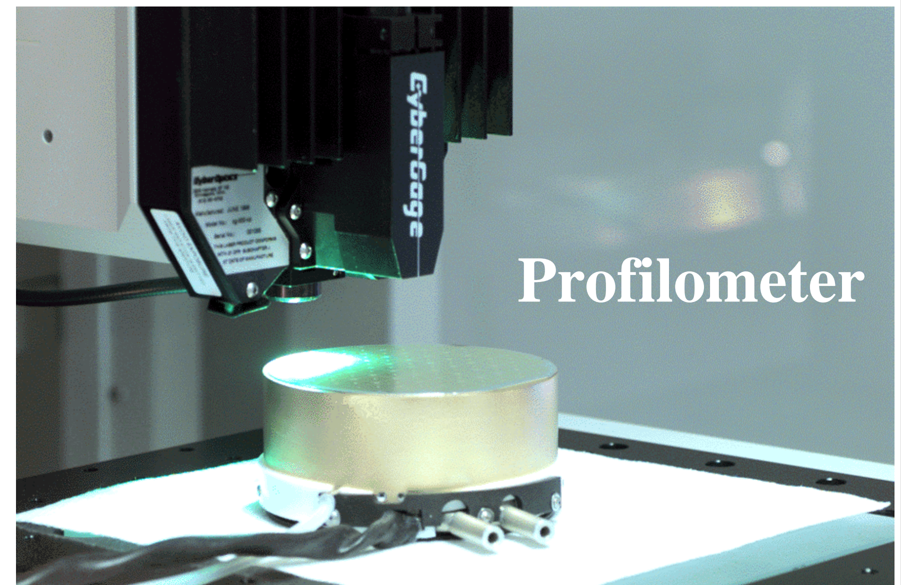
- Quick turn of new probe design
- Route around defects
- Lower cost - standardized substrate

WLTB Probe Laboratory

- Test Electronics
  - Up to 2000 pins
  - Total Current source up to 330A @ 8.0V
- Mechanical Fixture
  - Wafer Size - Up to 8”
  - Force - 4 - 6000 lbs, 2 lb resolution
  - Alignment - +/-0.5 mils
  - Planarization - Self-Planarizing
  - Chuck - Vacuum chuck with active cooling




Fixture Close Up



Profilometer

- Mechanical Fixture