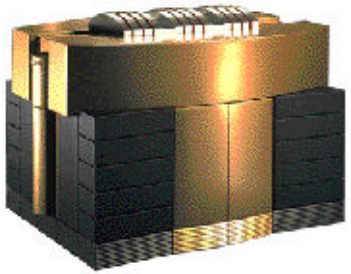

“Scotty, I need more power!”

Dale Slaby

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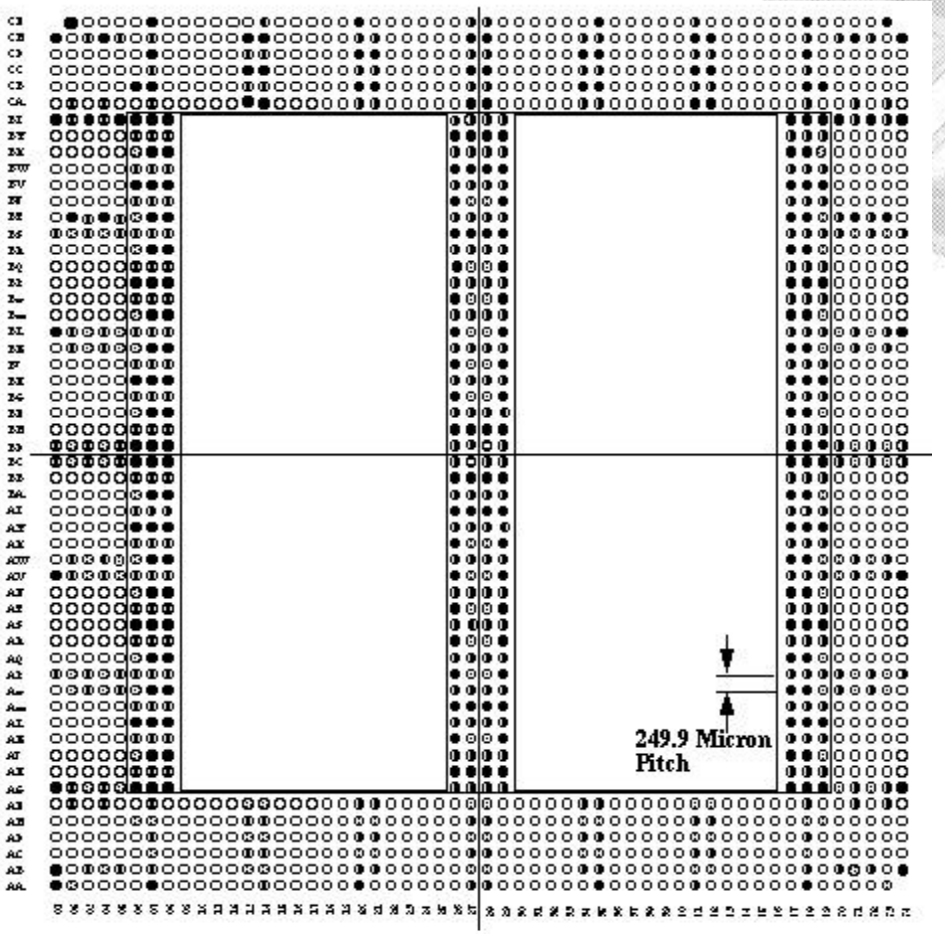
Background

- *13.78 x 13.78 mm sq. die size*
- *1485 total power/ground and I/O*
- *699 power/ground*
- *46 wafer-level test I/O*
- *BiCMOS technology*
- *Dual-rail supply (-2.7 V / -3.3 V)*
- *Initial power estimate at 70 W nominal*
- *Solder ball implementation*

Die I/O Pattern



View of Circuit Side
(Solder Bump Side) of Die.
(Balls Up)

○	784 Signal IO
●	229 Vee1
◐	346 Vcc
⊛	124 Vee4
⊖	2 Clock
	1485 TOTAL I/O

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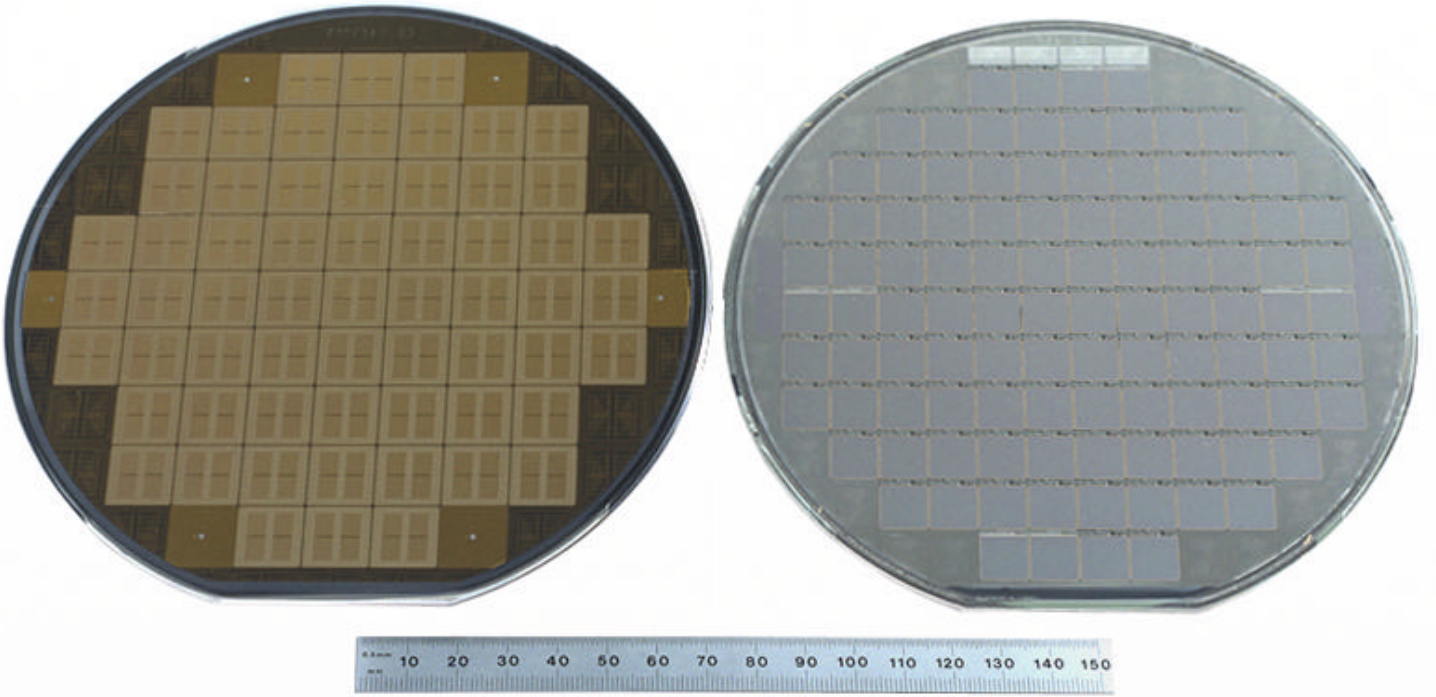
BiCMOS and ECD Wafers

BiCMOS

ECD



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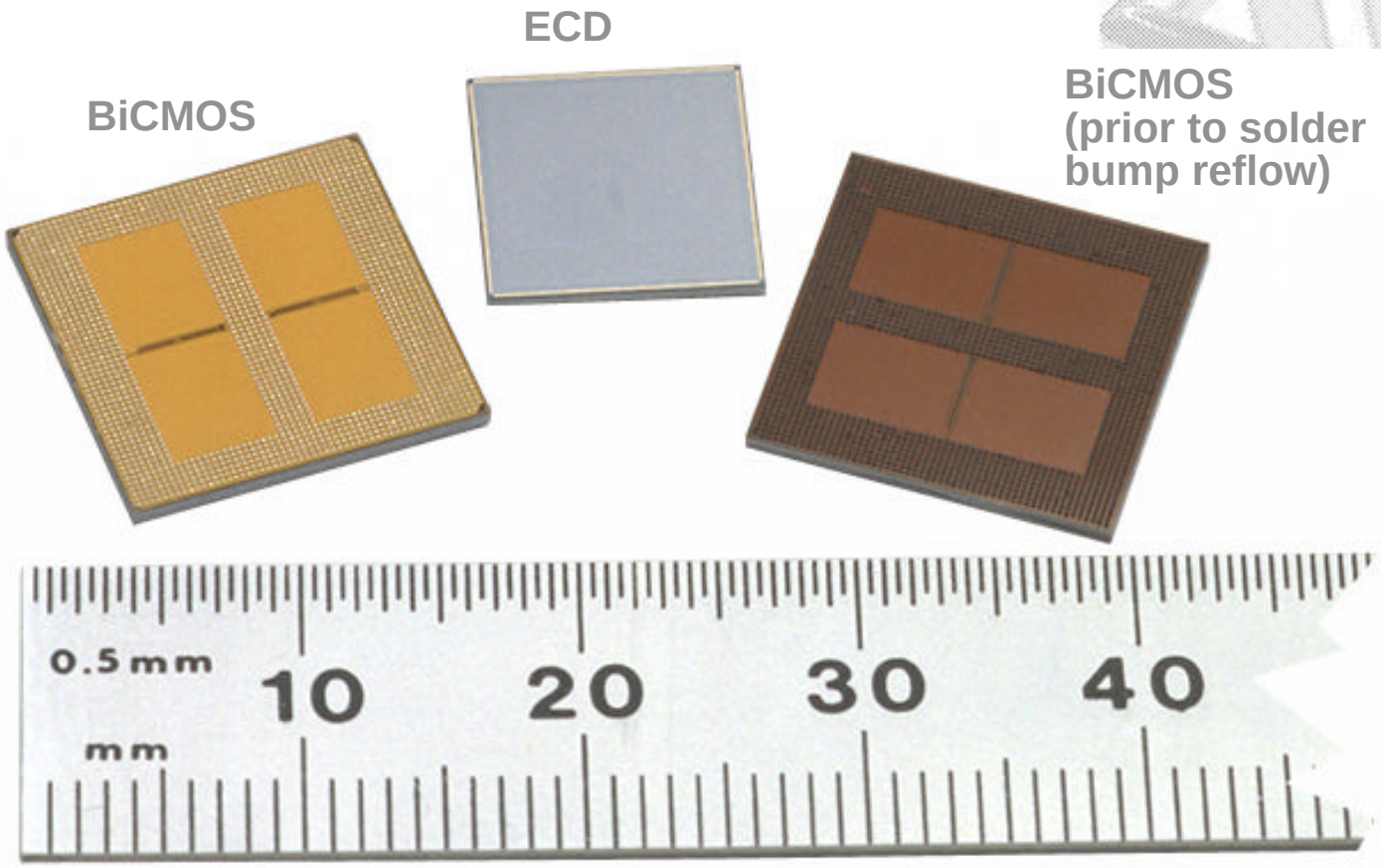
BiCMOS and ECD Die



Decisions...Decisions

- *Wafer probe appeared improbable*
- *Investigated Temporary Chip Attach (TCA)*
- *TCA cost vs. volume advantage*
- *Extra handling and rework*
- *Option to burn-in utilizing TCA*
- *Some risks and infancy of technology*
- *Needed to find an alternative*

Requirements

- *Power up to 100 W nominal; 150 W worse case!*
- *Heat flux density at 2.5 W / mm sq.*
- *Thermal manage core and wafer under full power*
- *Implement DC parametrics, BSCAN and at-speed BIST with reduced pin set*
- *Maintain minimal IR drop across hardware and core*
- *Balanced power distribution*
- *Minimal solder ball deformation*
- *Thermal monitor capability*
- *2 GHz bandwidth for at-speed tests (required membrane core)*
- *Alignment windows through membrane core*
- *Reliable and repeatable touchdowns*

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Hardware

- *Thermal Chuck from Temptronic Corporation*
  - *Co-developed with two technology partners*
  - *Circular grooves for vacuum and helium*
  - *Water cooled with 6” custom chuck plate for SGI/Cray*
- *Electroglas 3001X Probe Station with High Z-force Stage*
  - *Allowed adequate force for high pin count contact force*
- *Cascade Microtech Membrane Core/Probe Card*
  - *Capable of contacting desired solder balls easily*
  - *Offered controlled impedance out to solder ball*
  - *High bandwidth interconnect / metal trace*
  - *Minimal contact area on solder ball reduces deformation/rework*

Close-up of Thermo-chuck

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Cascade Membrane BiCMOS Wafer Test Head

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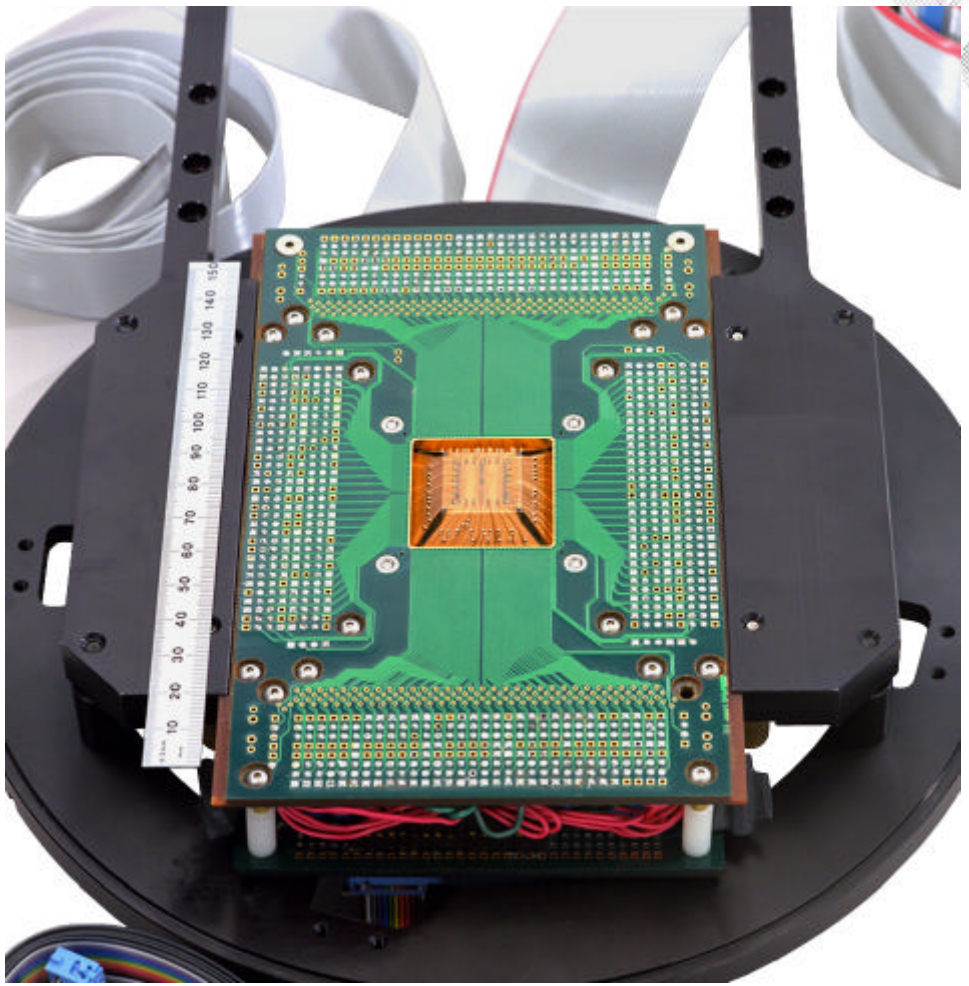
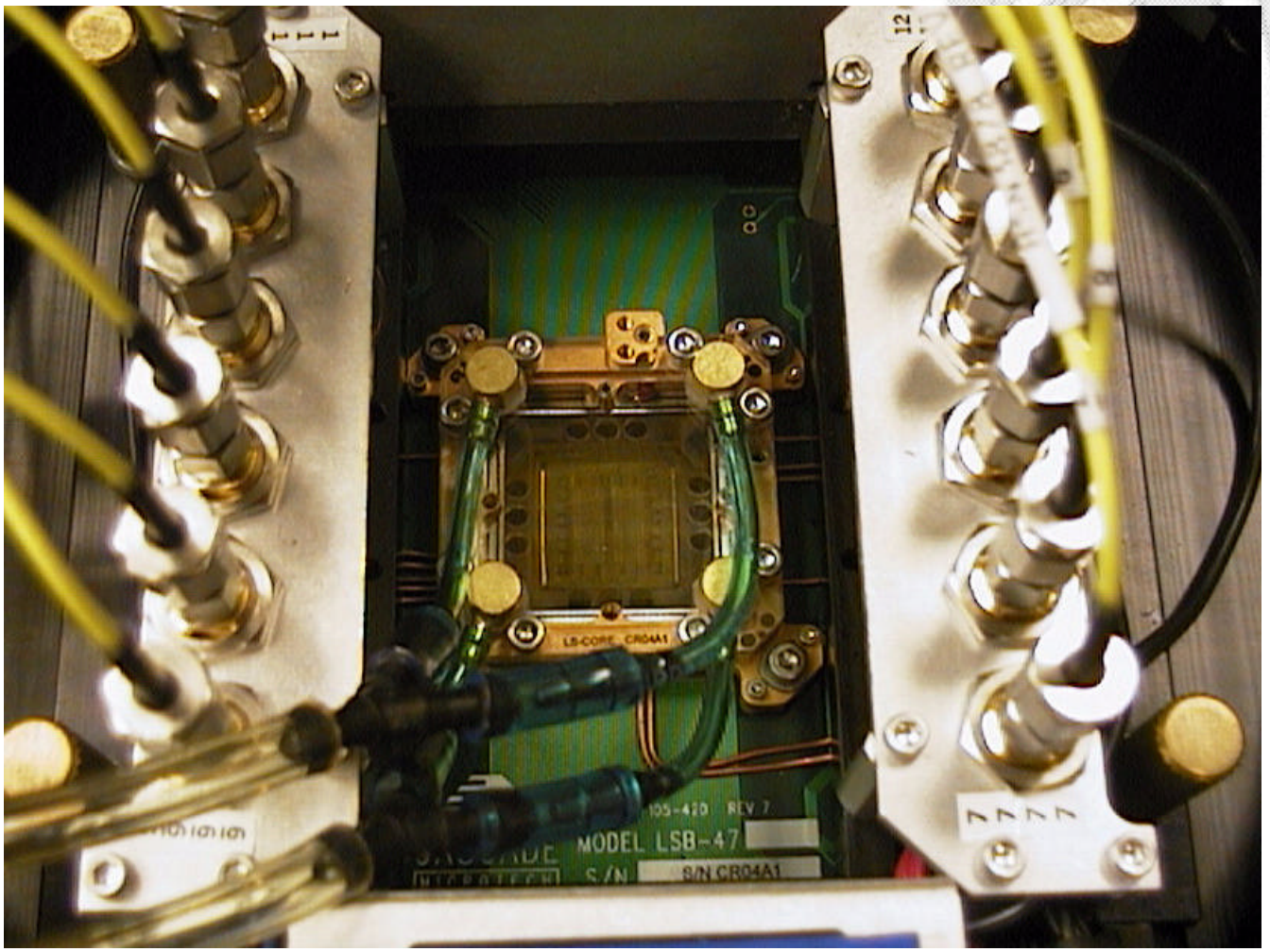
Cascade Membrane BiCMOS Wafer Test Head



Core Layout / Features

- *Dual-power rail distribution with minimal drop*
- *Current capability > 70 amps*
- *R-loop resistor for thermal monitoring on high-current wings*
- *Optimized for memory and CPU ASIC options*
- *25-mm core bumps for excellent electrical contact and minor deformation*
- *Allowed for 5-7 mils overtravel, which reduced planar issues*
- *Creative air manifold to maintain thermal control of membrane core*
- *Ability to mount caps close to bumps for high-frequency noise reduction*
- *View windows for wafer to core-bump alignment*

Top View of Membrane Core



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Membrane Core Test Data

Full Power UP of TMTC 109 W3 w/no He on Chuck@ 20C (2/12/98)

Wafer Tcr @ 1.25 ohms/ Die Location x6,y7

Volts	ee1 Cor	lee1 I/O	Watts	%Chang	RL1	RL3	RL4	TR2	TR3	Tj (C)	Comments
0.40	3.75	1.19	1.98		7.80	6.46	6.52	403.00	399.00	20.00	TR@20C
0.60	5.58	1.79	4.42	0.50	7.83	6.48	6.55	406.00	403.00	23.20	
0.80	7.41	2.37	8.00	0.83	7.85	6.50	6.57	408.00	405.00	24.80	
1.00	9.30	2.96	13.00	1.50	7.89	6.53	6.62	411.00	409.00	28.00	
1.50	13.80	4.40	27.00	4.17	8.05	6.67	6.78	421.00	420.00	36.80	
2.00	18.20	5.85	48.00	7.67	8.26	6.87	7.03	435.00	436.00	49.60	@35psi
2.00	18.20	5.85	48.00	6.67	8.20	6.79	6.94	435.00	436.00	49.60	@50psi
2.20	19.90	6.40	58.00	7.83	8.27	6.85	7.02	441.00	443.00	55.20	
2.40	21.50	6.96	68.00	9.00	8.34	6.93	7.12	448.00	451.00	61.60	
2.60	23.30	7.53	80.00	10.83	8.45	7.01	7.22	455.00	459.00	68.00	@50psi
2.60	23.30	7.53	80.00	10.67	8.44	6.98	7.17	455.00	459.00	68.00	@60psi
2.80	24.70	8.05	92.00	12.17	8.53	7.07	7.28	463.00	468.00	75.20	
2.80	24.70	8.05	92.00	11.50	8.49			463.00	468.00	75.20	@65psi
3.00	26.30	8.59	105.00	12.67	8.56			471.00	478.00	83.20	
3.00	26.30	8.59	105.00	9.50	8.37	6.94	7.13	471.00	478.00	83.20	Dual
3.20	28.10	9.17	119.00	11.33	8.48	7.01	7.22	479.00	488.00	91.20	Manf'd
3.40	29.50	9.71	**133.00**	12.50	8.55	7.08	7.30	488.00	500.00	**100.80**	line @60
3.00	**26.30**	**8.59**	**105.00**	**10.67**	**8.44**					**66.00**	He &
3.60	**31.24**	**10.26**	**149.00**	**16.67**	**8.80**					**97.00**	dedicated
3.80	**33.00**	**10.80**	**166.00**	**18.00**	**8.88**					**113.00**	manifold
4.00	**34.79**	**11.35**	**184.00**	**20.00**	**9.00**					**132.00**	

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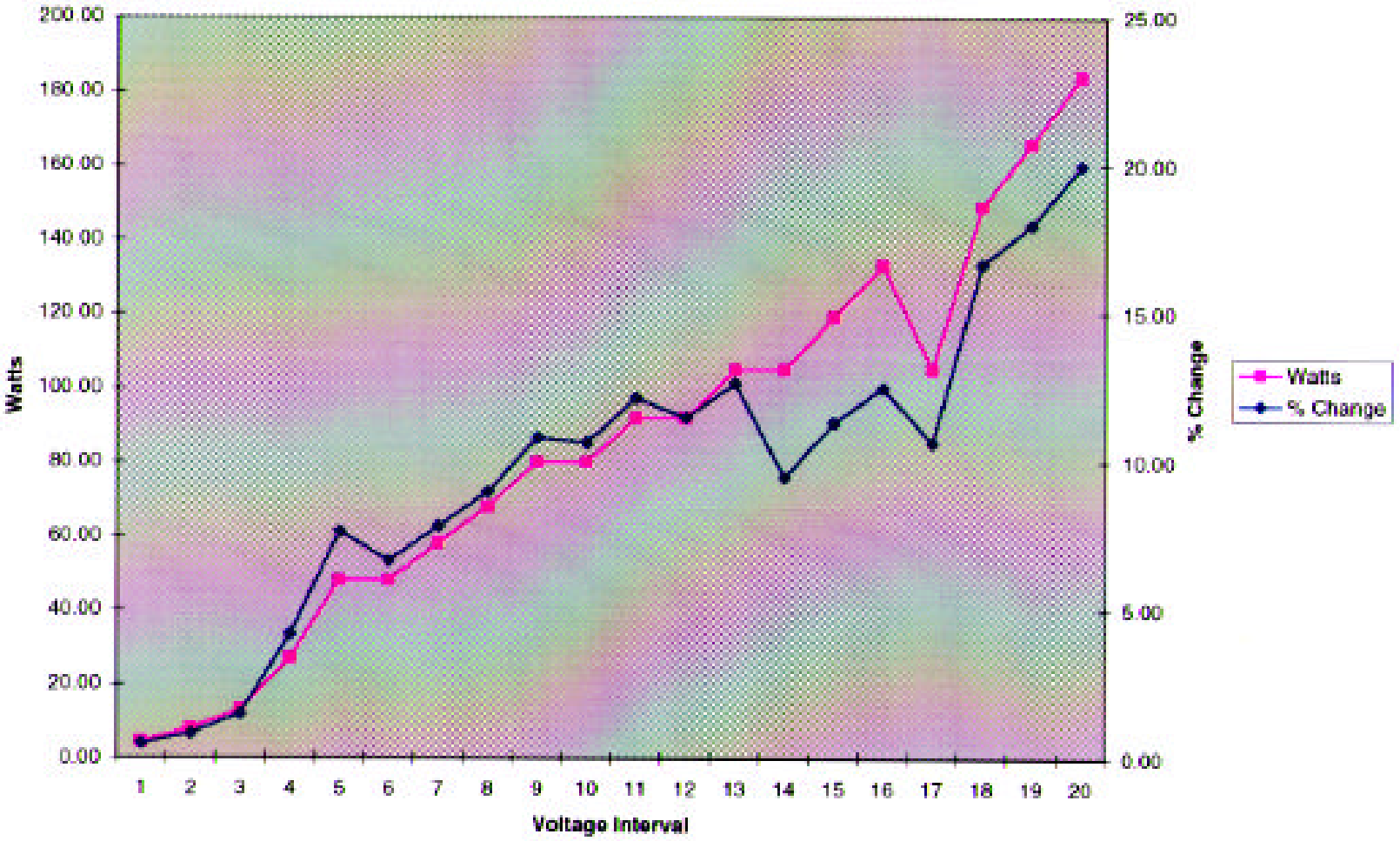
Power vs. R-loop Change



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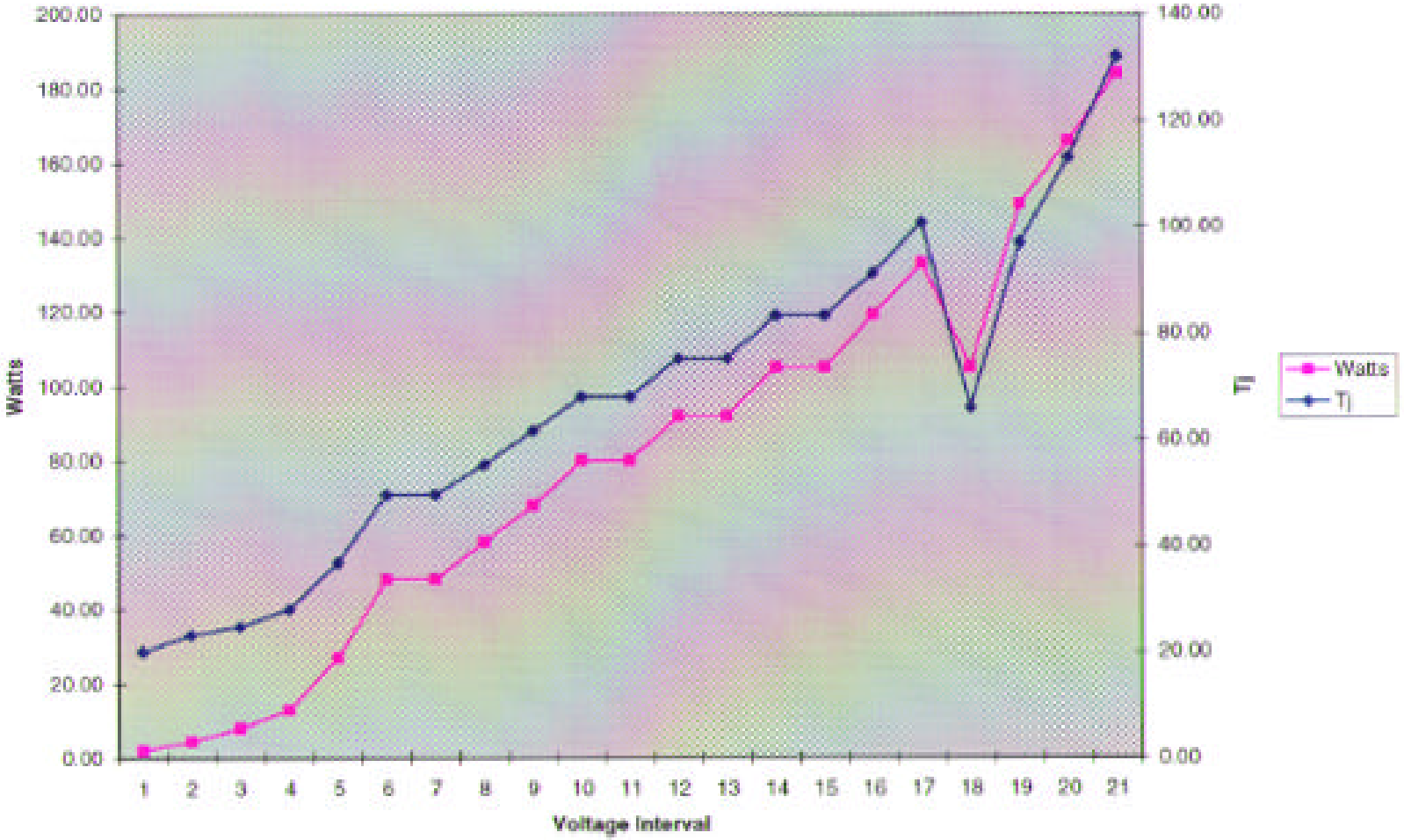
Power vs. Junction Temperature (Tj)



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Conclusion

- *Successful management of die Tj's up to 180 W of device power!*
- *Uniform contact of all solder bumps*
- *Minimal contact resistance after many touchdowns*
- *CTE mismatch managed with adequate membrane and wafer cooling*
- *No smearing or excess stress observed*
- *Membrane layout yielded relative ease in wafer to bump alignment*
- *Thermal chuck design with helium impingement reduced thermal resistance by ≥ 20%*
- *Readiness to thermally manage wafer-test environment for actual options*

Acknowledgments

- *Cascade Microtech – Ken Smith*
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- *SGI/Cray – Mike Higgins, Joe Christensen, Nick Krajewski, Nancy Burgess, Craig Swoboda, Warren Kerola*

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