

IEEE SW Test Workshop Semiconductor Wafer Test Workshop

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Effective Integration of Advanced Probe Card Technologies from Development to Production Test Floors



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- ACKNOWLEDGEMENTS



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INTRODUCTION

- TI and sub-con test floors use a variety of probe card technologies ranging from cantilever to advanced MEMs on wafers with an array of probe test requirements.
- Each new device exhibits increased functionality, which requires increased test capability and a decrease in the cost of test or COO-cost of ownership. *"cheaper, faster, better,"...what else is new?*



PROBLEM STATEMENT

- But, increasingly shorter and complex product cycles also shorten the time to design, develop, characterize and introduce wafer-level probe card technologies into test floors and "Qualify" as "Production Worthy."
- So, how does one go about getting probe card technology quickly into production without incurring significant evaluation costs in as non-intrusive and/or as non-disruptive manner to production?



INTEGRATION APPROACH

Perform a focused integration process that reduces the qualification time, yet increases the success-rate of introducing probe card technologies into test floors. Composed of 2 key steps:

> 1. Technology Qualification- A few wafers and probe cards

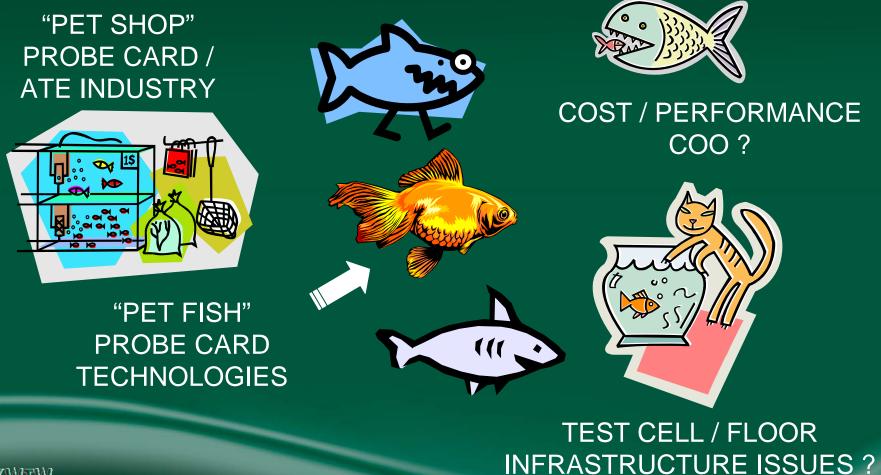
2. Production Qualification- A lot more wafers and more production exposure

"Similar to bringing a pet fish home from the pet store"



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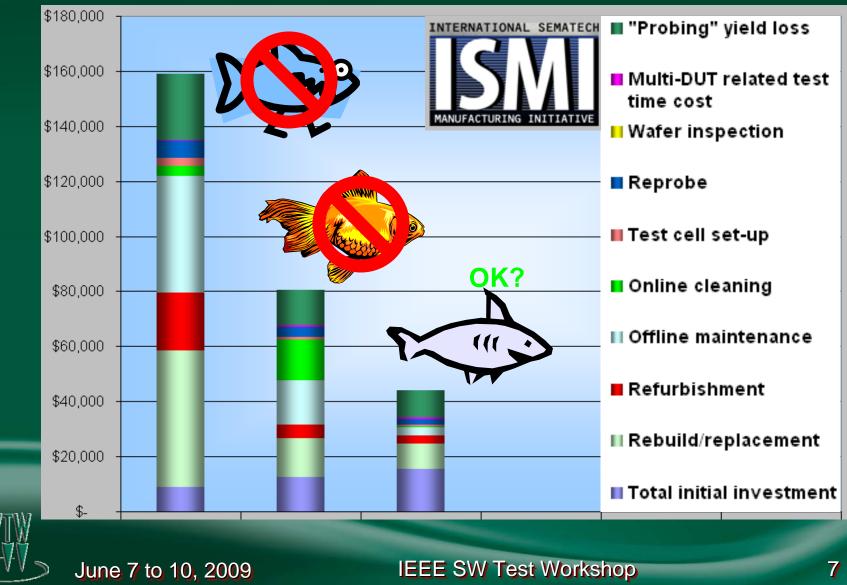
1-PET FISH INTEGRATION Probe Technology "Fish" Qualification



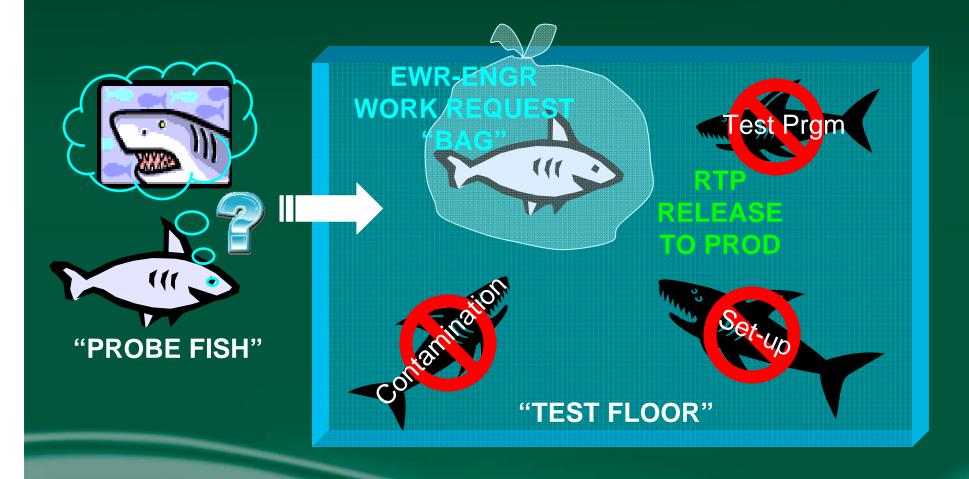


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ISMI Probe COO Model Breakdown of Probe Related Test Costs



2-PET FISH INTEGRATION Production "Aquarium" Qualification





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PROBE CARD INTEGRATION PROCESS: (2 Steps Each with 4 Compliance Levels)

Technology - Production QUALIFICATION	
PASSES Category	Meets required CTF-Critical To Function parameters. Passes qualification category for the particular probe requirements envelope or node intended. e.g. 70 um, x32/x64 multi-site enablement
PASSES Category	Meets most CTF-Critical To Function parameters. Passes qualification step. However, contingent on additional data, data analysis either on-line or off-line to resolve
DOES NOT QUALIFY	Does not meet most CTF-critical to function parameters. Does not pass qualification category. Not considered a show-stopper; however, ARs required to be resolved
DOES NOT QUALIFY	Does not meet required CTF-critical to function parameters. Does not pass qualification category. Considered a show-stopper, significant work required to resolve.





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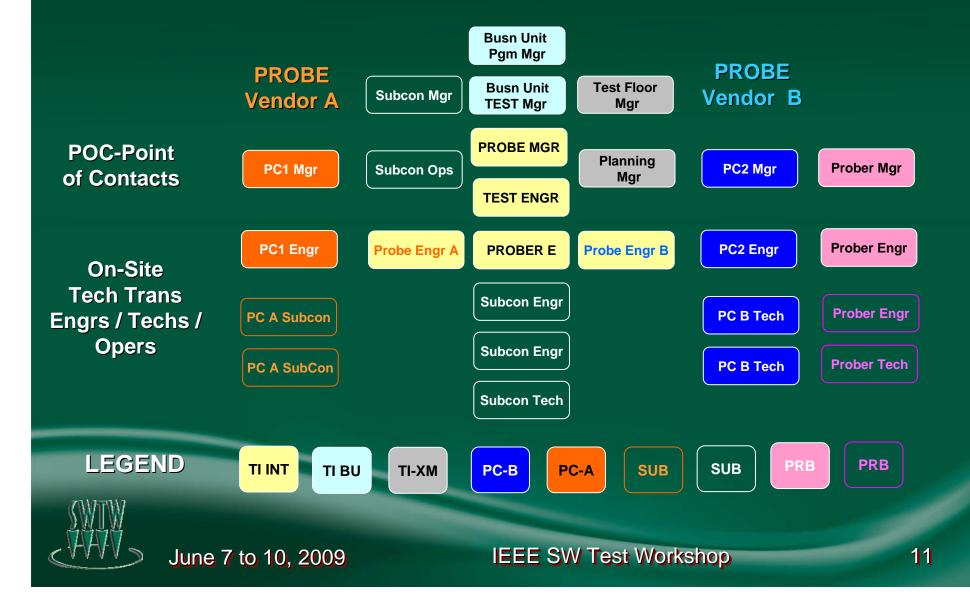
CTF Critical-to-Function Qualification Areas

	DEVICE 11/7/2007	PROBE CARD QUALIFICATION CTF-AREAS / PARAMETERS	TECHNOLOGY QUALIFICATION	PRODUCTION QUALIFICATION		
					Meets required CTF-Critical To Function parameters. Passes qualification category for the particular probe requirements envelope or node intended. e.g. 70 um, x32/x64 multi-site, CD14 enablement	
	ITEMS HIGHLIGHTED IN Red, considered	LEGEND	PASSES Qualification Category		Meets most CTF-Critical To Function parameters. Passes qualfication step. However, contingent on additional data, data analysis either on-line or off-line to resolve.	
	RED, CONSIDERED MUST HAVES		DOES NOT QUALIFY		Does not meet most CTF-critical to function parameters. Does not pass qualification category. Not considered a show-stopper; however, ARs required to be resolved	
			DOES NOT QUALIFY		Does not meet required CTF-critical to function parameters. Does not pass qualification category. Considered a show-stopper, significant work required to resolve.	
ITEM#	CTF AREA	CTF PARAMETER	TECH QUAL Category	PROD QUAL Category	STATUS- ACTIONS REQUIRED	OWNER(s)
1		•Pitch	60um	60um		J
2		•Pincounts	1216	1216	152 probes/die x 8 DUTs	J
3	•Nulti.site •Planarity		8	8	Skip 1 row and 1 column with 2by4 layout	Jī
4			25um	25um		
5	PHYSICAL	•Maximum Overdrive	75um	60um	FFI Spec is max 75um but restriction to current release process spec of 60um	J
6		 Probe Working Area 	Pass	Pass		Jī
7		 Component Area 	Pass	Pass		J
8	•PCB Mfgr/Functionable		Pass	Pass	PCB design worked right of the box	J
9		•PCB Design Make Flow •Routing Die Design •Probe Design	Pass	Pass	Design took too long to complete	FFI/MTI
10	DESIGN PROCESS		Pass	Pass	Site remapping due to FFI PCB Design optimization	FFI/MTI
11			Pass	Pass	Inadequate tip pre-condition at time zero	FFI
12		•Capacity •Leadtime	Pass	Pass	Delivery of 1st article was delayed numerous time due to PCB design. — Lead time: Re-order 6wks	
13	MANUFACTURING		Pass	Pass		
14	•Delivery		Pass	Pass		
15		•PC Analyzer	Pass	Pass	No RASP x1 mother board in FFI-TSC	
16	SUSTAINABILITY	 Repairability 	Pass	Pass	FFI-TSC had demonstrated numerous time on quick tum repair.	
17	n	•On-Site Support	Pass	Pass	Limited FSE and is a concern on ramp production situation	

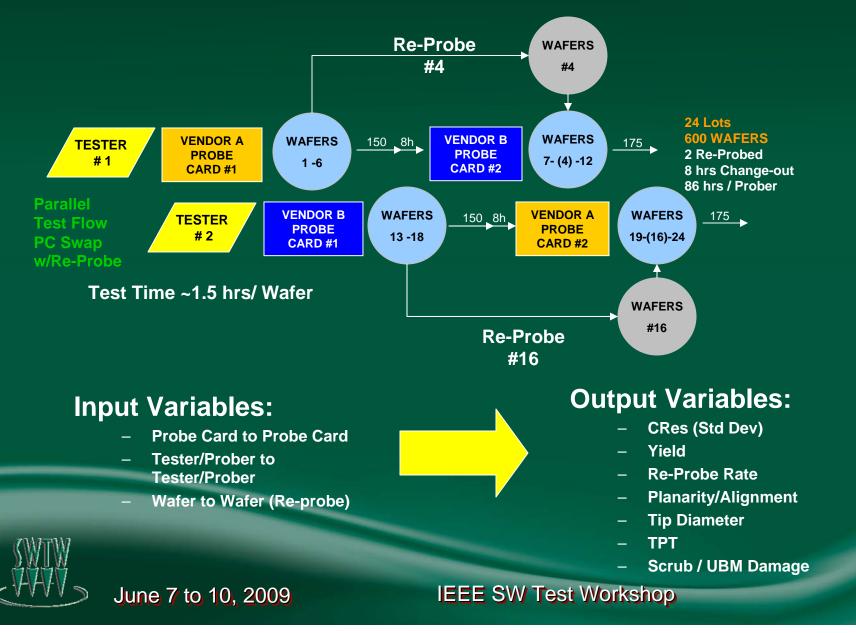
- PHYSICAL

- DESIGN PROCESS
- MANUFACTURING
- SUSTAINABILITY
- TEST PERFORMANCE
- RELIABILITY
- TEST OPERATIONS
- FUTURE
 APPLICABLITY
- COST OF
 OWNERSHIP
- OVERALL ASSESSMENT

Qualification Team Structure: EXAMPLE: FOR A DUAL COMPARATIVE QUALIFICATION

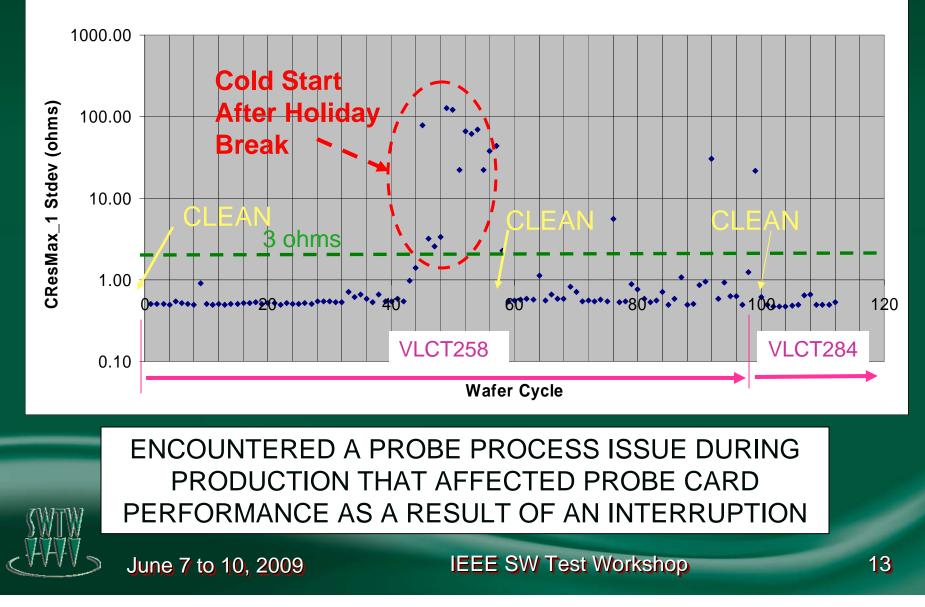


TEST FLOW FOR PRODUCTION QUALIFICATION-RTP



Example: Effect of Downtime

CResMax_1 Stdev (Ohms) PC#01



KEY MESSAGE

- The probe technology may appear to work from the outset, but need the production time to expose the technology to various use conditions.
- A high number of TDs not necessarily required, but by designing evaluation DOEs for multiple set-ups, change-outs, test program checks, etc., the production issues are given more opportunity to appear and resolve earlier.

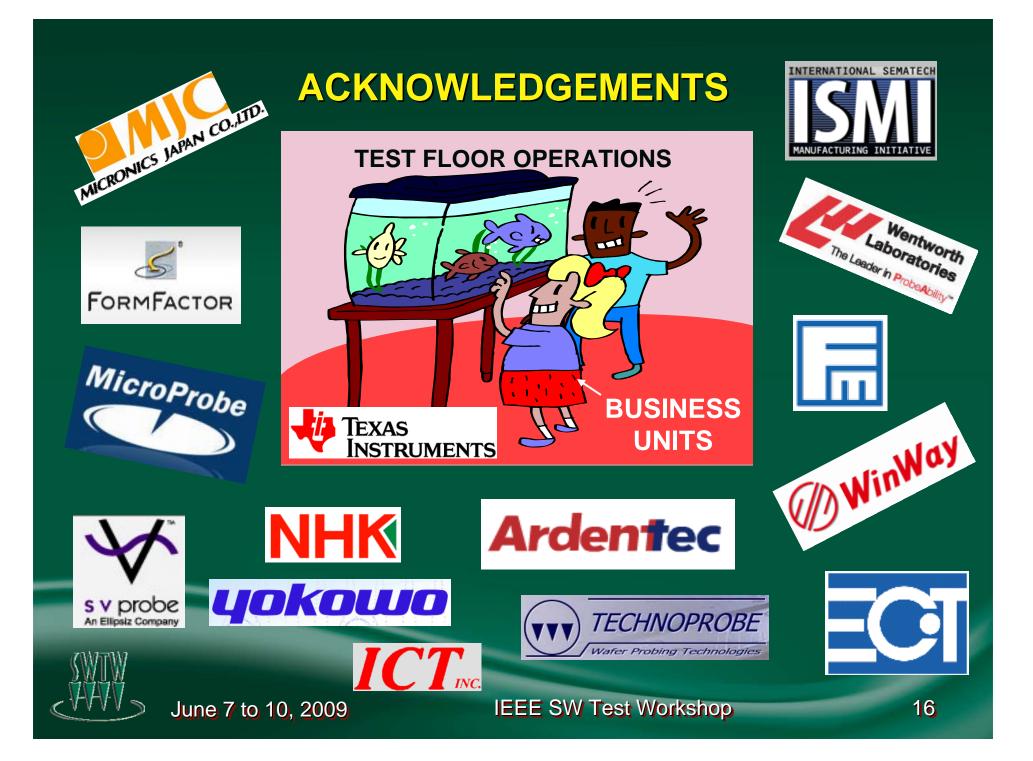


KEY LEARNINGS

- Project management CPM-critical path methodology proved critical to success: Key obstacles identified ahead of time to still meet major milestones.
- Cross-matrixed organizational structure formed across TI, vendors and sub-cons covers key personnel and technology requirements with roles / responsibilities clearly defined.
- Both on-site (TI-Dallas) and off-site (Sub-con) training provided by TI and vendors for both engineering and operators facilitates probe technology integration.

A Test Plan is CRITICAL









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