Novel direct probe solution for opto-electronic wafer-level PIC testing

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Overview

- **Introduction Ayar Labs**
- **Application (DUT for Photonic Test)**
- **Current Wafer Sort Flow**
- **Intended HVM Test Cell**
- **Technology Demonstrator**
- **Measurement Results**
- **Summary**
- **Outlook**

Introduction to Ayar Labs

We Design and Sell Optical I/O
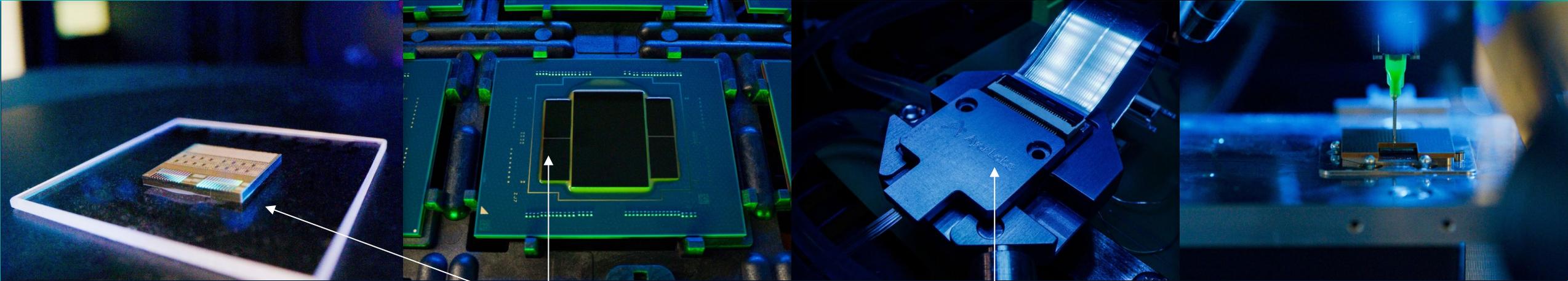
TeraPHY™ optical
I/O chiplet

SuperNova™
light source

Our solution is delivered as a CMOS based
electronic/photonic chiplet using an external CW-WDM light
source.

TeraPHY Product
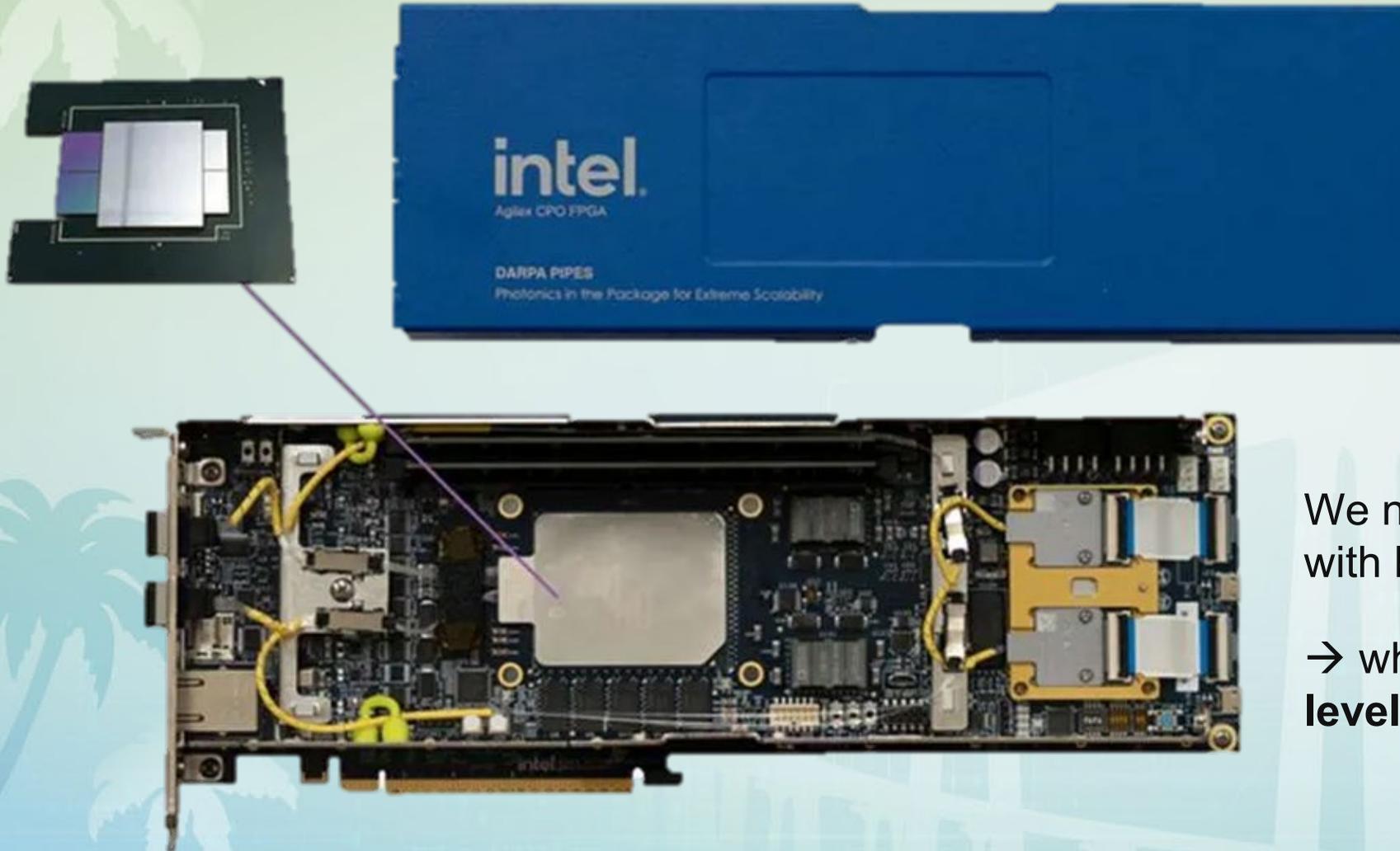
TeraPHY is an **optical I/O chiplet**, which our customers will co-package with their die (CPU, GPU, FPGA, etc)

We need to provide our customers with known-good-die (KGD),

→ which means **extensive wafer-level screening.**

Application (DUT for Photonic Test)

- Wide parallel interface (Advanced Interface Bus)

  – 4 Tbps bidirectional bandwidth
  – 8 transceivers (Laser, Tx, Rx)
  – 8 wavelengths per transceiver
  – 32 GBaud per wavelength

- Final test must be performed at wafer level to deliver known-good die (KGD)

AIB microbumps

Core bumps

Wafer Sort

Advantest V93k
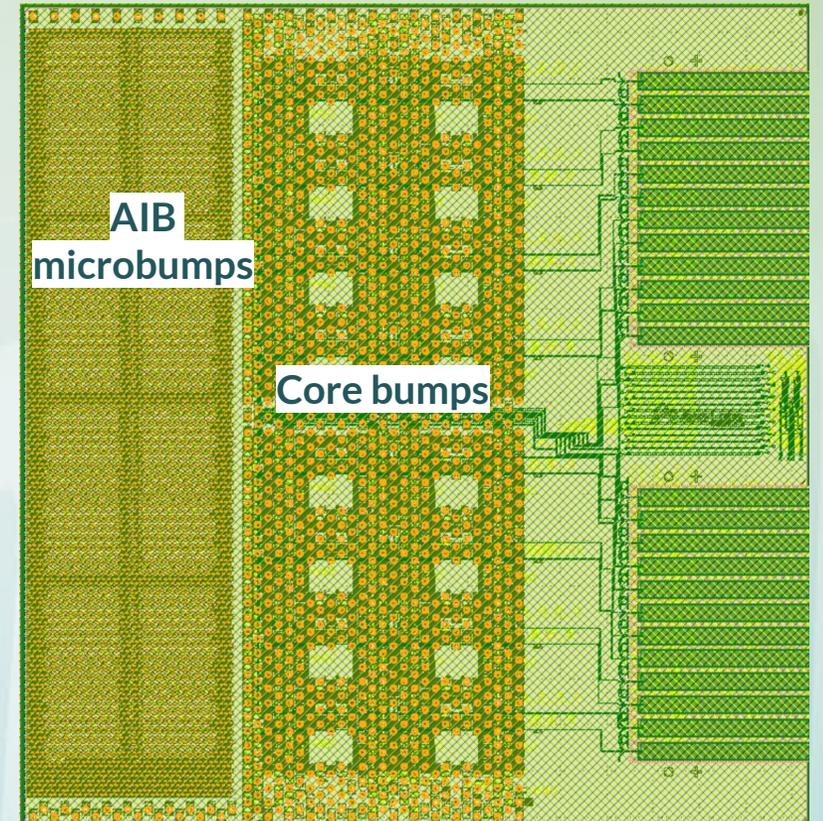
- **Dual test insertion**

- **Electrical Wafer Sort (V93K ATE)**
  - ~1400 bumps for electrical connectivity
  - Standby current, scan test, DFT, and at-speed functional test

- **Optical Wafer Sort (CM300-SiPh probe station)**
  - Optically couple into chip through edge couplers at wafer level
  - Passive optical characterization

CM300-SiPh
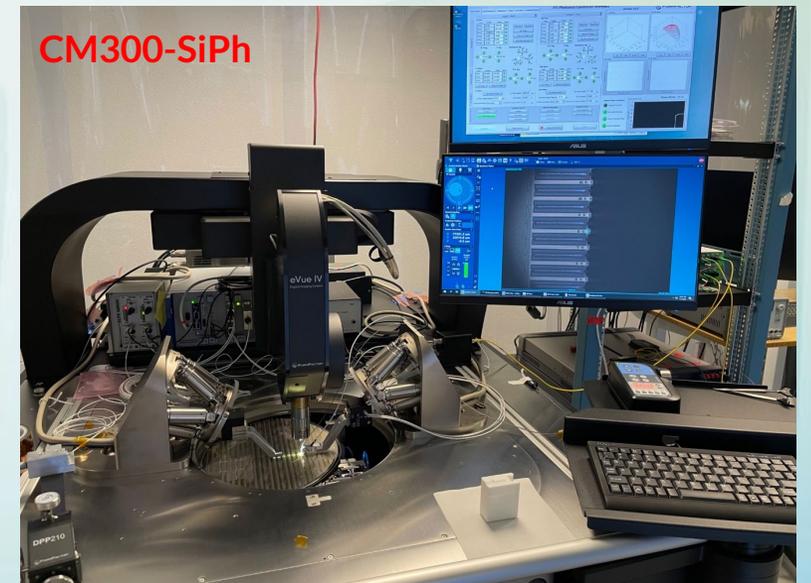
Wafer Sort

- **To meet cost targets, silicon photonics must use standardized equipment that can be shared across multiple customers**
  - Today, silicon photonics probe platforms and testers are customized to specific products
    - → Test equipment must be consigned, or production run in house
  - Future: Convert Cap Ex into Op Ex by running test subcontractors

- **Drive to single test insertion on standardized platform for high volume manufacturing**
  - Test cell needs to provide both optical and electrical connectivity to DUT electro-optic final test

HVM Test Cell

- **Target HVM test cell**

  – **As easy to set up as pure electrical wafer sort test cells**

  – **Fully connected optical and electrical resources with docking test head to prober/probe card**

- **Key building blocks**

  – **Direct dock enabled UFO probe card**

  – **Reliable and durable optical blind mate connection at DUT interface**

  – **Test head side panel access to required optical and electrical rack resources**

GPIB

ATE control

LAN/USB/RS232

0.00000

laser source

0.00000

polarization controller
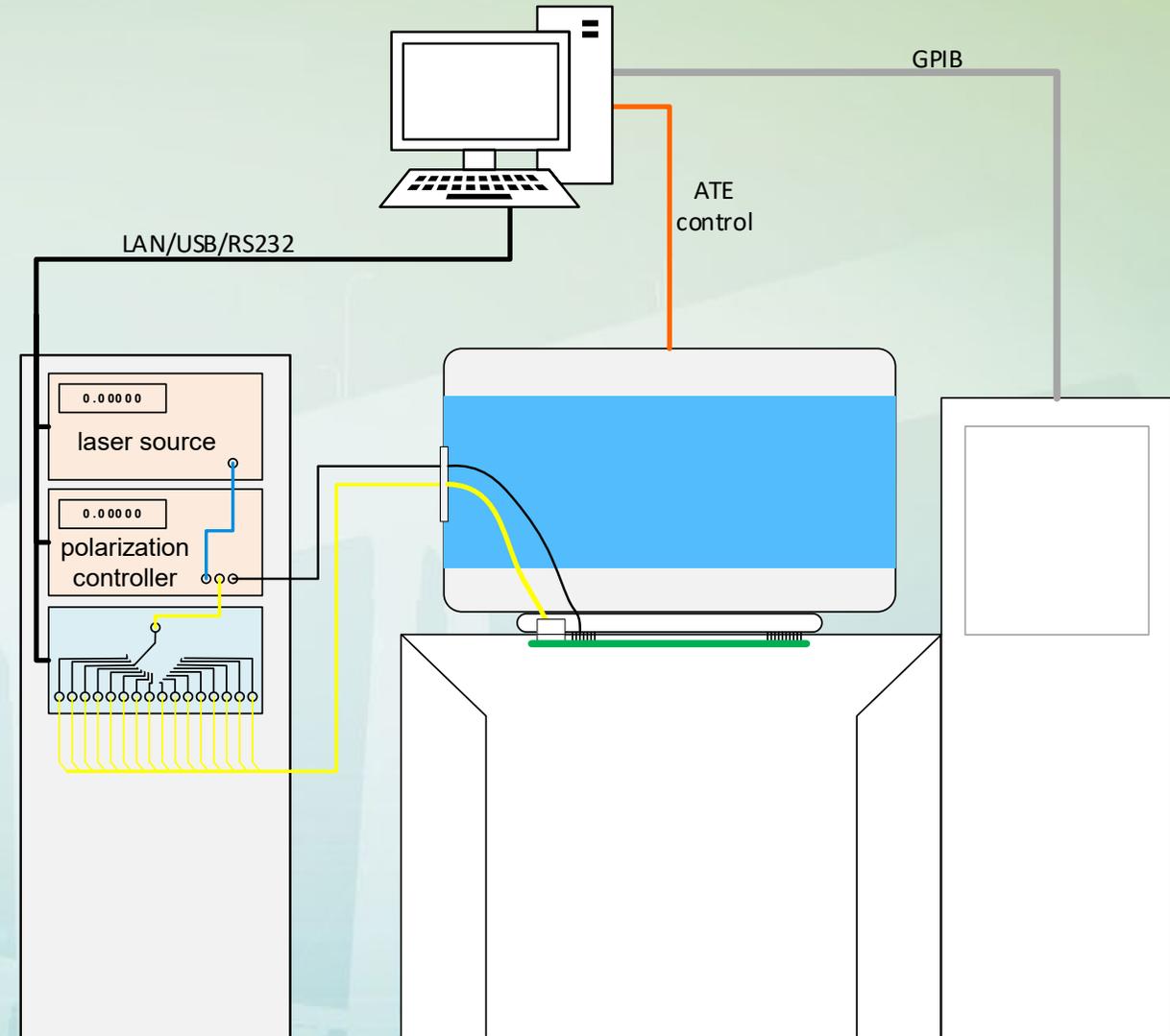
Challenges towards HVM Test Cell

- **Direct docking E/O probe card, especially for the optical docking**

- **Test cell integration into ATE Test Cell Control environment**

  - **Control of external instruments**

  - **Mechanical integration of additional E/O signal paths**

  - **Additional functionality for initial E/O alignments and setups**

- **Integration into an OSAT environment**

GPIB

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0.00000

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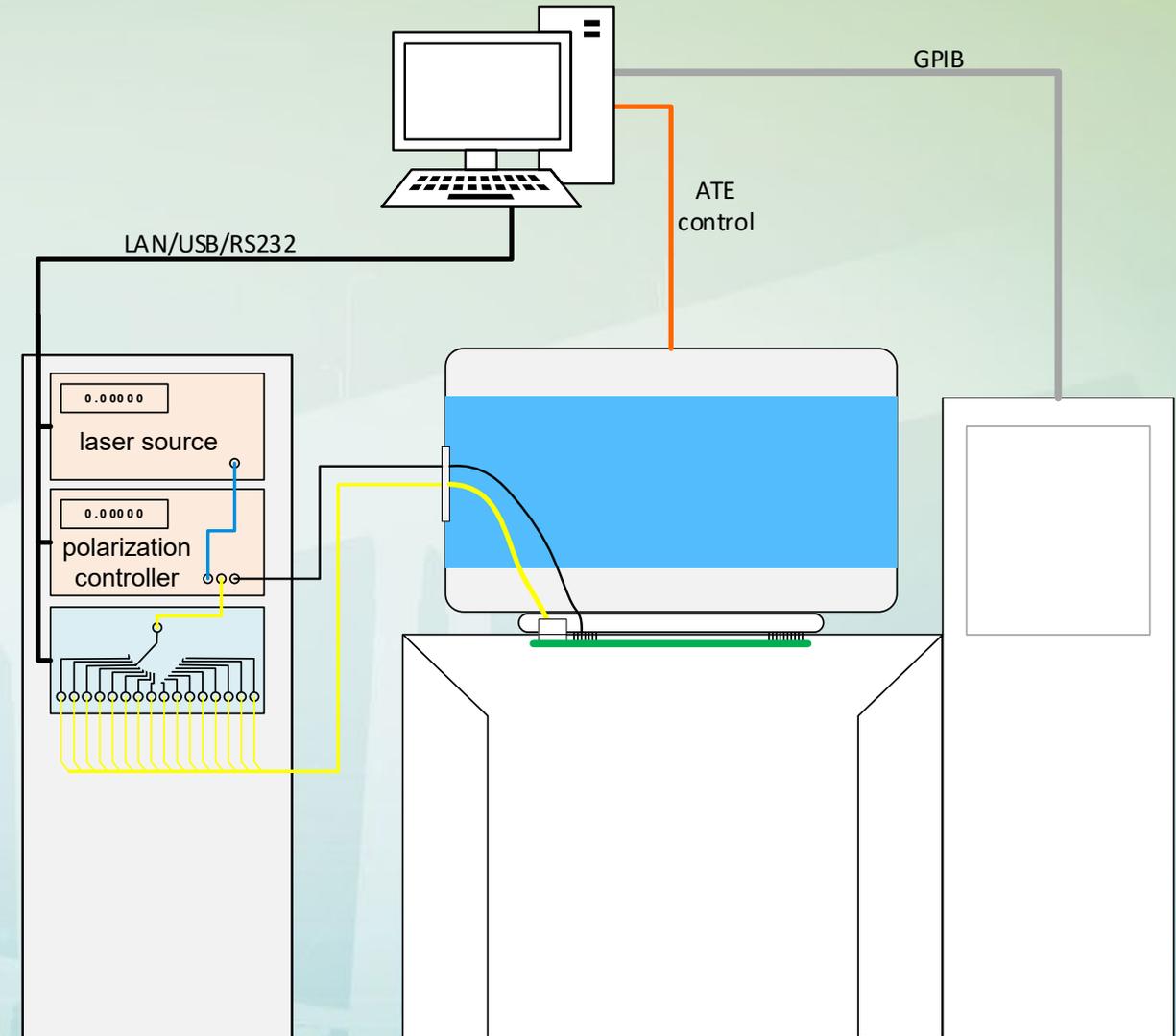
Test Device

- **Dedicated test die on the reticle**

- **Passive sites**
  - 5 rows x 8 grating coupler loopbacks per row
  - **Design of experiments to improve coupling loss to optical probe card**
  - **Measure wavelength dependent insertion loss**

- **Electro-optic sites**
  - **Grating coupler inputs to photodetector**
  - **Measure wavelength and power dependent photocurrent**

3	6	9	13	16
2	4	**7**	12	15
1	5	8	11	14

Photo diode setup

Grating couplers

Photodetectors

Bond Pads
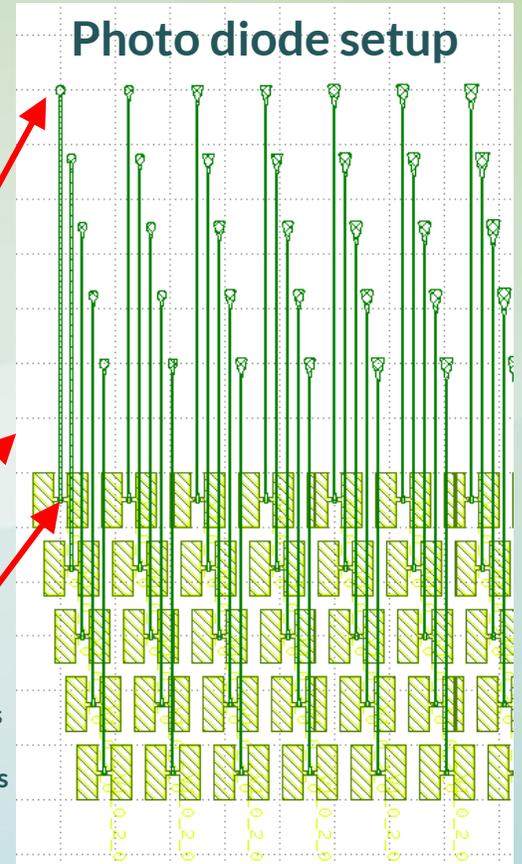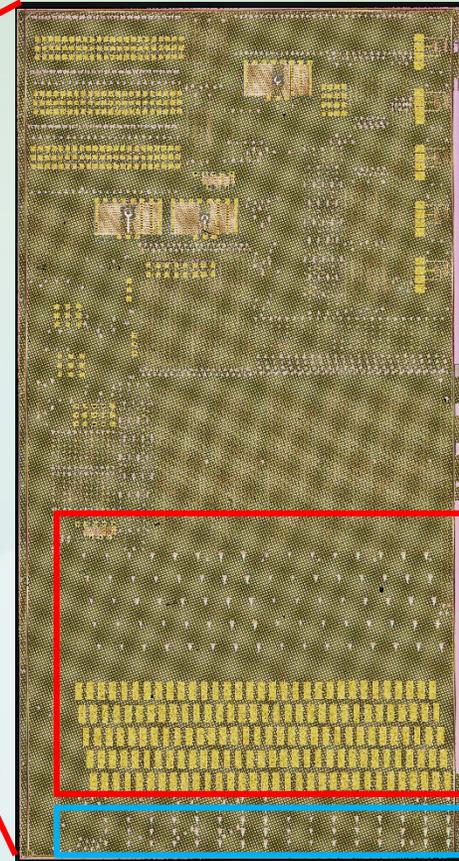
Loopback channel setup

Grating couplers
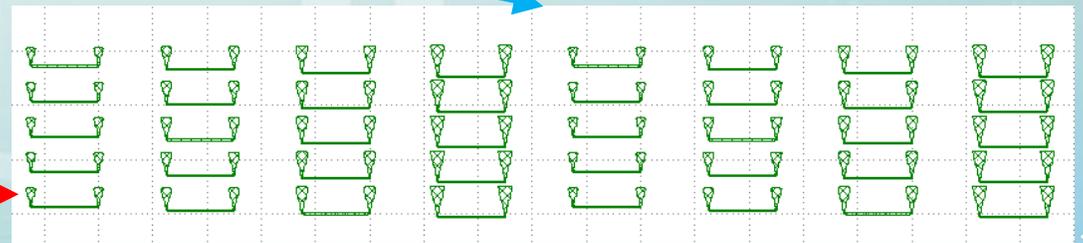
Technology Demonstrator - Setup

- **Probe Card: UFO Probe™ TechDemo**

  - Probe card format: V93000 direct docking
  - 32 cantilever needles (PD pads)
  - 16 channel optical probe head
  - Optical SM fiber connection with MPO connector
  - Capacitive distance sensor (CAP sensor)
  - Feedback loop to polarization controller
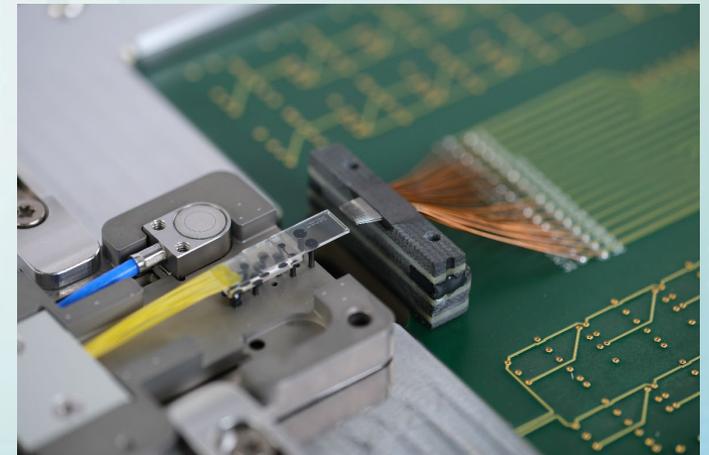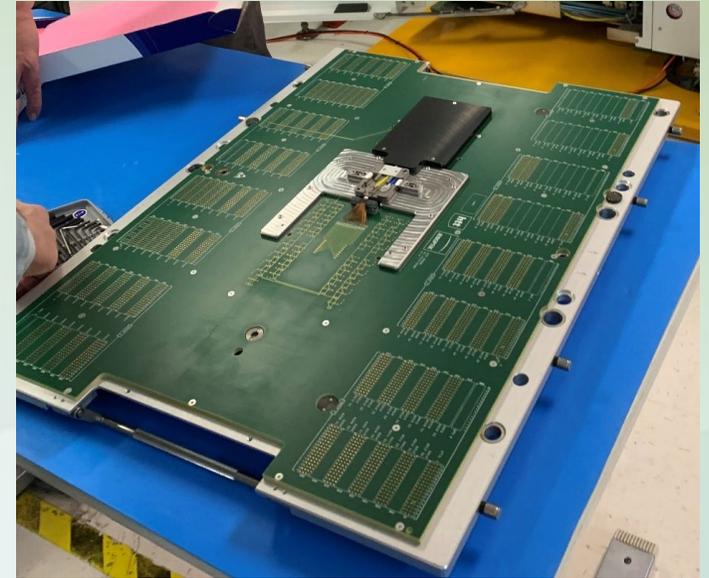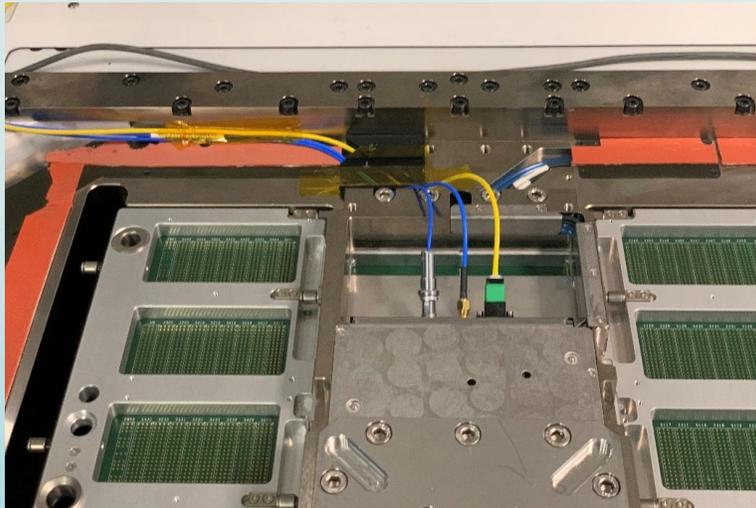
Technology Demonstrator - Setup

- ● **Probe Card: UFO Probe™ Working Principle**

  - – **Simultaneous optical and electrical probing in a single touch down**
  - – **Monolithic integrated optical module**
  - – **Alignment insensitive optical coupling for vertical emitting PICs**
  - – **Compensation of coarse prober position tolerances**
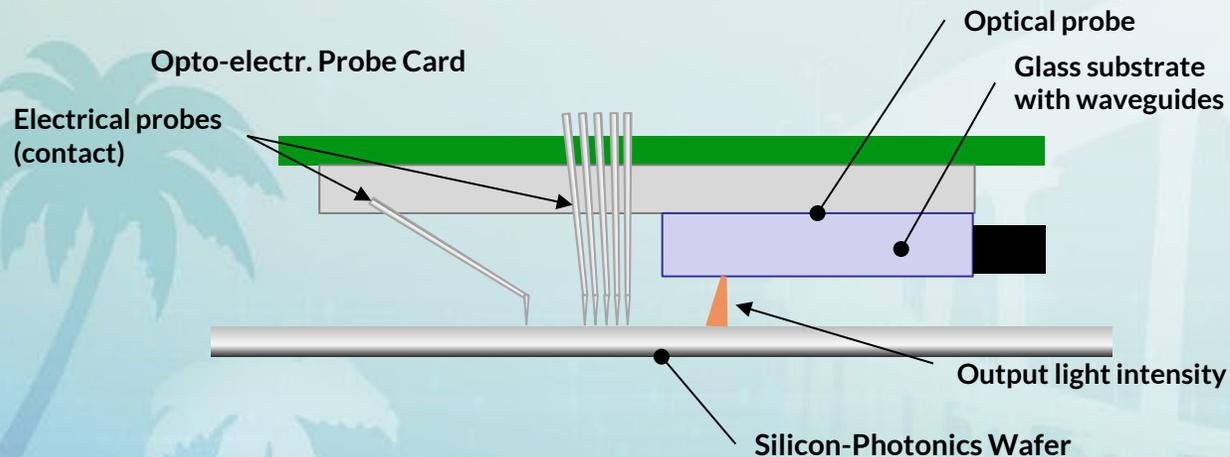
Optical concept compensates prober alignment tolerances.

Opto-electr. Probe Card

Electrical probes (contact)

Optical probe

Glass substrate with waveguides

Output light intensity

Silicon-Photonics Wafer

Expected input light intensity profile of Grating Coupler

Shaped intensity output profile of probe card

Prober position tolerance

Grating coupler

Needle / Bond pad

Prober position tolerance

Silicon Photonics Wafer on prober chuck
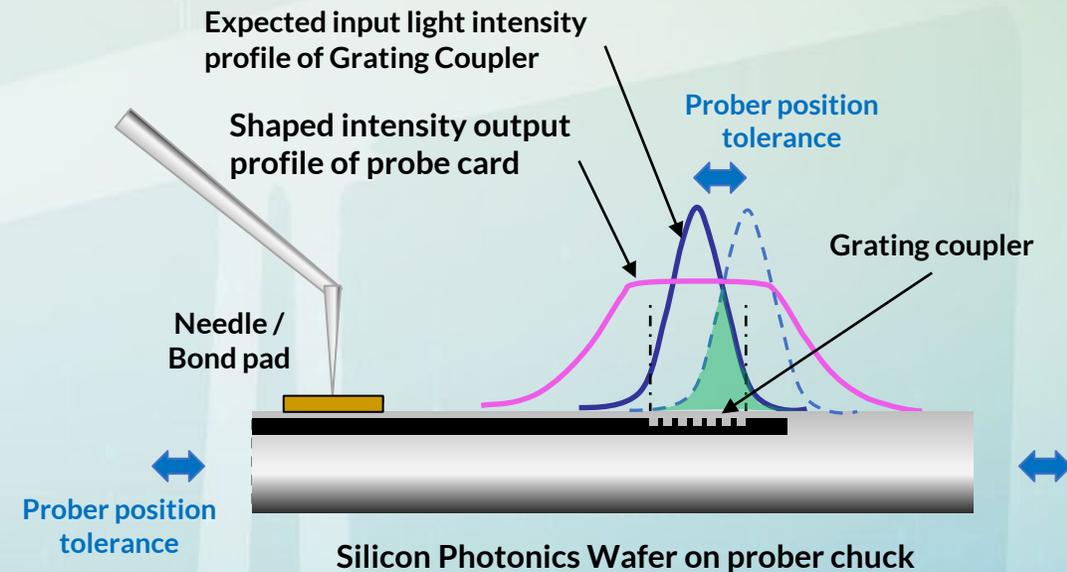
Technology Demonstrator - Setup

- **Prober: Standard TEL Precio XL**
  - **Prober control by ATE prober/handler driver via GPIB**

- **Tester: Advantest V93000 SmartScale**
  - **AVI 64 for photodiode current measurements**

- **Optical Test Equipment (rack & stack):**
  - **Santec TSL-570 tunable laser**
  - **Luna POS-203 Polarization controller**
  - **DiCon Fiberoptics MEMS 1x16 switch module**

- **Probe Card: UFO Probe™ TechDemo**
  - **V93K direct docking format**
  - **Cantilever needles and optical module**
  - **Microepsilon capacitive distance sensor**

GPIB

ATE control

LAN/USB/RS232

0.00000

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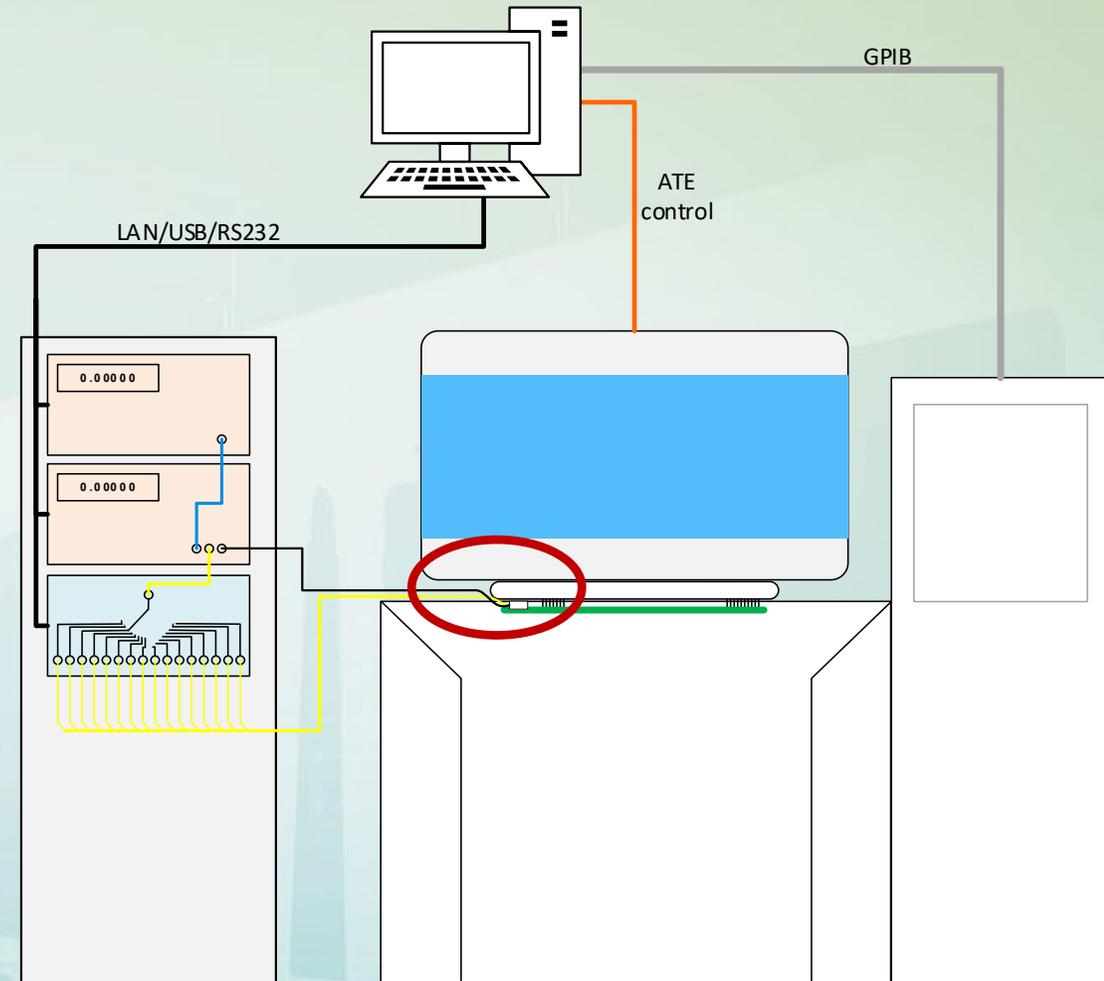
Technology Demonstrator - Setup

- **Prober: Standard TEL Precio XL**
  - Replaced sealing with 3D printed cable duct for optical and electrical cable access on docking plane (picture lower r.h.s)

- **Tester: Advantest V93000 SmartScale**
  - Top covers removed to reduce stress on optical and electrical cables when docking to prober

- **Probe Card: UFO Probe™ TechDemo**
  - Connector panel as separation plane for electrical and optical cables installed on probe card stiffener
  - After loading probe card, required connections were set up manually between rack and connector panel
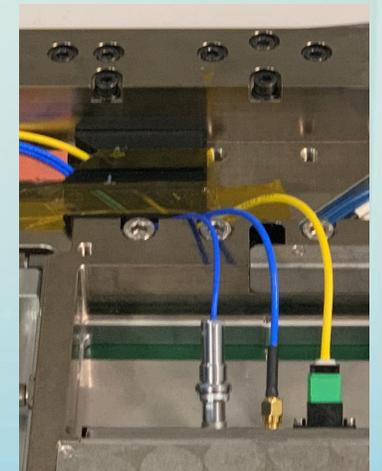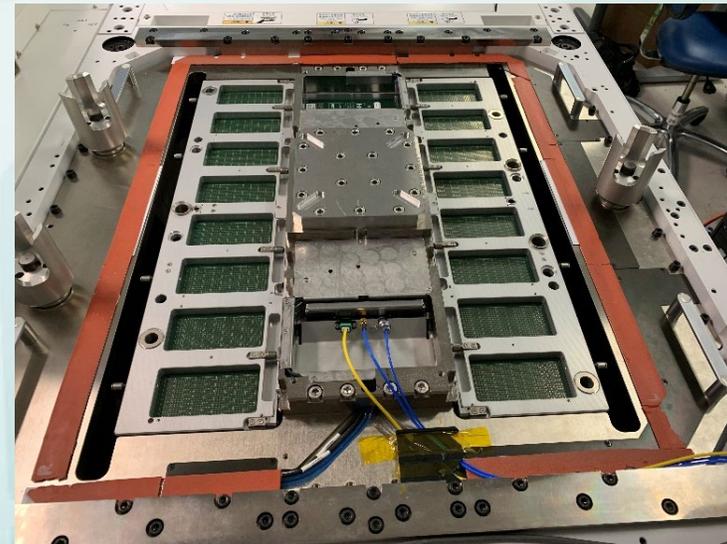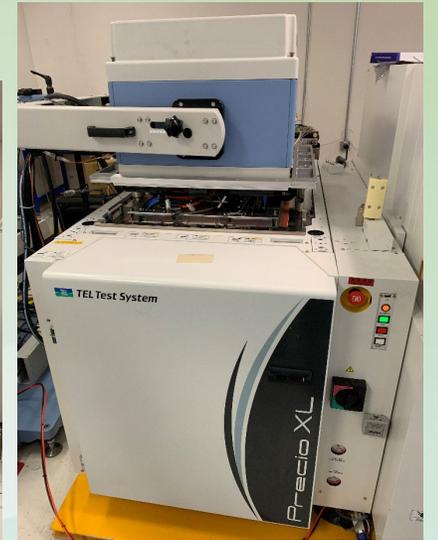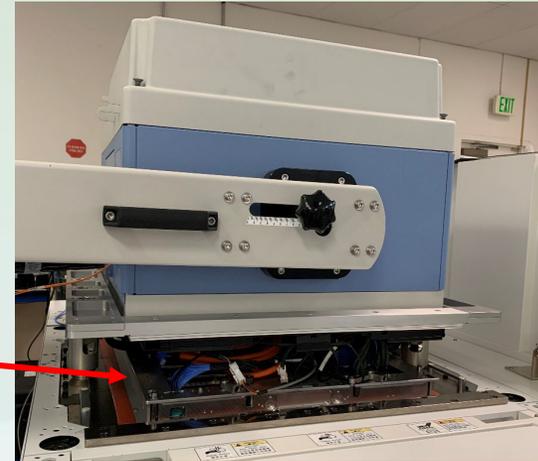
Measurement results

- **Qualification of loop-back in Lab setup**
  - **Prior to prober measurements, the loop-back channel were qualified in a lab setup with same optical module**

  - **No prober but a xy-scanning setup was used**

  - **Entire loss of loop-back 15-17dB (including overfilling losses)**
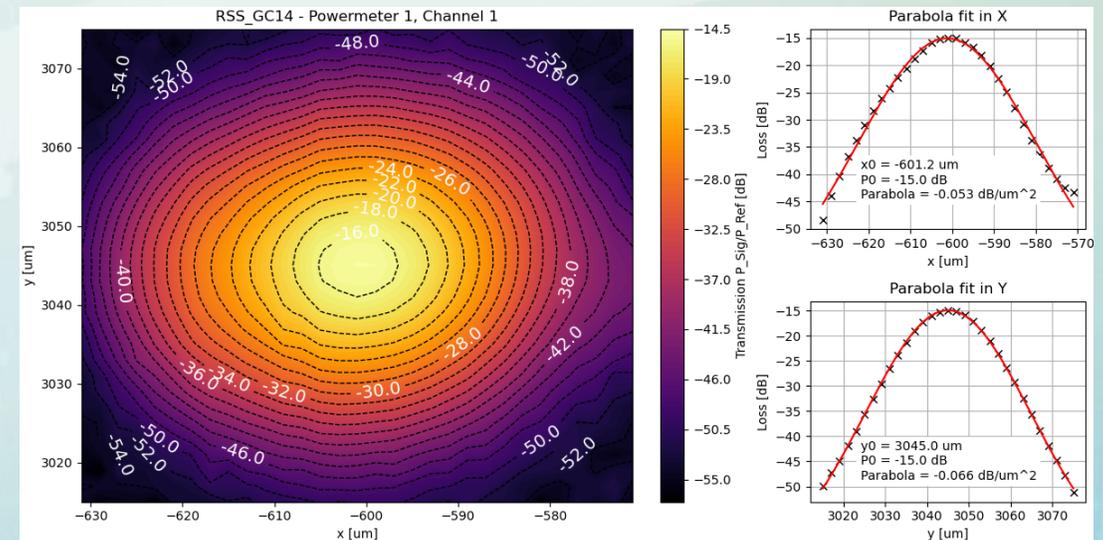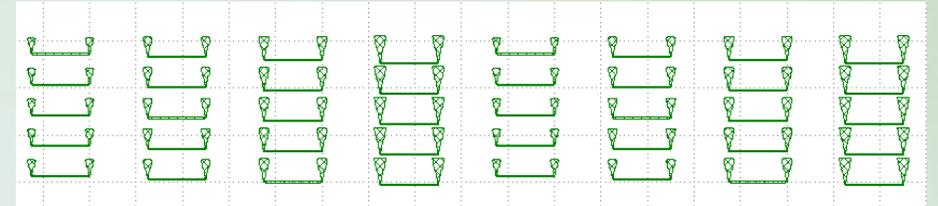
Measurement results

- **Measurements at iTest**

  - **Tolerance against alignment inaccuracies**
  - **Prober positioning accuracy typ. 2µm**

grating coupler

Ch1 Ch2 Ch3 . . .
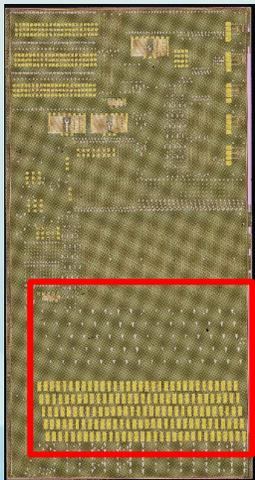
Site 5
Site 4
Site 3
Site 2
Site 1

~15 µm
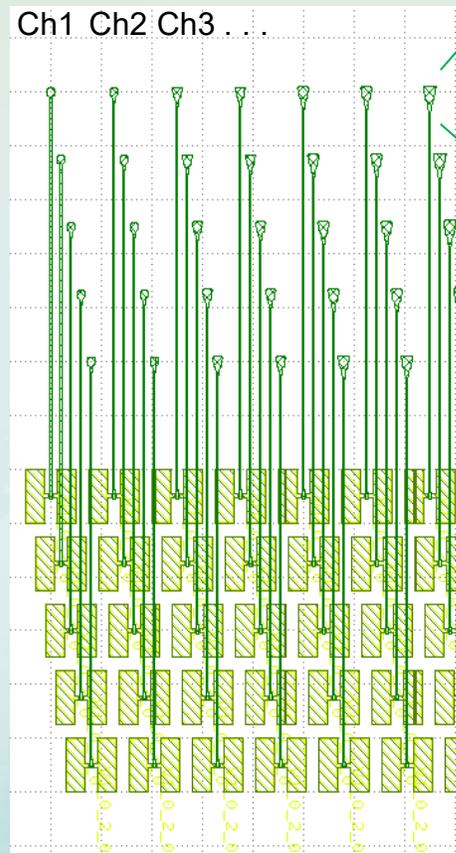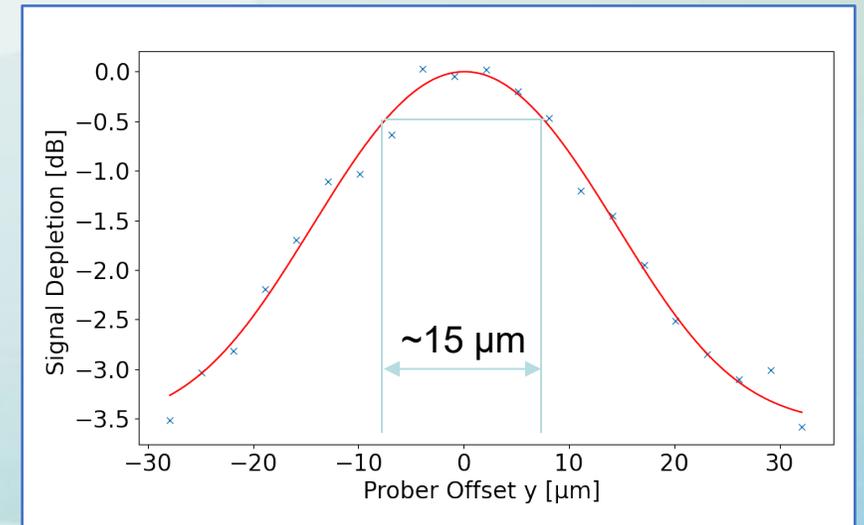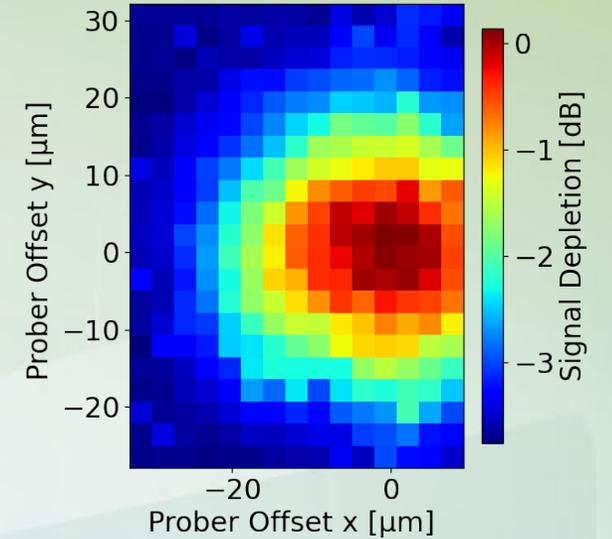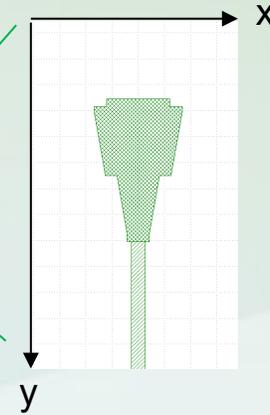
Measurement results

- ## Measurements at iTest

  – **Wafer and site (sub-die) stepping without extra optical alignment per die**

  – **Demonstrator setup allows characterization of chips**

  – **Wavelength scan, maximum at site 1 (@ ~1316nm)**
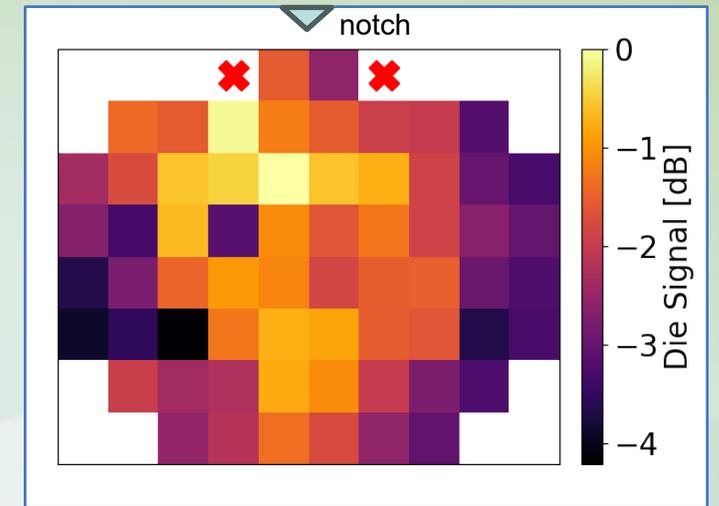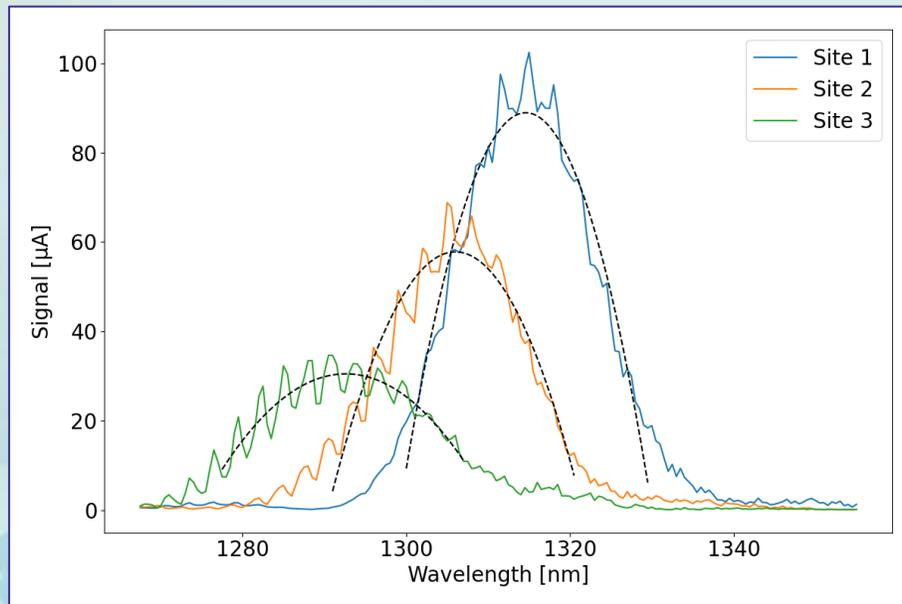
Wafer map channel 4
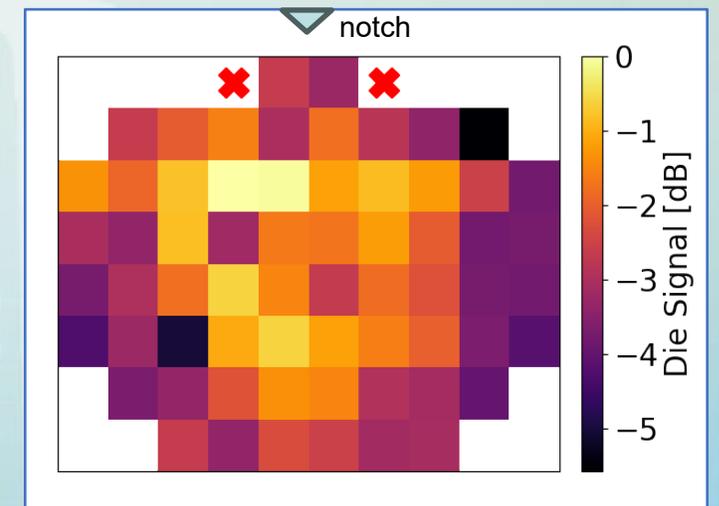
Wafer map channel 8

Conclusion

- **We demonstrated**

  - That a Standard IC Test Cell can test photonics

  - Direct prober loading of an E/O-probe card

  - Tester direct docking with an E/O-probe card

  - Tester/prober/external instrument handling

  - Initial lateral E/O-probe card alignment

  - Wafer and site (sub-Die) stepping

  - Wavelength scan
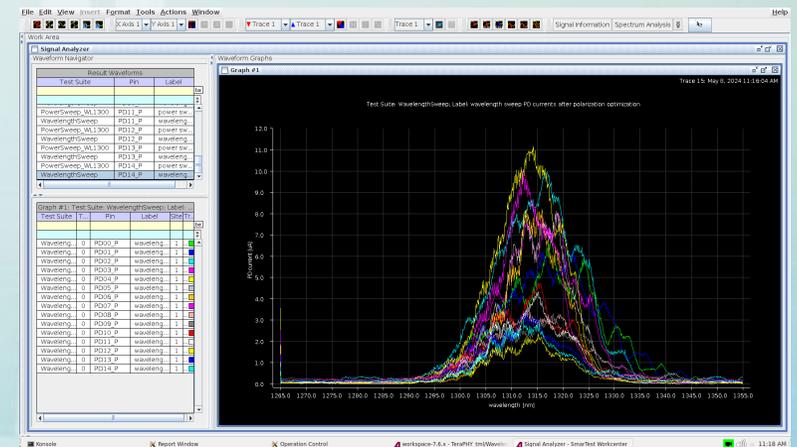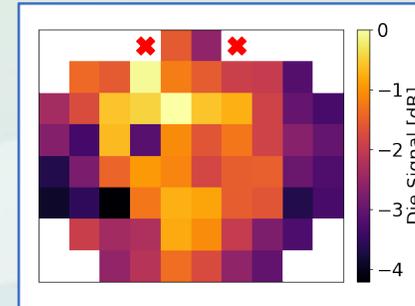
Outlook

Way to full HVM Test cell

- **UFO Probe integration with Vertical Needles already demonstrated (UFO Probe™ Vertical)**

- **Next logical step: "full chip" direct docking probe card for V93000**

- **Direct and automated optical docking of E/O Probe Card to tester → 'blind mate' connection**

- **Optical channel routing through tester**

- **Automated probe card initialization routines by tester**

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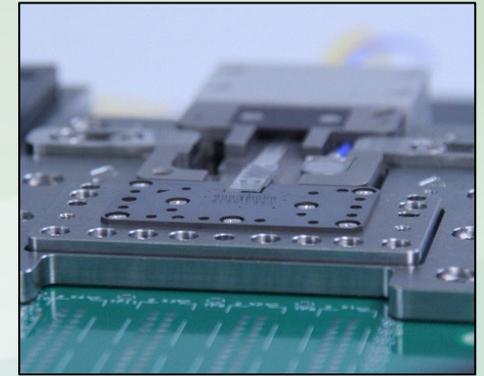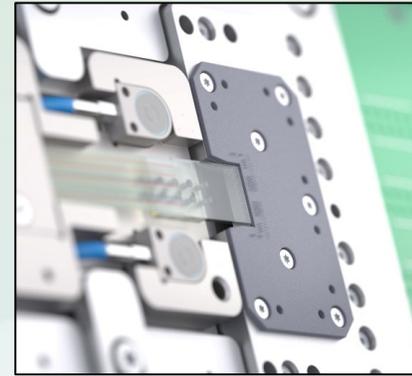
Acknowledgements

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- **Clemens Leichtle (Advantest)**
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