POSTER 11

Known Good Die
Best Practice for Probing High Power Devices

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Introduction

Renewable Energy
Semiconductors switching high currents at high voltages gain increasing importance. **Energy efficiency** is the main driver, essential for production-distribution-consumption of renewable energy.

Technology Transition
SiC and GaN materials have better electrical and thermal properties than silicon, allowing smaller device sizes with reduced losses.

SiC devices have best efficiency at medium switching frequency and very high voltage/power.

GaN devices use even higher switching frequencies allowing very compact circuitry at lower voltages.

Power Modules
A leading-edge power module for high power applications consists of multiple SiC MOSFETs, up to 24x and more. Due to high parallelism **minor defect rates** of singulated dies already lead to significantly **reduced final test yield**.

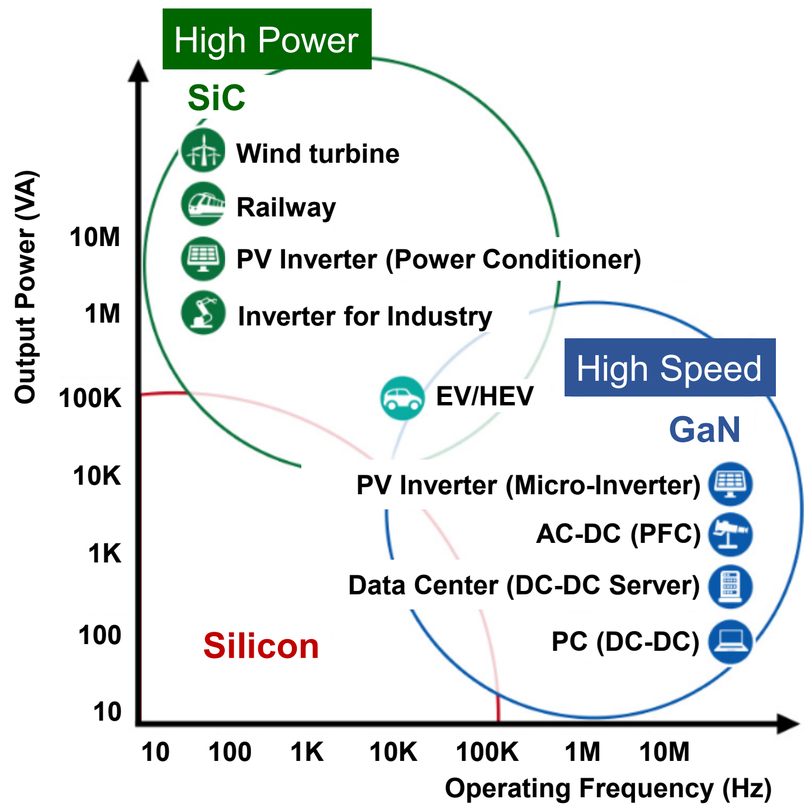
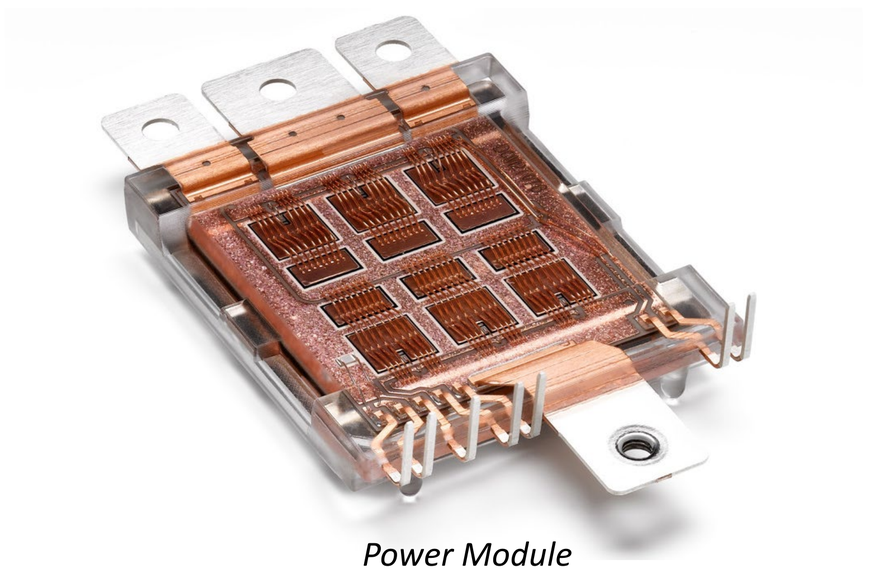


Image Sources:
1. Danfoss Webpage; https://www.danfoss.com/en-us/about-danfoss/our-businesses/silicon-power/danfoss-dcm-1000-power-module-technology-platform/
2. https://www.reddit.com/r/electronics/comments/qykjtl/salvaged_infineon_fs400r12a2t4_3phase_igbt_module/#lightbox



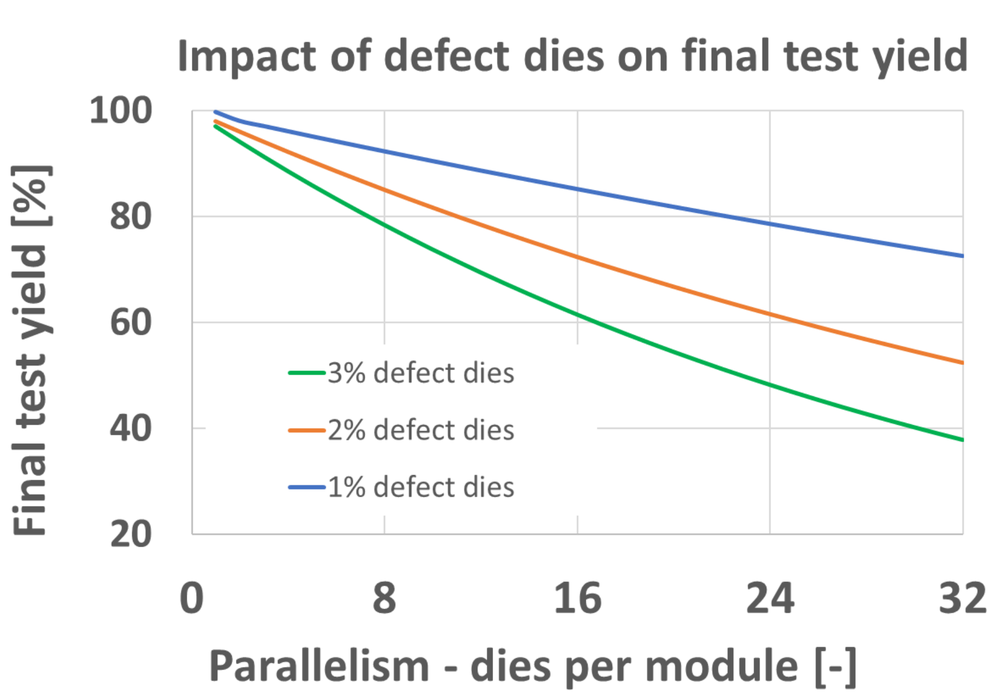
Power Module

Test Concept

Wafer Test not suitable
Wafer test is not able to **test in-depth** a SiC power device to further reduce the defect rate to the low parts per thousand range to get satisfying final test yield (see diagram on the right).

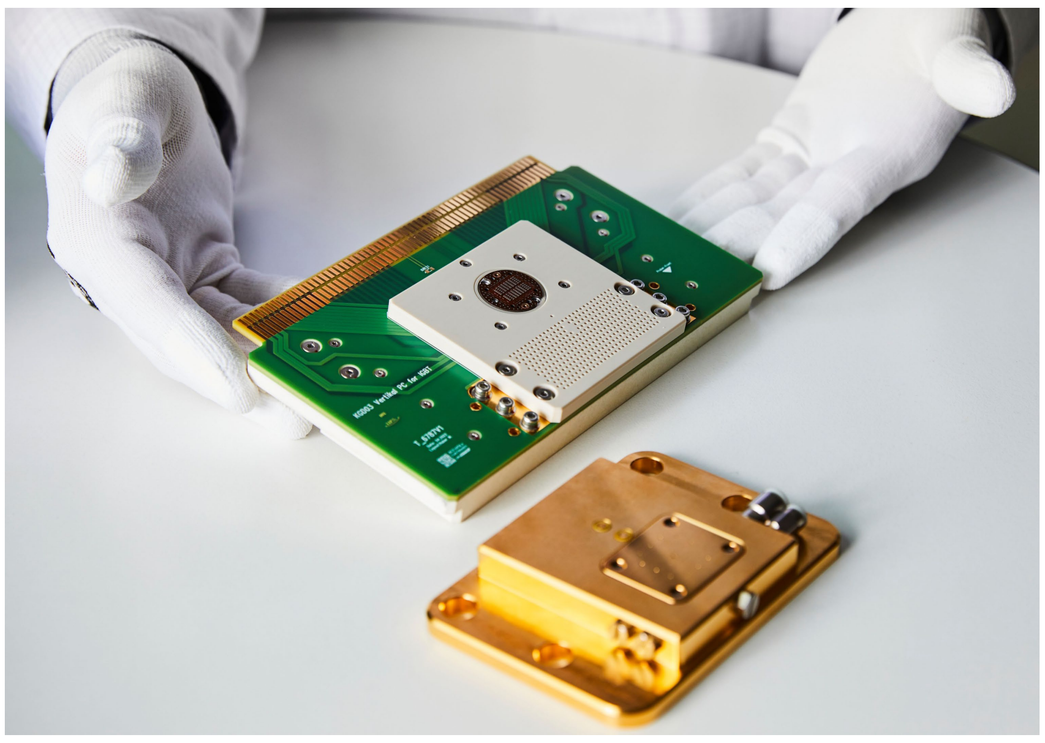
Crystal defects in the SIC substrate need a certain energy level to get detectable. If the test excites a defect, the chip quickly goes from being structurally sound to being short-circuit. At this point, the test needs to be **aborted** instantly **within nanoseconds** range.

High **parasitic inductance** of the entire test system dumps a large amount of electrical charge in a very small defect site. **Damages to** the **probe card** or to the **wafer** itself (cracks) are likely consequences.



Damages of Cutting Process
If only wafer test is performed, damages of the singulation process are not detected before device installation into the power modules.

Why Known Good Die (KGD) Test ?
- The entire test system meets requirements for low parasitic inductance with **instant current cut-off.**
- Test is done after singulation. **Damages of cutting** process **are detectable.**



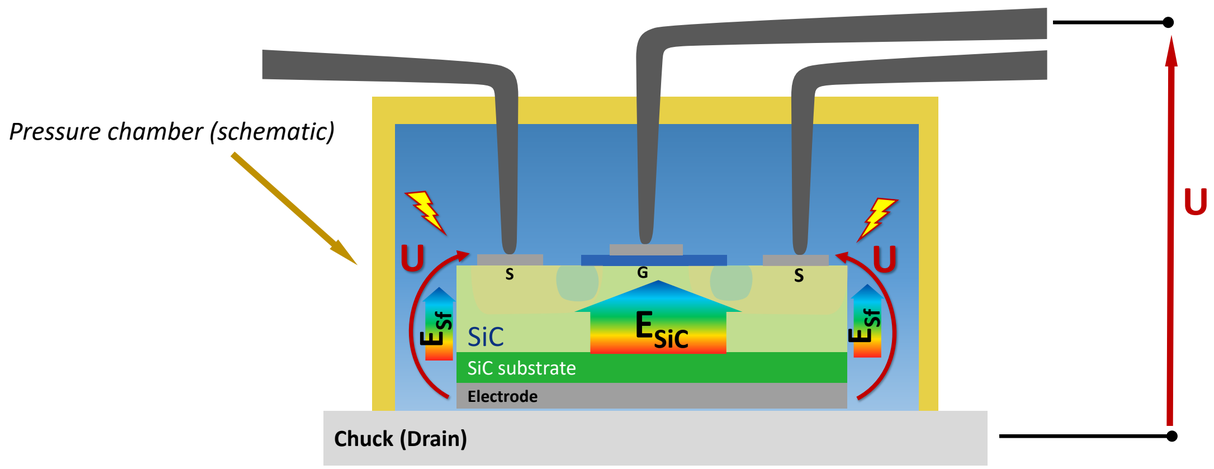
T.I.P.S. KGD (Known Good Die) Micro Contact System

Test Requirements

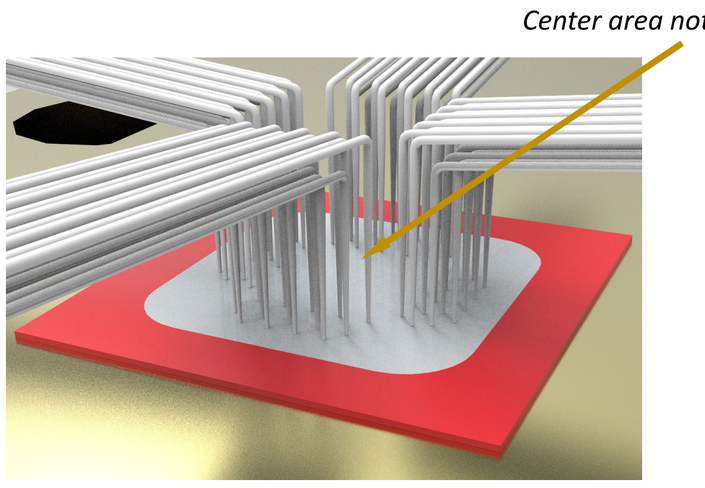
High Voltage – *Arcing Suppression*

KGD test regime includes high voltage tests **up to 3kV** which would lead to **flashovers** (arcing) between source/gate and drain potential if no suppression is active.

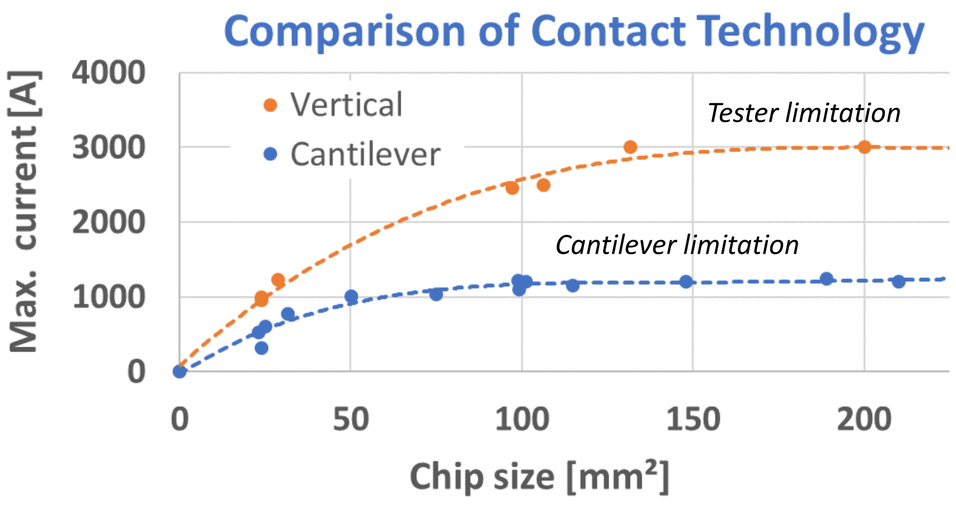
Breakdown strength of ambient air is low but increases with static pressure. Applying **higher** static **pressure** above the chip surface **suppresses arcing**. A probe card with integrated pressure chamber is used.



High voltage KGD test with arcing suppression



Physical constraints of cantilever probe cards



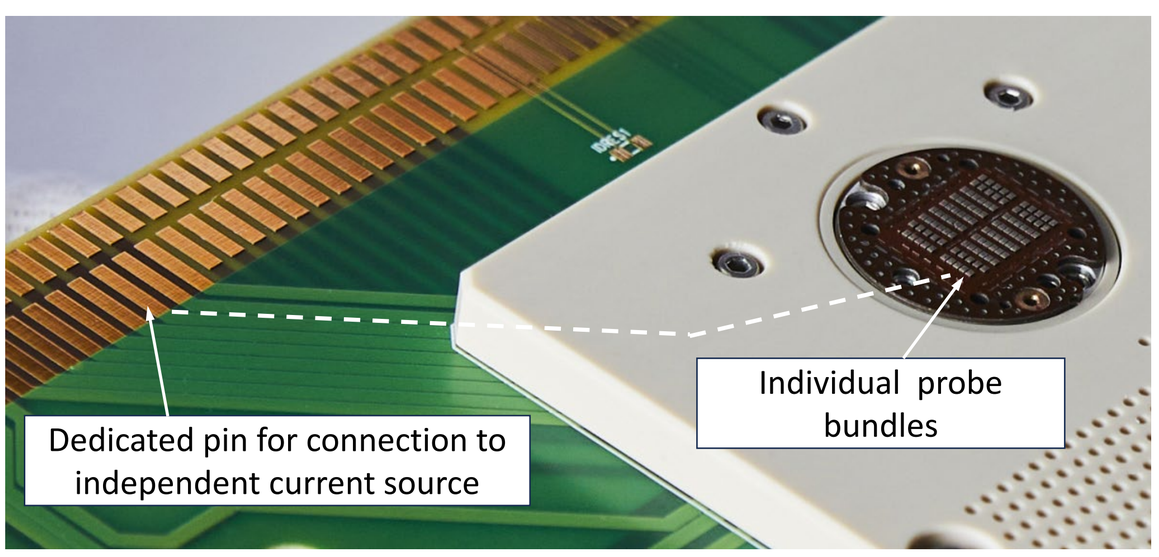
High Current – *High Current Density (A/mm²)*

Short circuit test requires **highest test currents for a few microseconds**. Means of choice in terms of micro contact technology (cantilever or vertical) depends on the **available chip pad size.**

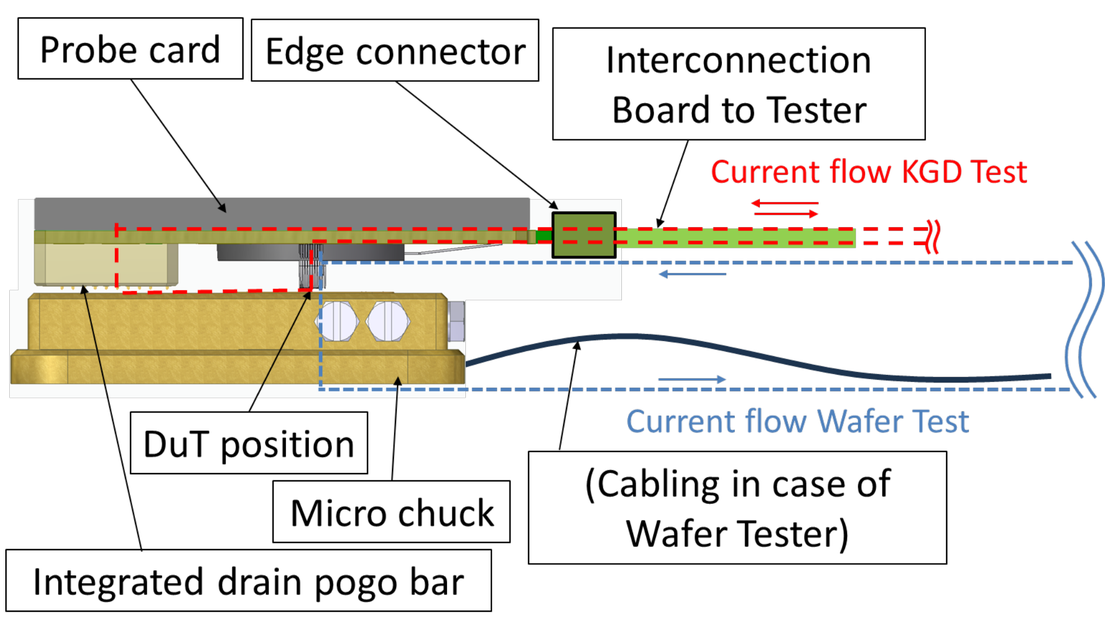
Vertical probes technology has an inherent advantage in terms of current density. A factor of 1,7 is already given for small devices. With larger devices physical constraints for cantilever needle spiders are increasing the advantage of vertical technology. While **vertical** probe heads are able to **access the entire chip surface, cantilever is limited** to a maximum number of probes layers causing a **“blind spot”** in the center.
Overall maximum of 3000A is related to tester limitation.

Current Monitoring – *Chip Failure Detection*

In case a failure is excited the device behaves short-circuited in a very localized area (hot spot). Probes close to this hot spot are forced to deliver significantly higher currents. This can be detected by the tester via **current consumption monitoring** of individual needles or bundle of needles. **Fast current cut-off** is crucial to prevent damages at the probe card.



Independent current source connected to individual probe bundle



Schematic illustration of conductor loop; KGD vs. Wafer Test

Fast Switching – *Reduced Parasitic Inductance*

To allow current cut-off in a **nano-seconds time scale**, **parasitic inductance** of the entire test system needs to be minimized to **below 50nH**. This requires a short distance between DuT and tester on the one hand. On the other hand the area spanned by the **conductor loop** (cabling, contact system, etc.) needs to be **minimized**.

A **comparison** between latest **KGD** test system developed by T.I.P.S. and a **conventional wafer probing** system illustrates the difference in the size of the conductor loop.

High Test Temperature – *Temperature accuracy*

For automotive applications test temperatures **up to 175°C are required**. KGD testing allows to use a closed pressure chamber touching the chuck surface (EWS needs hovering chamber). This results in **no air-cooling effect during the test**. Only chamber inflating and deflating before and after the test brings a minor temperature drop at the chuck surface which can be compensated via “chuck over-heating”. Calibration of necessary over-heating can be done with a temperature sensitive device without pressurized air at low voltage.

Challenges

Failure Modes

Crystal defects need a certain **energy of activation**. The key is to find the right amount of energy which separates the good devices from the defective ones. If the energy level is too high, the **failure mode can be very disruptive**.

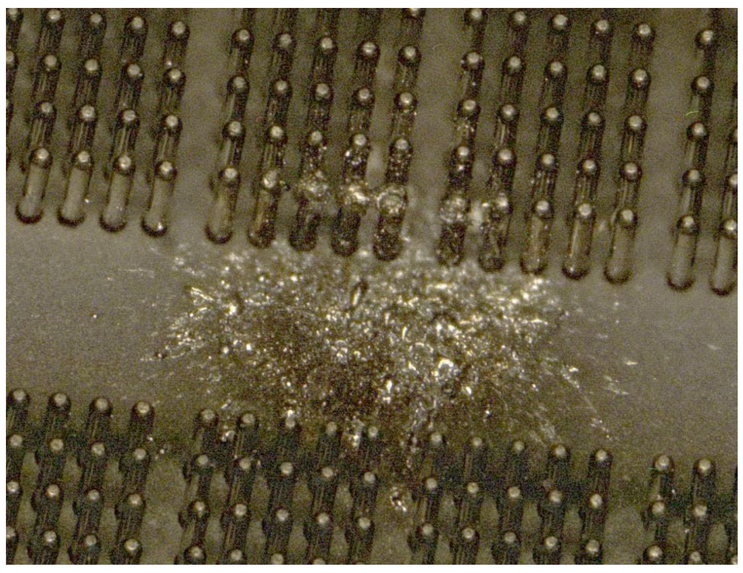
Uncontained Chip Failures

A catastrophic chip failure during test might result in a very localized **thermal runaway** ("hot spot") leading to melting, splashing and evaporation of chip pad metallization and its **spraying towards the probe head**.

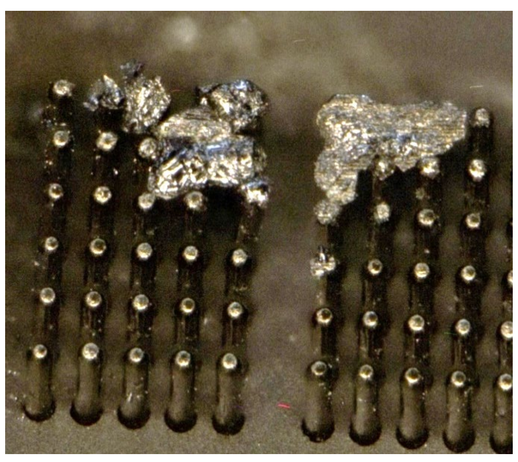
This type of contamination **increases friction** forces when needles are gliding in the ceramic guide holes. At a certain degree of contamination needle movement will be blocked, which leads to an excessive mechanical stress within the **guide plate eventually breaking** it.

Nuggets on Probe Tips

Probe tip is in **contact with liquid chip pad metal** during test. Once test is finished, the metal gets solid again and is soldered to probe tip. Parts of **metallization** (nuggets) are then **pulled out** when de-contacting.



Liquid metal splashed on the probe head



Metal contamination fused to probe tip

Corresponding void in chip pad metallization

Customer Responsibility

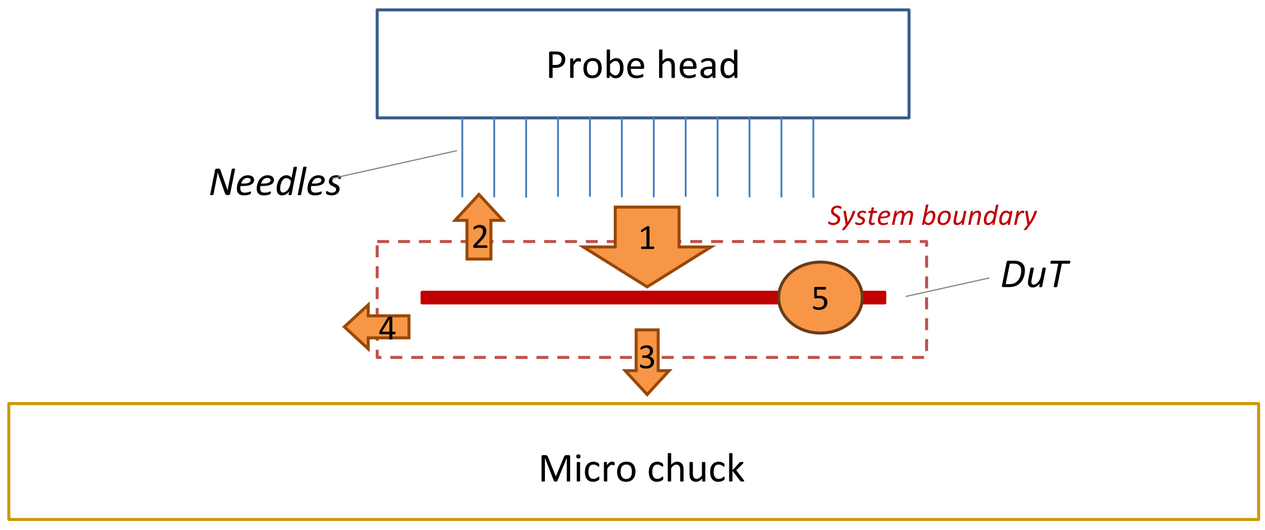
Robust Material to be Tested

Devices showing a **high defect rate** in combination **with catastrophic failure** mode will require **frequent offline maintenance** of the probe cards with corresponding downtimes.

Feasible Test Conditions

High temperature base level in addition with **severe energy deposition** inside the chip during the test will give a high probability of localized thermal runaway for the device und test.

A basic **calorimetric calculation** for the short circuit test indicates that the overall temperature of the device will increase by an additional 100-200°C. In a test that starts at 175°C, it is to be expected that the chip **junction temperatures** (e.g. 300°C) **will be exceeded** with the associated consequences. Customers should be clear about feasible limits regarding test conditions.



Heat flow across system boundary:

- 1: Electric power dissipating inside the device
- 2: Thermal conduction through needles: *<< compared to Electric Power*
- 3: Thermal conduction to micro chuck: *<< compared to Electric Power*
- 4: Thermal convection to ambient air: *<< compared to Electric Power*
- 5: Change in internal energy of device

Conclusion

Results and Performance

Against previous version of T.I.P.S. KGD Micro Contact Systems the maximum pulse current could be increased from 1200A to 3000A. Parasitic inductance of entire test system was reduced from 100nH to 50nH.

Limitations and Outlook

Devices with frequent occurrence of catastrophic chip failures behave destructive especially to vertical probe technology. Cantilever has higher robustness but the disadvantage of lower test currents.
Ongoing research activities give us confidence that maximum test current can be further increased.

Contact

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