SWTEST

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2024 CONFERENCE

# Singulated Die Sort as a tool to enable high precision thermal control during high-volume manufacturing


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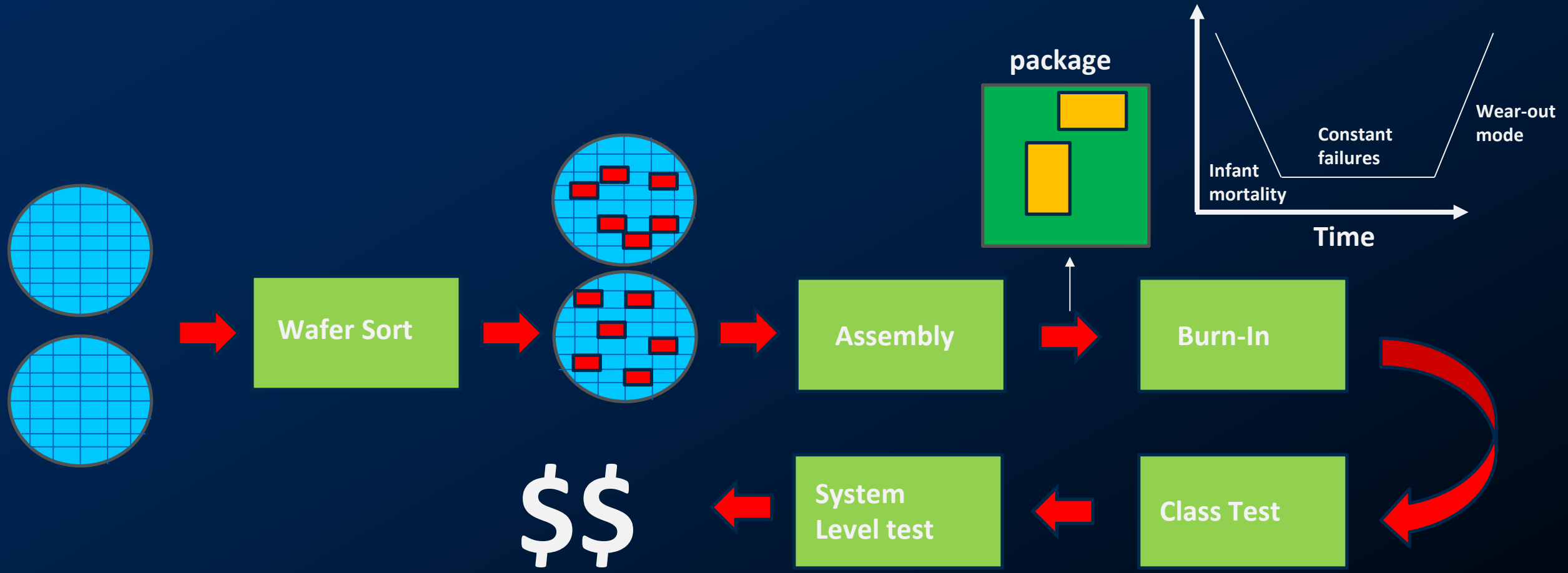
# Outline

- Overview of a High-Volume Manufacturing (HVM) test flow
- Wafer Sort: a thermal perspective
- HVM flow with Known Good Die
- Singulated Die Sort (SDX): a thermal perspective
- Thermal management
- Thermal performance comparisons: wafer sort vs. SDX
- Summary

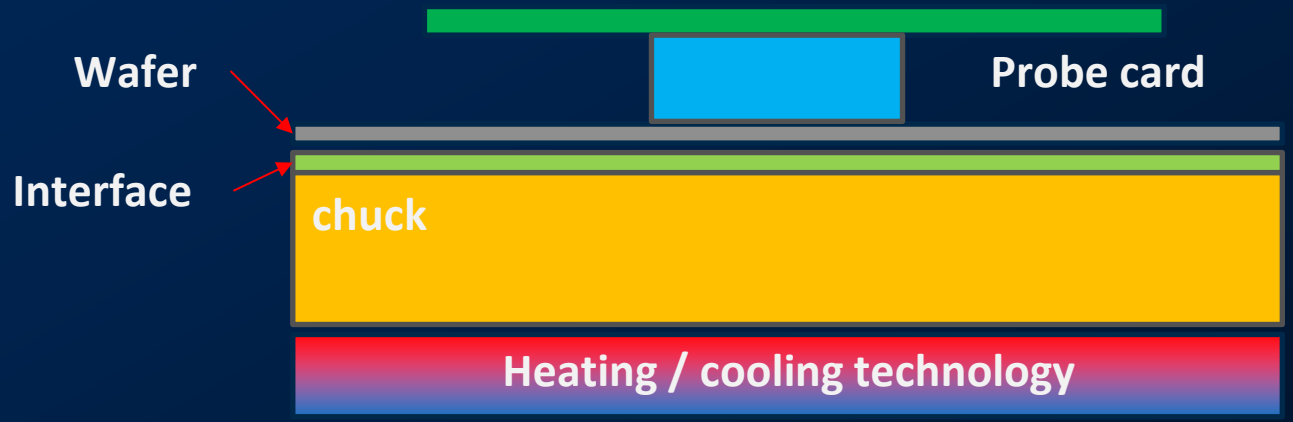
# Overview of a HVM Test Flow



# Wafer Sort: a thermal perspective

- A tool to maintain the wafer at a constant temperature while some tests are performed

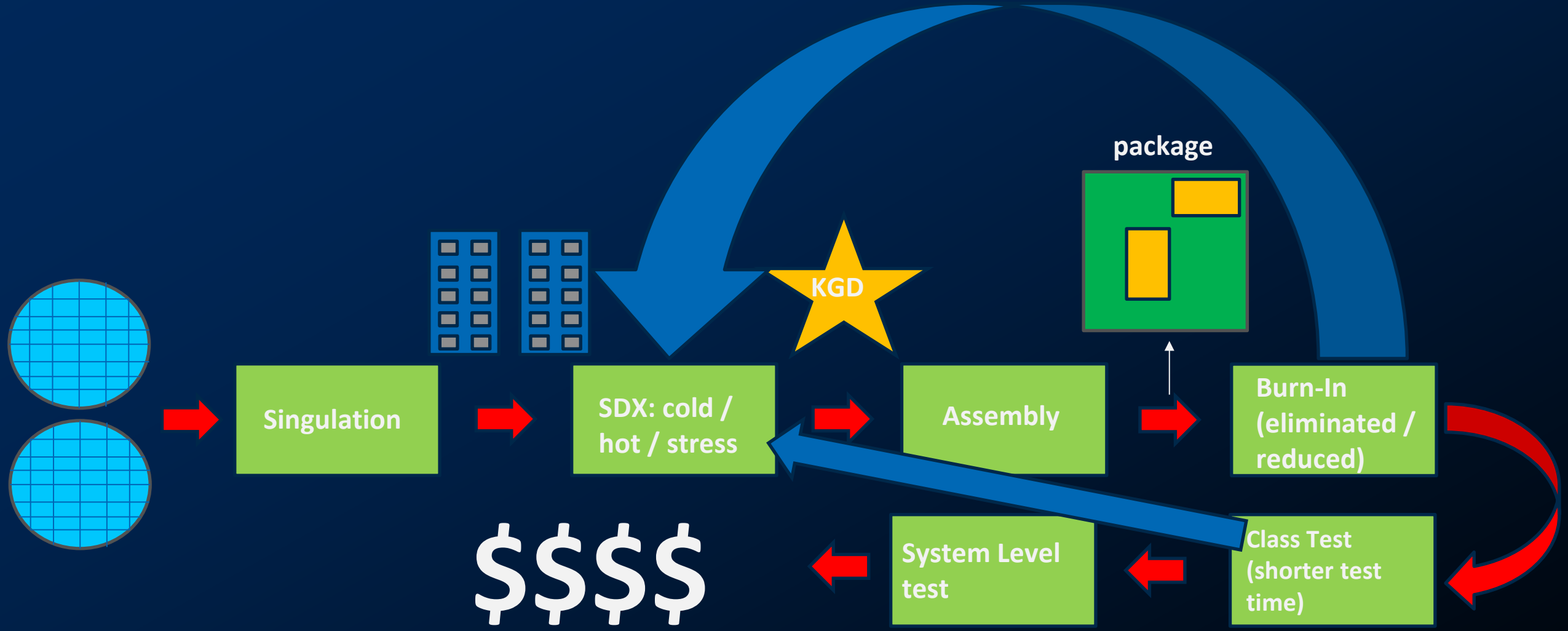
**Schematic of a typical wafer prober, not drawn to scale**




**Thermal considerations:**

1. **Mass:**
   - The chuck diameter needs to match the wafer
   - To maintain low gradient, high thermal conductivity materials are needed
   - High thermal conductivity materials also have high density → the mass of the chuck is large.
2. **Interface:**
   - A thermal interface is formed between the wafer and the top of the chuck
   - The contact resistance is a function of the pressure and the surface quality
   - Assuming a dry contact interface with relatively low pressure, the contact resistance is high.

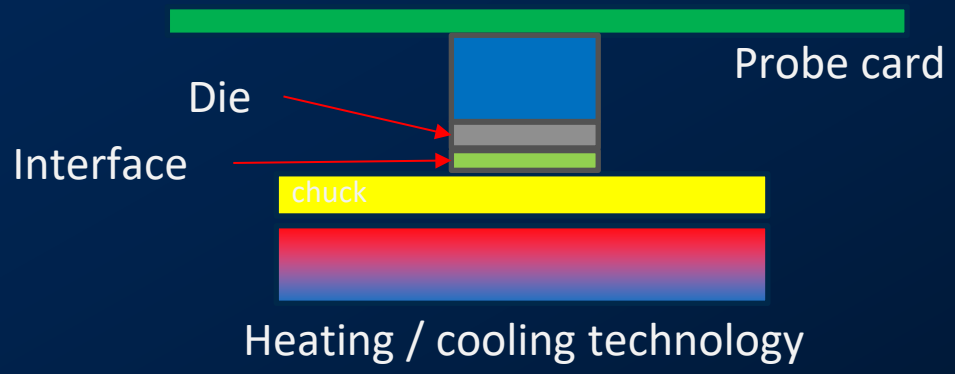
# HVM flow with Known Good Die



# SDX: a thermal perspective

- A tool to control the temperature of a single die during test with very high precision

**Schematic of SDX chuck, not drawn to scale**



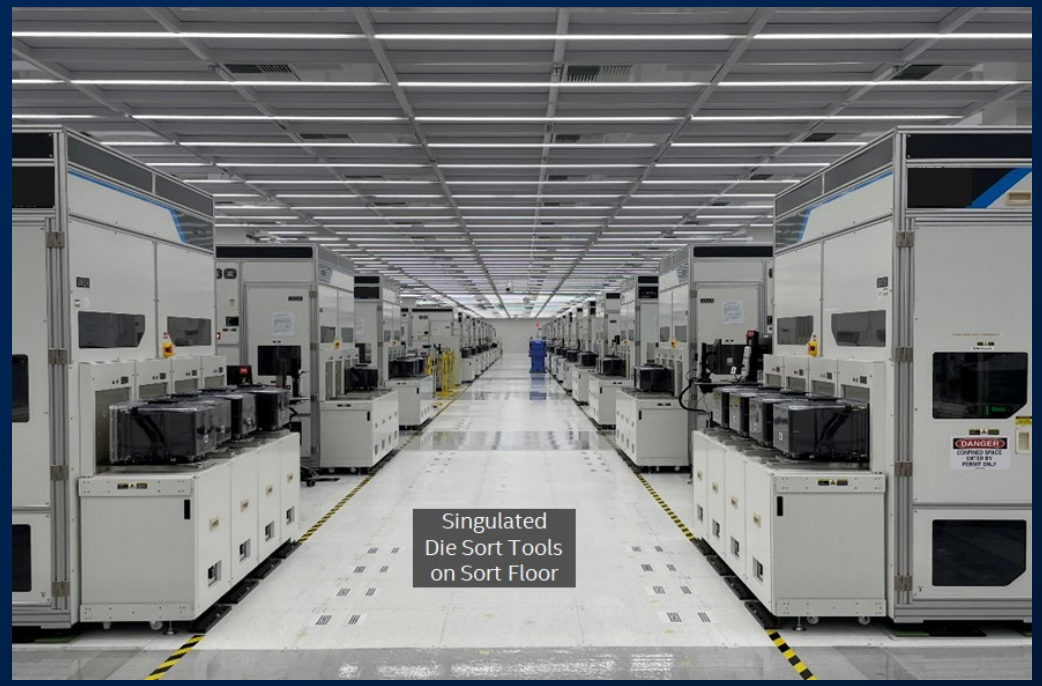

**Thermal considerations:**

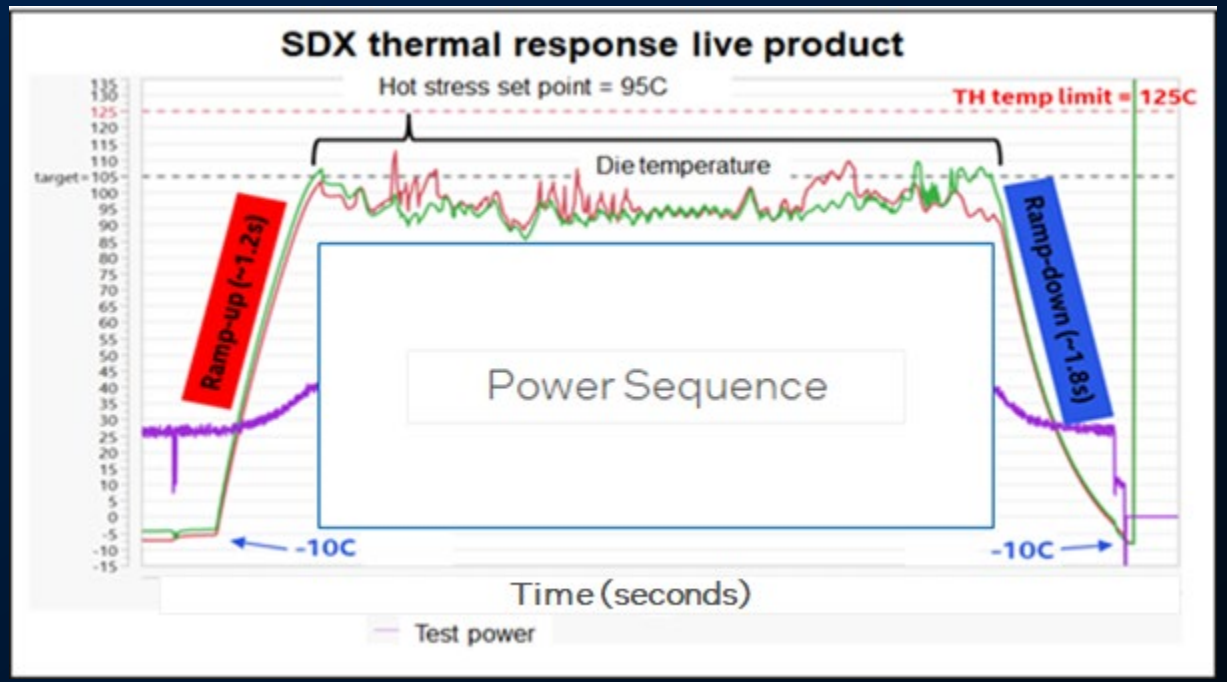
1. Mass:
   - The chuck dimensions defined to support up to a full reticle die
   - Need materials with high stiffness and thermal conductivity
   - Due to dimensions of the chuck and material options → the mass of the chuck is very small.
2. Interface:
   - A thermal interface is formed between the die and the top of the chuck
   - The contact resistance is a function of the pressure and the surface quality
   - Using of a gas and high contact pressure, the contact resistance is very low.

| Parameter | Improvement of SDX over wafer sort |
|---|---|
| Interface resistance | 10X |
| Heating rate | 1785X |
| Cooling rate | 150X |

# The benefits of speed

- SDX enables multiple set points for the same insertion: cold / hot / cold for maximum test coverage



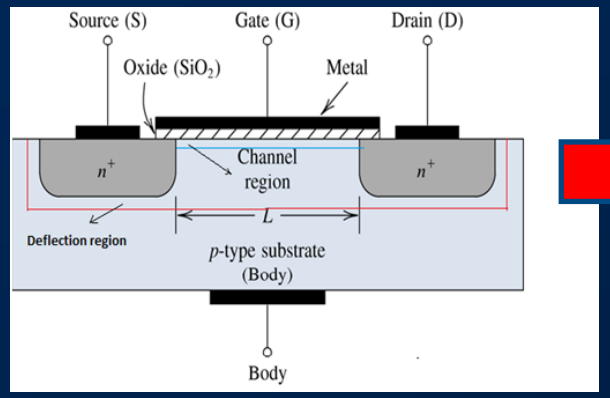




**SDX offers a unique advantage over wafer Sort equipment for test coverage in the same insertion**

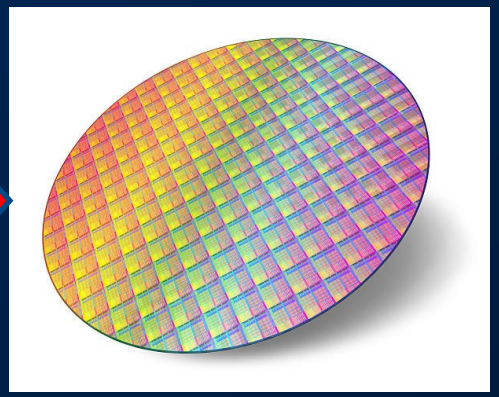
# Thermal Management: heat in electronics

- The flow of current inside a transistor dissipates energy as heat

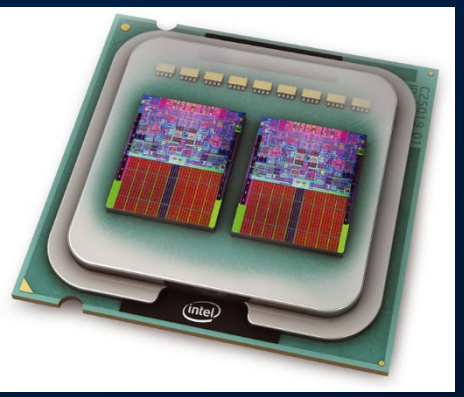
**Single transistor**



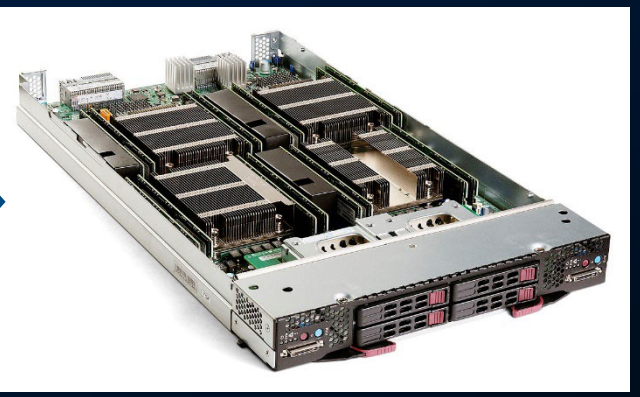

**Fabricated in a wafer**



**Diced and Packaged**



**Mounted on a board**

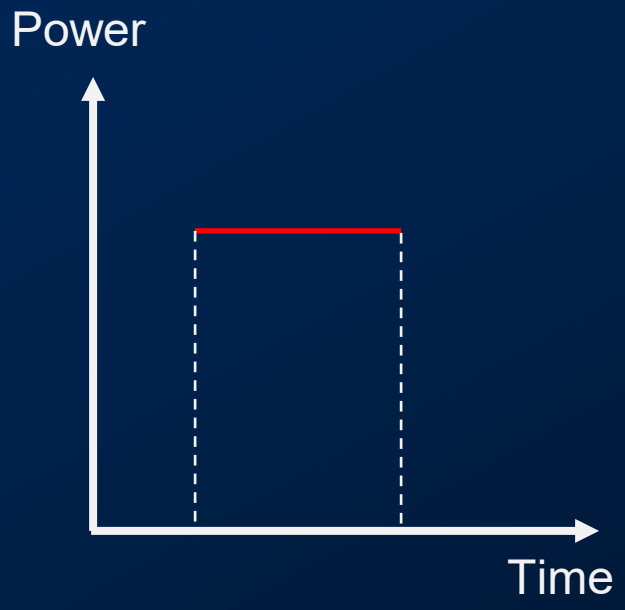


$$\text{Power} = \text{Voltage}^2 * \text{Capacitance} * \text{Frequency} + \text{Leakage}(T)$$

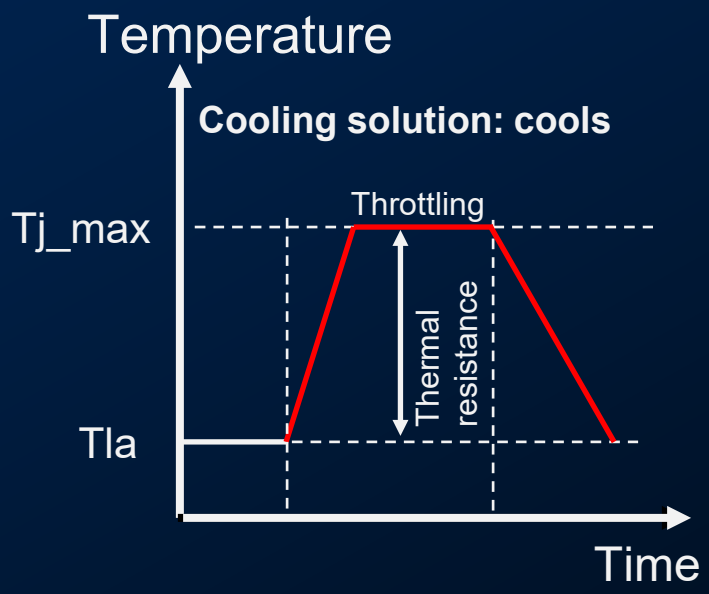
Process and die dependent

# Thermal Management: cooling vs. controlling

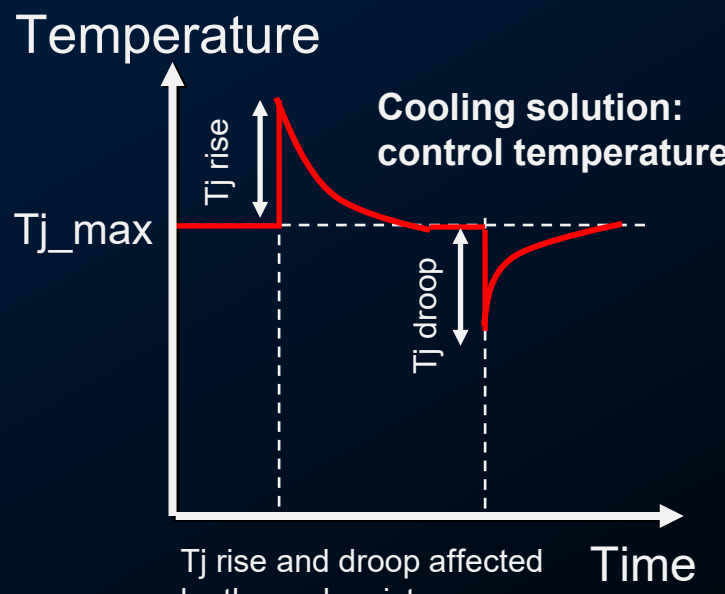
- A platform cooling solution cools the package
- A test thermal solution controls the temperature to a set point




**Platform thermals**



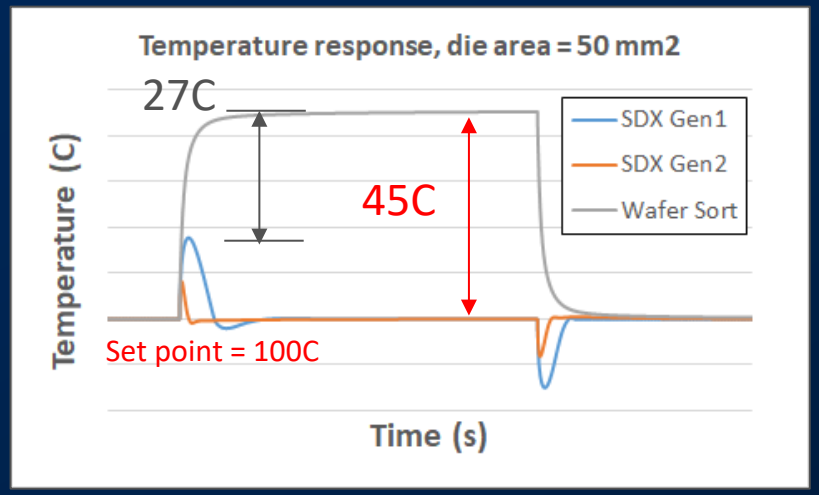

**Test thermals**

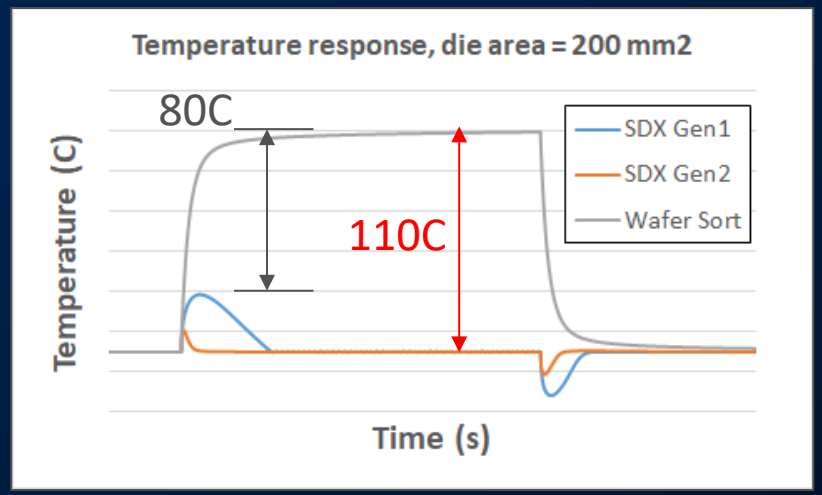


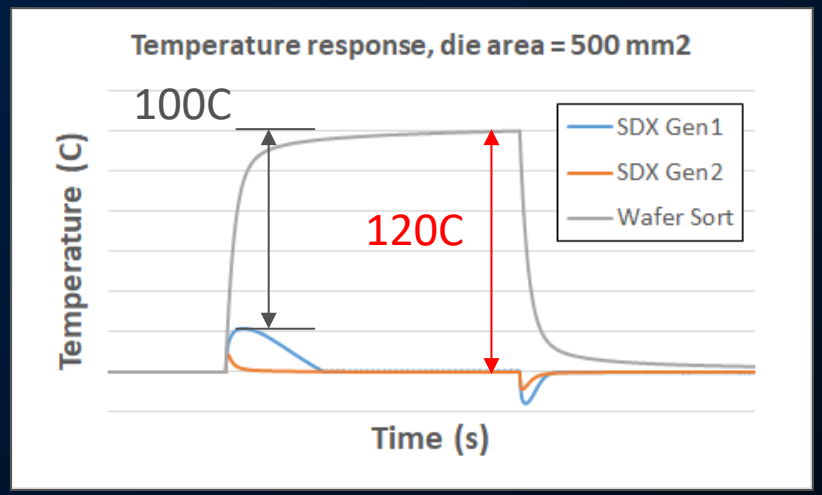

Tj rise and droop affected by thermal resistance, mass and controller

# Thermal comparisons: wafer Sort vs. SDX

- Thermal response comparison to a single power pulse; effect of die size



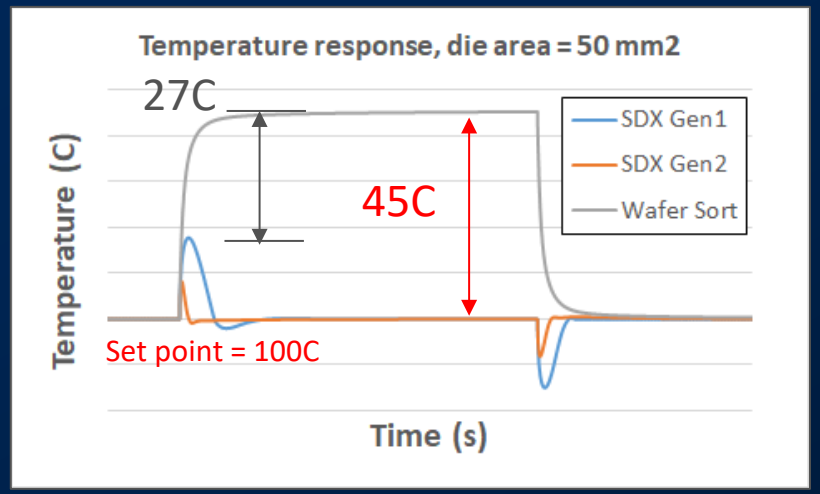



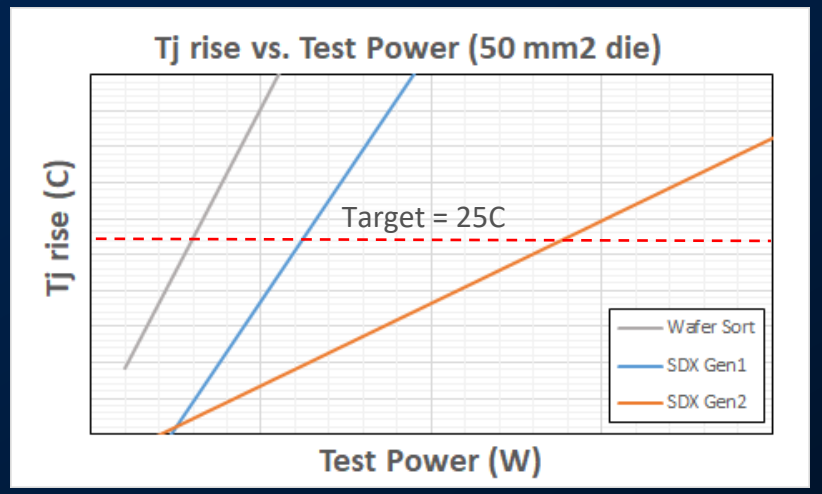

***Wafer Sort is considered as x1 parallelism***
***SDX Gen2 under development; to be ready by H2'26***

**Under the same test conditions, only SDX can maintain the temperature of the die under test at the set point**

# Thermal comparisons: wafer Sort vs. SDX

- SDX Gen 2 performance: new materials, improved design, extreme thermal response!




***Wafer Sort is considered as x1 parallelism***
***SDX Gen2 under development; to be ready by H2'26***

**Relative power improvement in SDX compared to wafer Sort for Tj rise target of 25C: 50 mm² die**

| Tool | Power (W) |
|---|---|
| SDX Gen 1 | 2X |
| SDX Gen 2 | 5X |

**Relative power improvement in SDX compared to wafer Sort for Tj rise target of 25C: 400 mm² die**

| Tool | Power (W) |
|---|---|
| SDX Gen 1 | 4X |
| SDX Gen 2 | 14X |

**SDX enables tighter thermal control and higher power: more aggressive test content for better coverage**

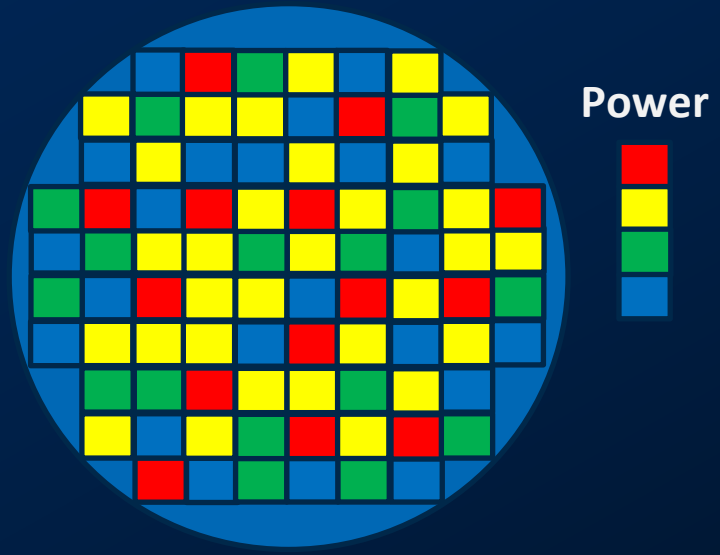
# Thermal comparisons: wafer Sort vs. SDX

- The impact of die-to-die variation on temperature response

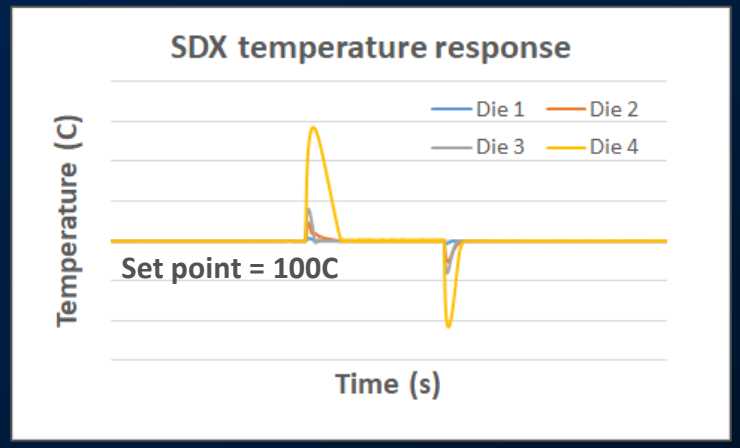
$$\text{Power} = \text{Voltage}^2 * \text{Capacitance} * \text{Frequency} + \text{Leakage}(T)$$

Process and die dependent

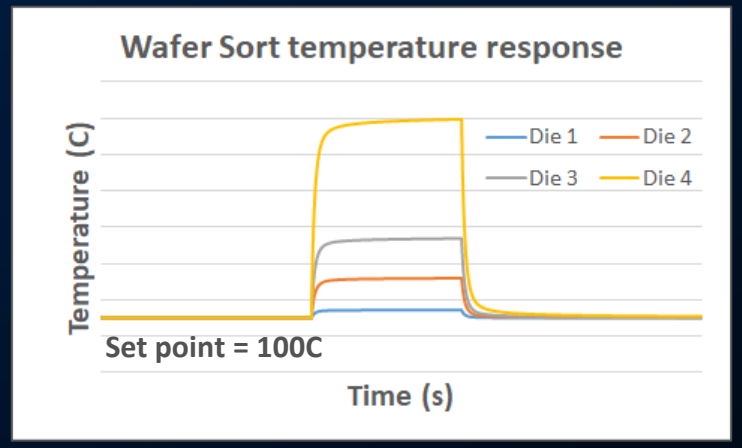
**Hypothetical wafer showing peak test power per die for the same test content**




**Power pulses applied to 4 different die; die area = 200 mm²**




Die temperature range: 27C




Die temperature range: 105C

**Even though the same test content is run on each die, the natural variation can result in significantly different power levels; SDX can easily compensate for this**

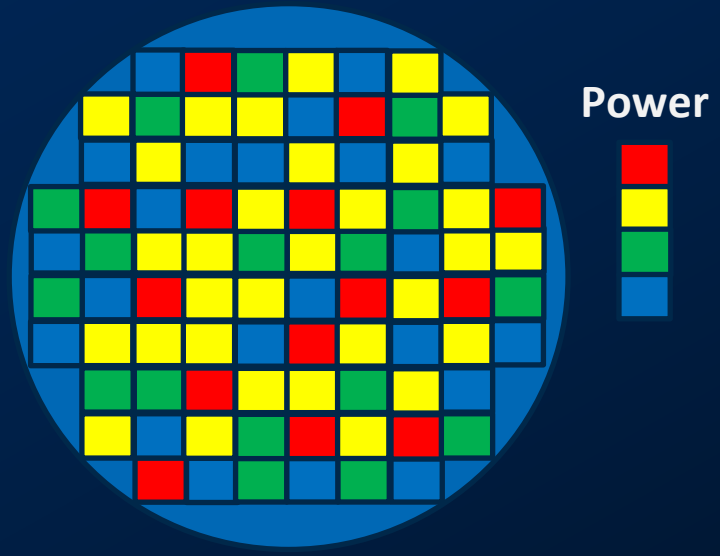
# Thermal comparisons: wafer Sort vs. SDX

- The impact of die-to-die variation on test set point

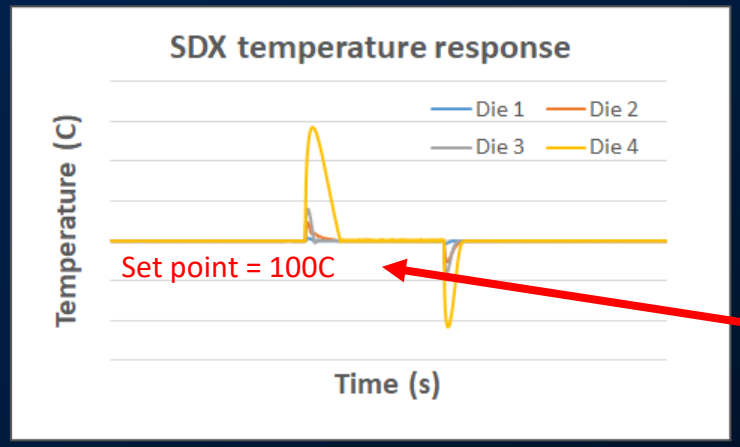
$$\text{Power} = \text{Voltage}^2 * \text{Capacitance} * \text{Frequency} + \text{Leakage}(T)$$

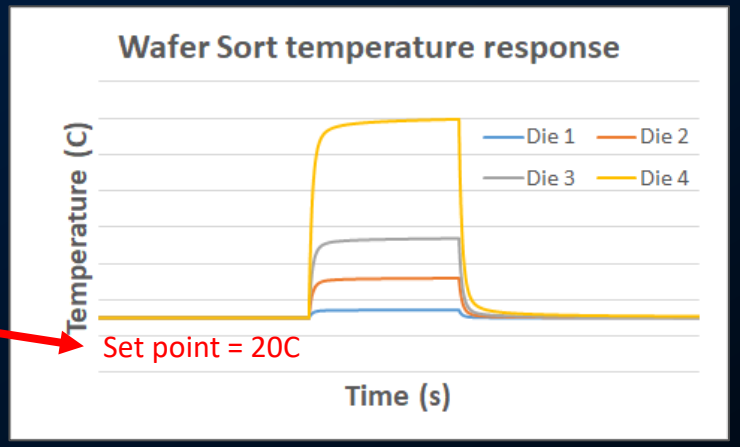
Process and die dependent

**Hypothetical wafer showing peak test power per die for the same test content**




**Power pulses applied to 4 different die; die area = 200 mm²**




**Because wafer Sort is very slow, its set point must be determined based on the highest power die; in this example, the wafer Sort chuck needs to be set 80C cooler than SDX → limits the ability of the tool to screen defects effectively**

# Summary

- SDX uses and extremely fast thermal solution that is capable of very high precision thermal control during test at Sort, that enables multiple set points for the same insertion.

- Tighter temperature control:
  - Enables precise execution of test content at the desired target set point critical for temperature-dependent content.
  - Minimizes variation in test results induced by the natural die-to-die variation.

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