SWTEST

PROBE TODAY, FOR TOMORROW

2024 CONFERENCE

Spike Safe Floating VI Design & Associated FET Testing Methods

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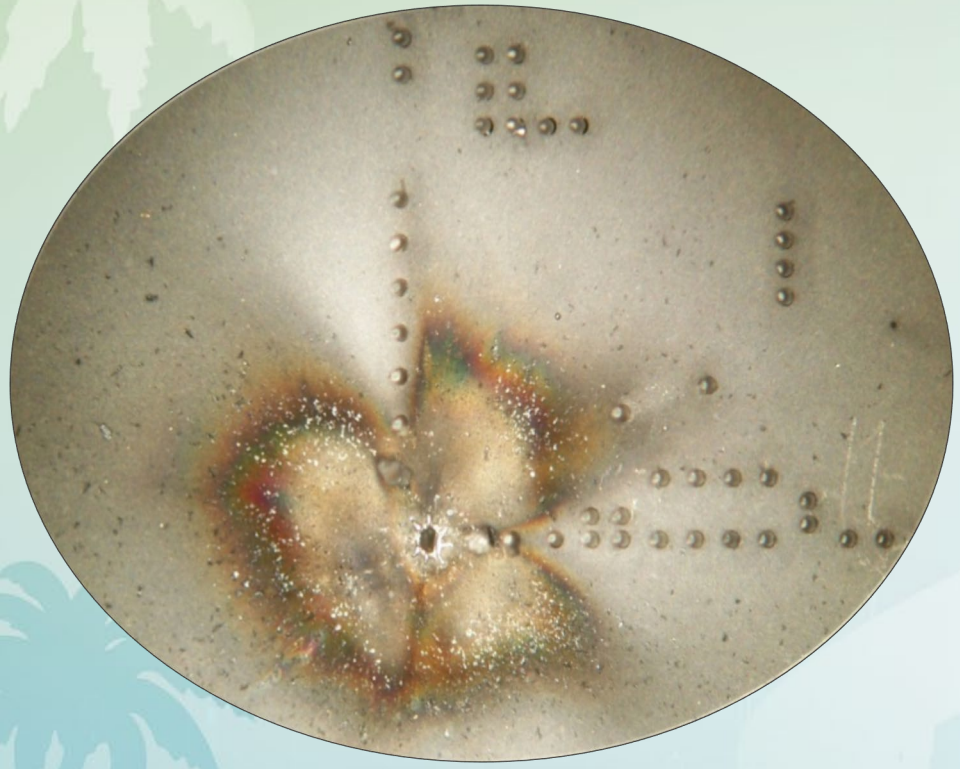
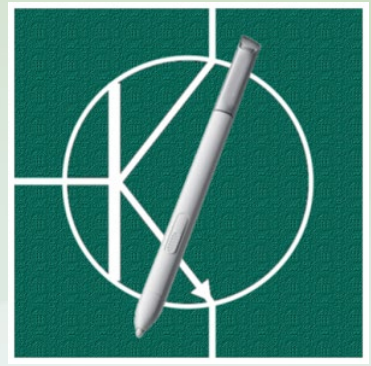
Test & Measurement Systems

How to prevent pretty (but destructive) floral patterns on probe cards (that cost more every day)?

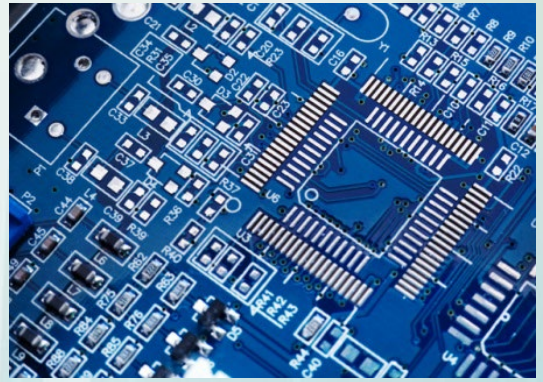


Introduction & Problem Statement

Proposed Design
& Test Methods

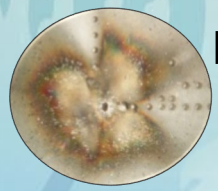


Benefits &
On Board Use



What is a floating VI?

- A Source / Measure Instrument (also often called a VI) that can be used with its 'Low Side' at any voltage relative to the tester GND
  - Use is often limited by 'isolation' breakdown of the instrument
  - Allows multiples to be 'stacked'
  - Can also be used with a GND reference



GND Referenced VI

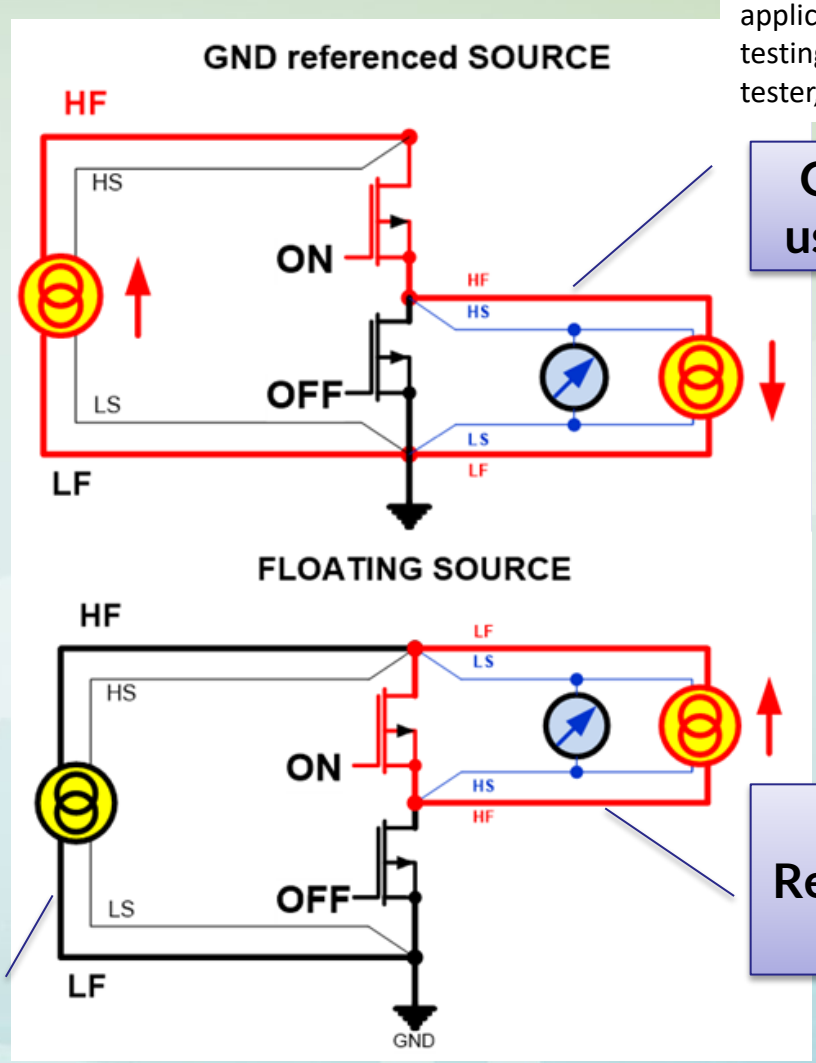


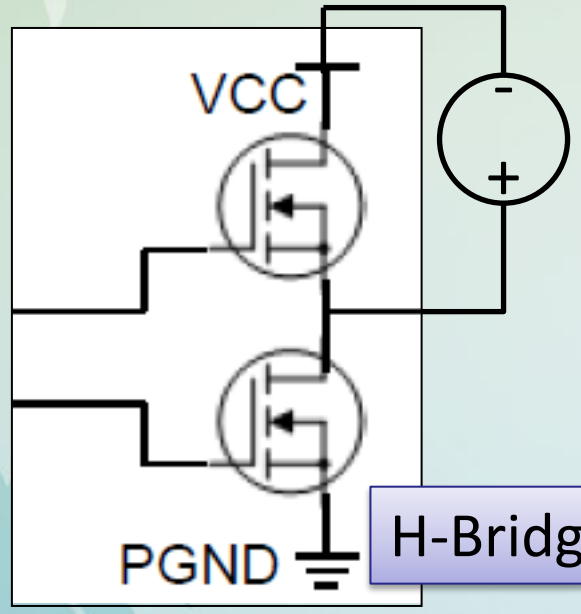
Image from : K. Liu and J. Fan, "Challenging solution design and application for automotive electronic testing on the Advantest V93000 tester," in TestConX China, 2022.

GND Referenced use of a floating VI

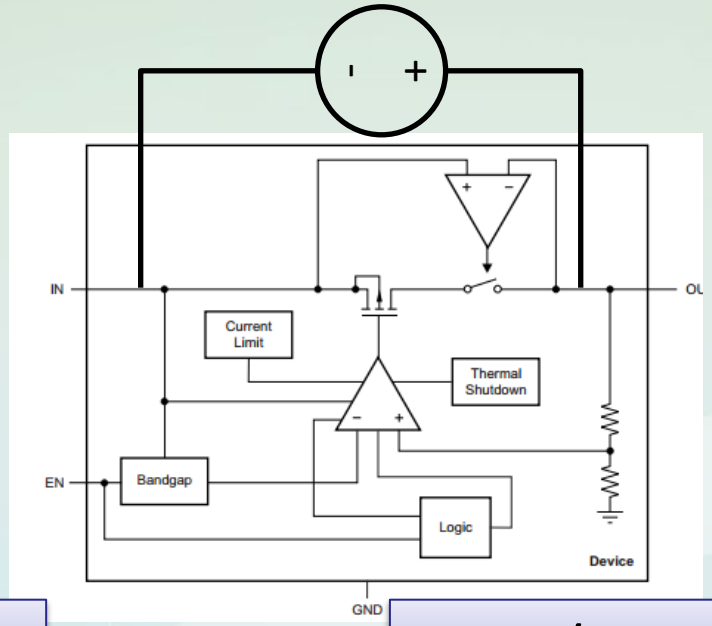
High Voltage Referenced use of a floating VI

Where are these used?

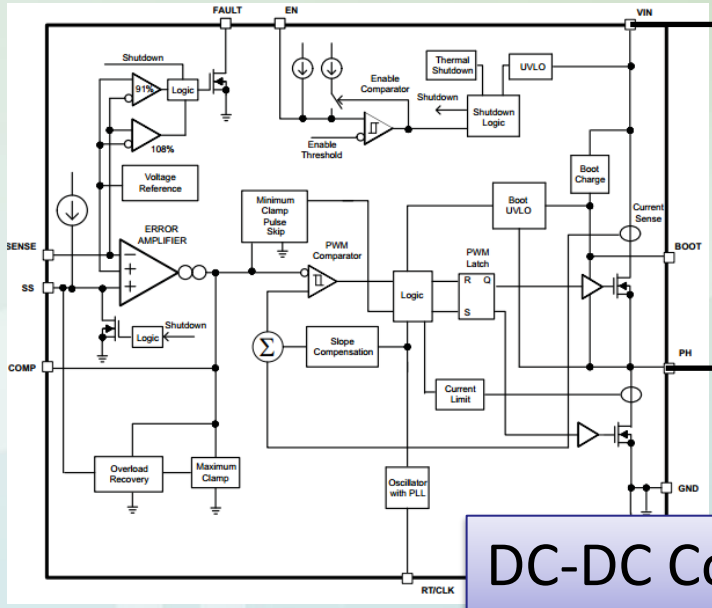
Testing for...



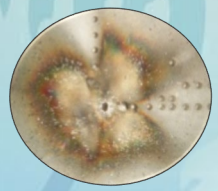
H-Bridges



LDOs / BMS



DC-DC Convertors



...and anywhere else an instrument referenced to a variable potential is needed

Existing VIs can be challenging to put to use

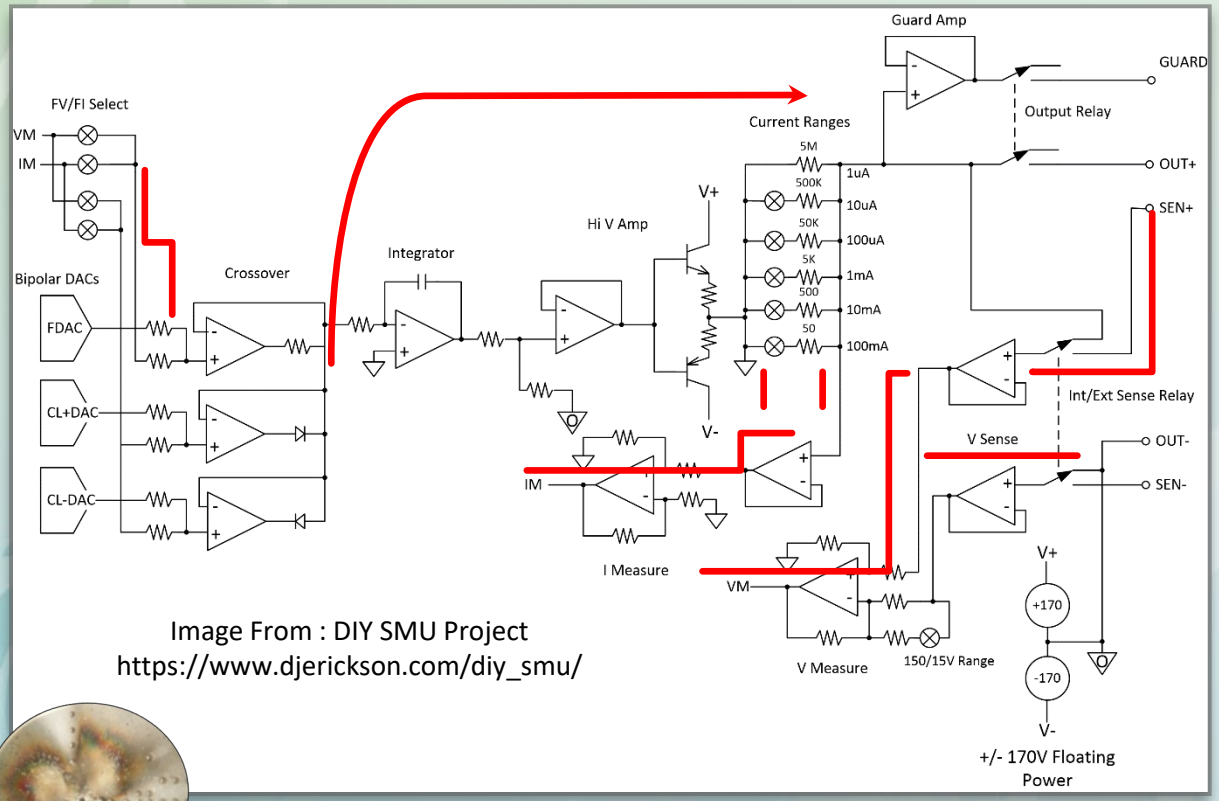
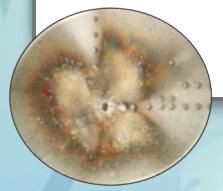
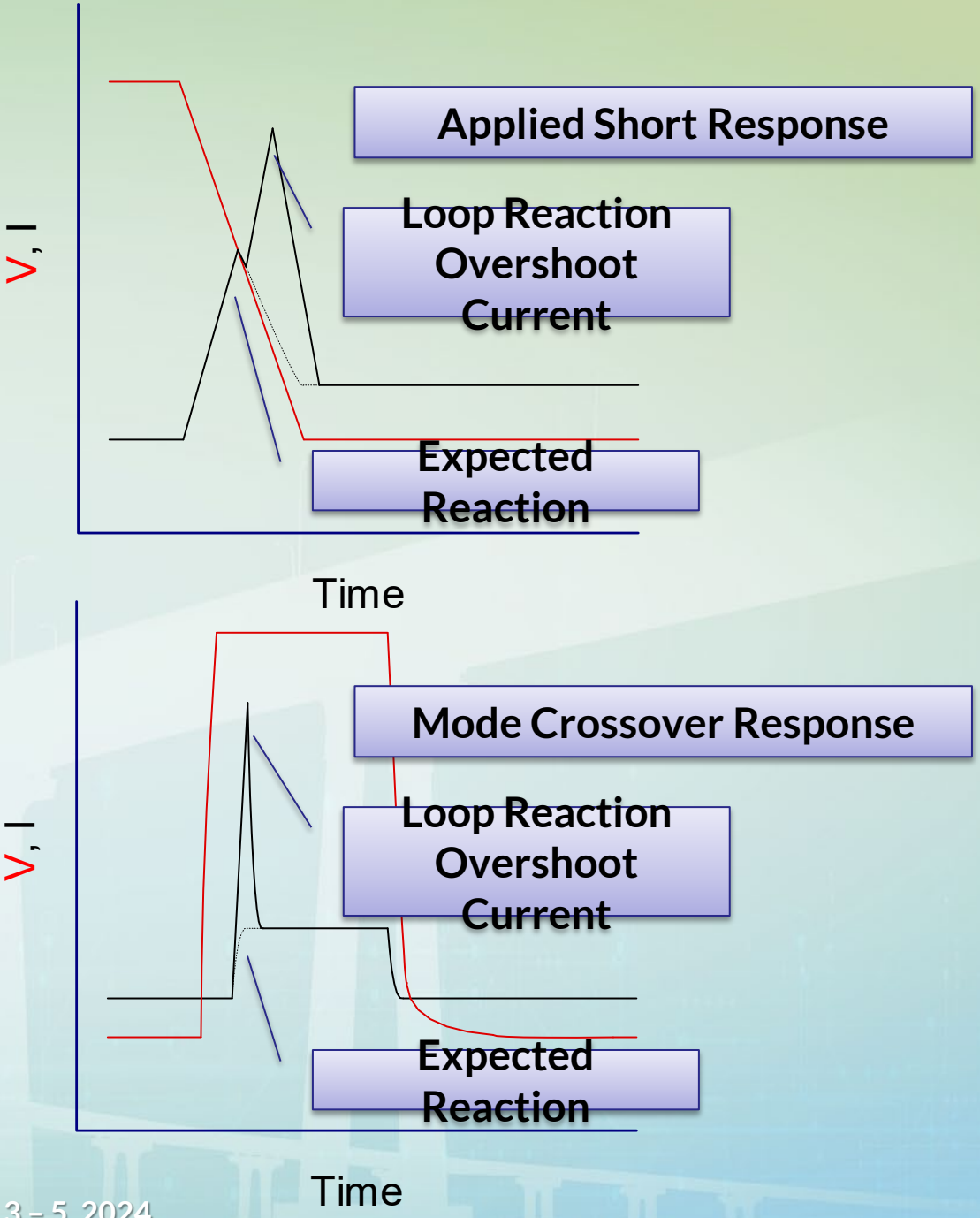


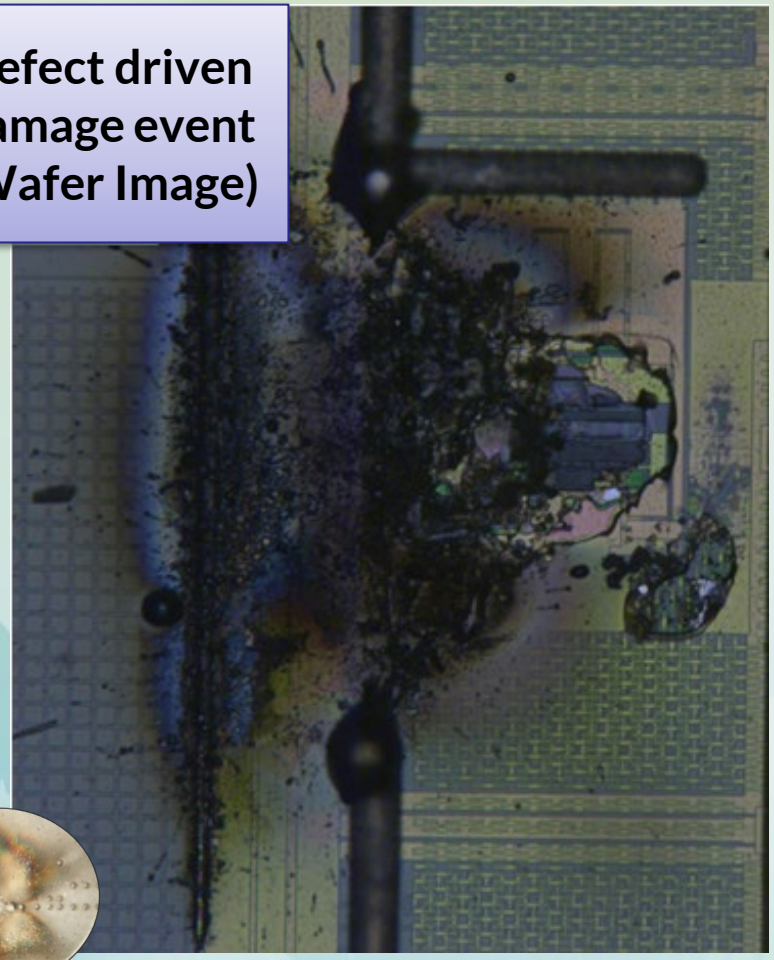
Image From : DIY SMU Project
https://www.djerickson.com/diy_smu/

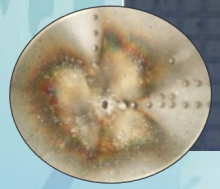


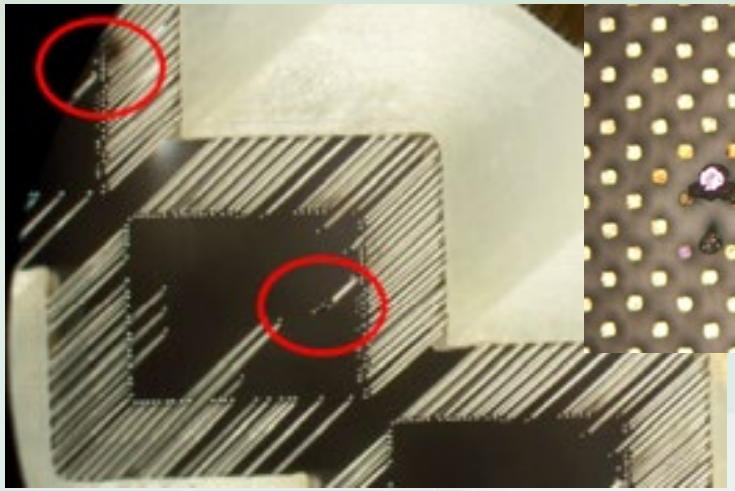


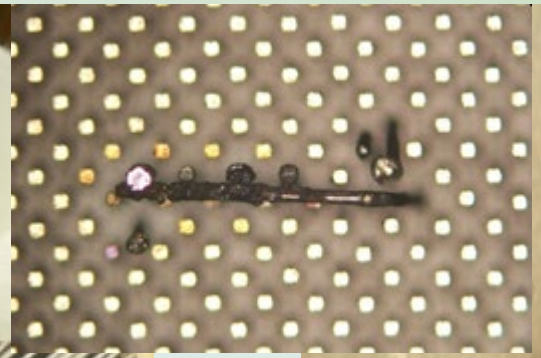
High power events get worse and typically exceed design capability when bad devices get tested

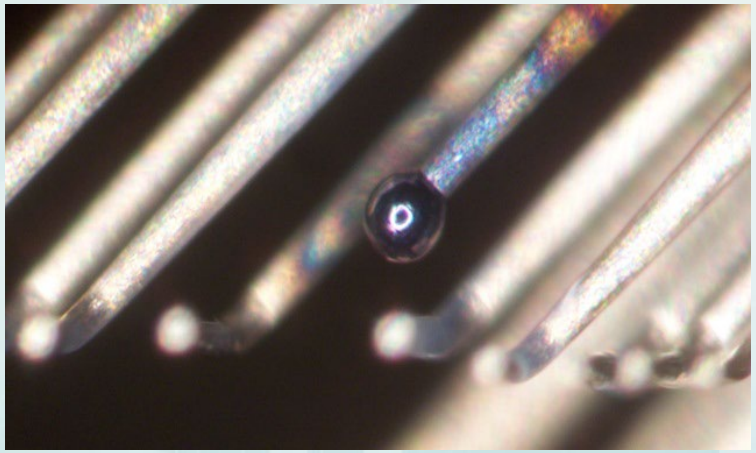
Defect driven damage event (Wafer Image)



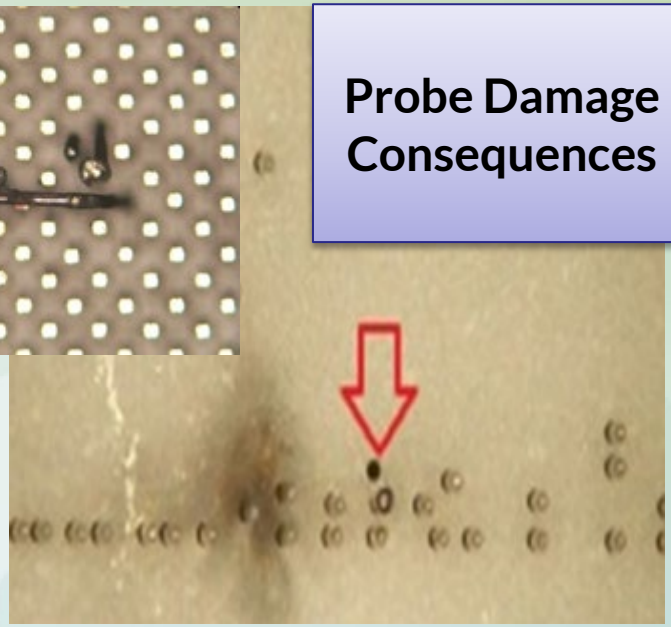






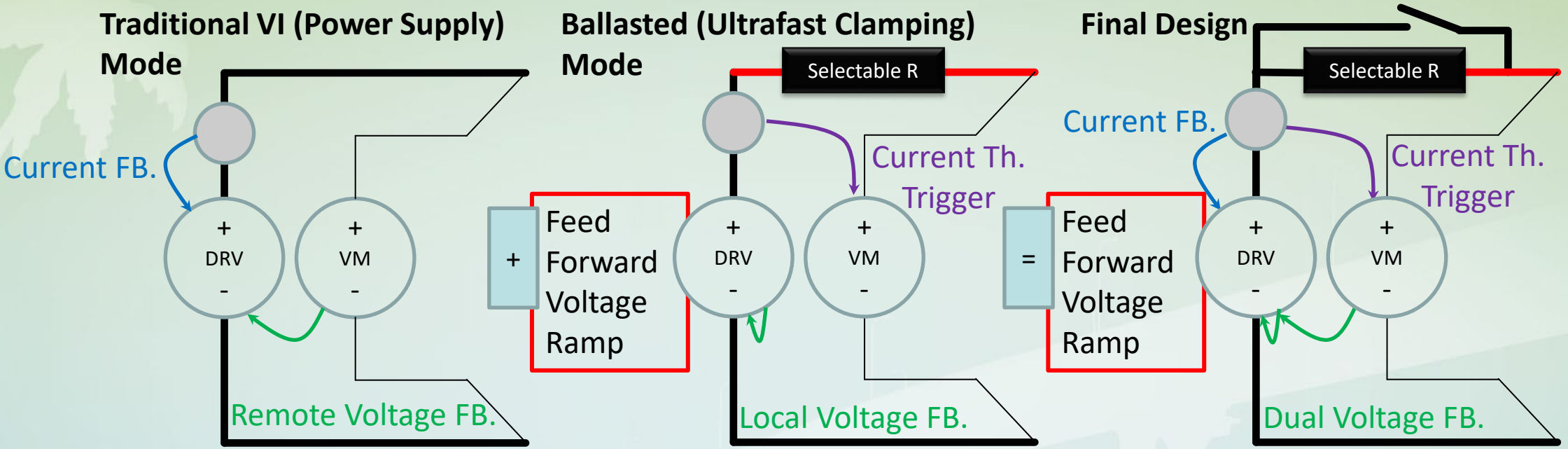


Probe Damage Consequences



Single events often cause expensive equipment to be severely damaged

Alleviating EOS conditions with a Ballasted Mode

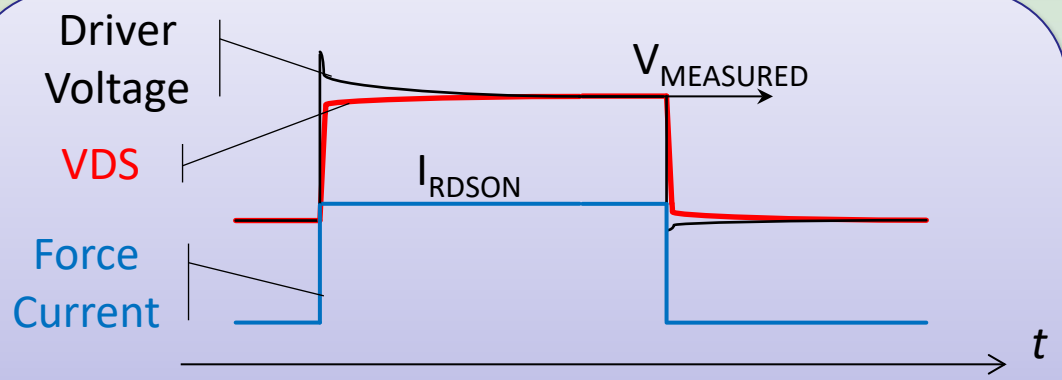


Driver – Closed Loop Normal VI Operation
Voltmeter ADC – Used closed loop – Same range as driver
Ammeter ADC – Use closed loop – Same Range as driver

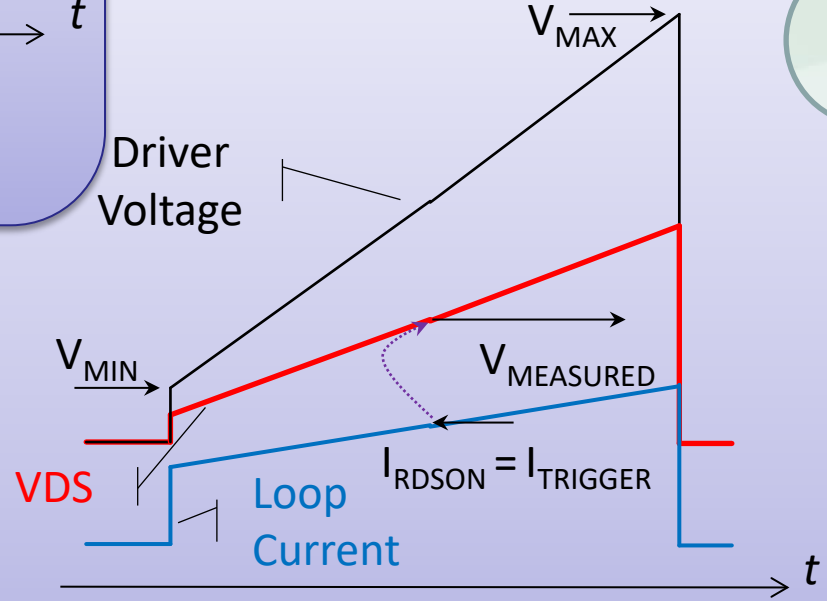
Driver – Force Line only with selectable series R
Voltmeter ADC – Used with high gain as precise VM
Ammeter ADC – Preset Threshold Trigger – Metering / Digitizing – Same range as driver

= Ammeter
= Driver
= Voltmeter

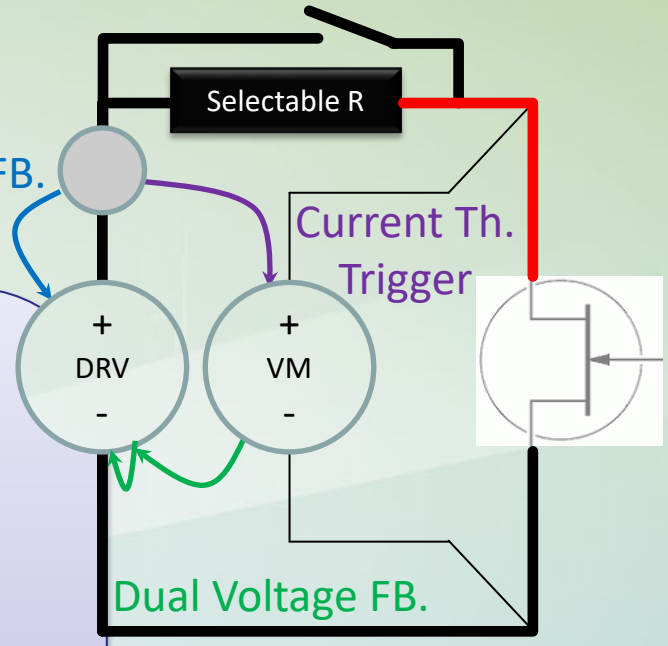
Implementing the tests..
rDS-On



Traditional rDS-On
Power Spikes & 2 Mode Changes



Ballasted rDS-On
Spike Free & No Mode Changes

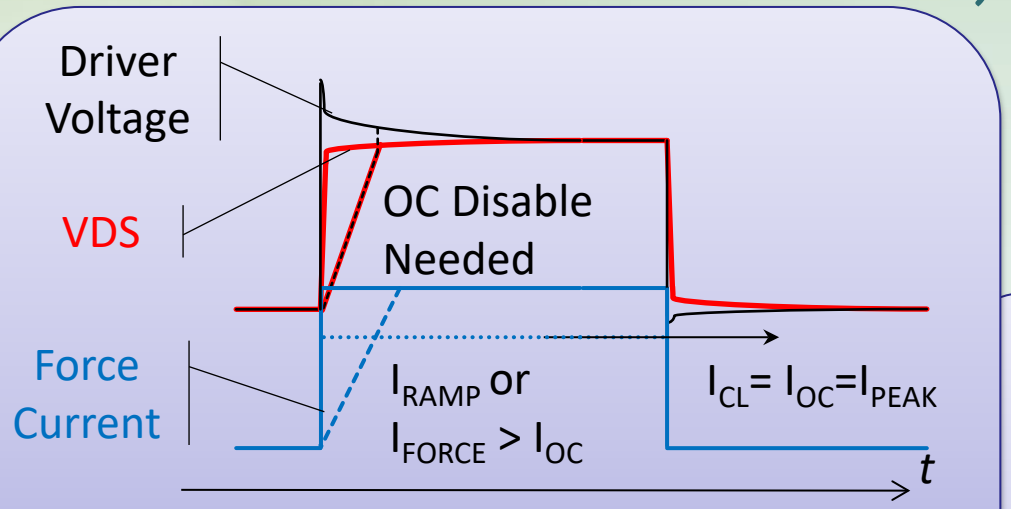


= Ammeter

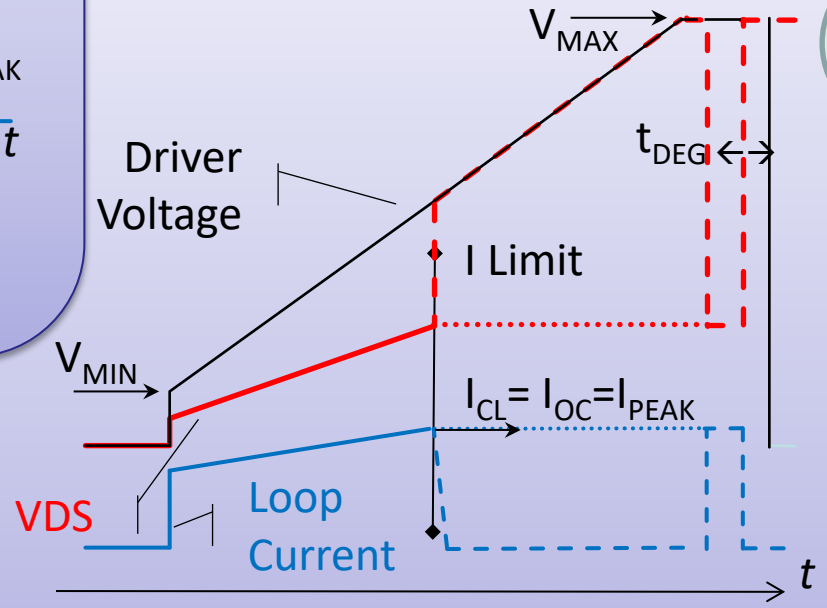
= Driver

= Voltmeter

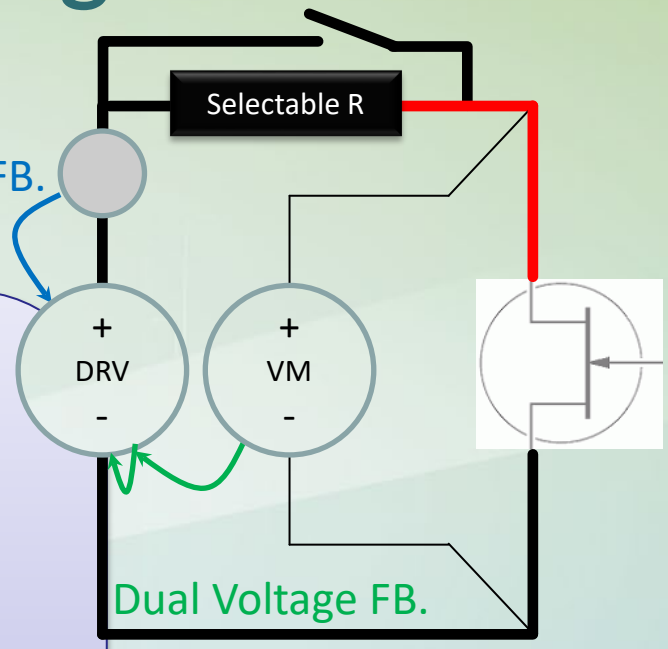
Implementing the tests..
Current Limit, Overcurrent & Deglitch



Traditional OC / CL etc.
Power Spikes & Multiple Mode Changes



Ballasted OC, CL & Deglitch
Spike Free & No Mode Changes

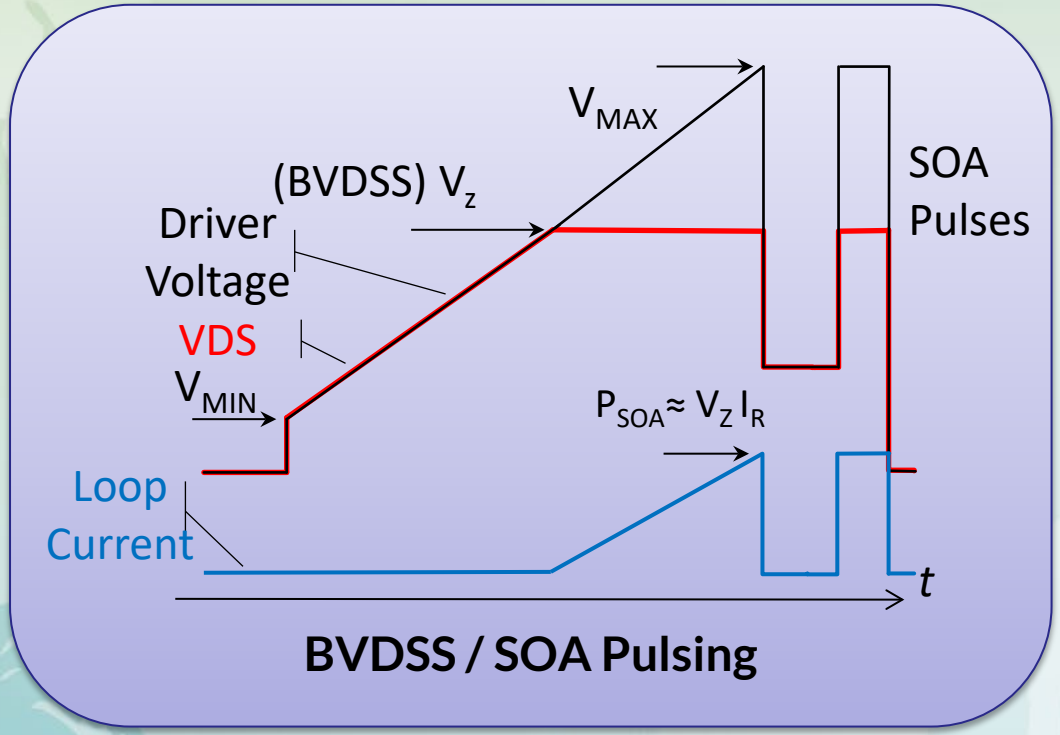


= Ammeter

= Driver

= Voltmeter

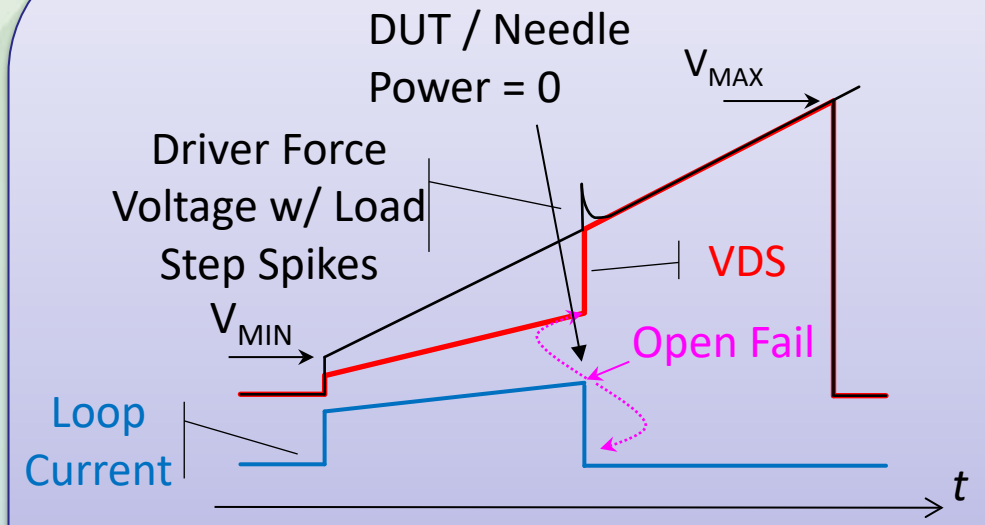
Implementing the tests.. BVDSS, SOA (Valve FETs) & the integrated approach



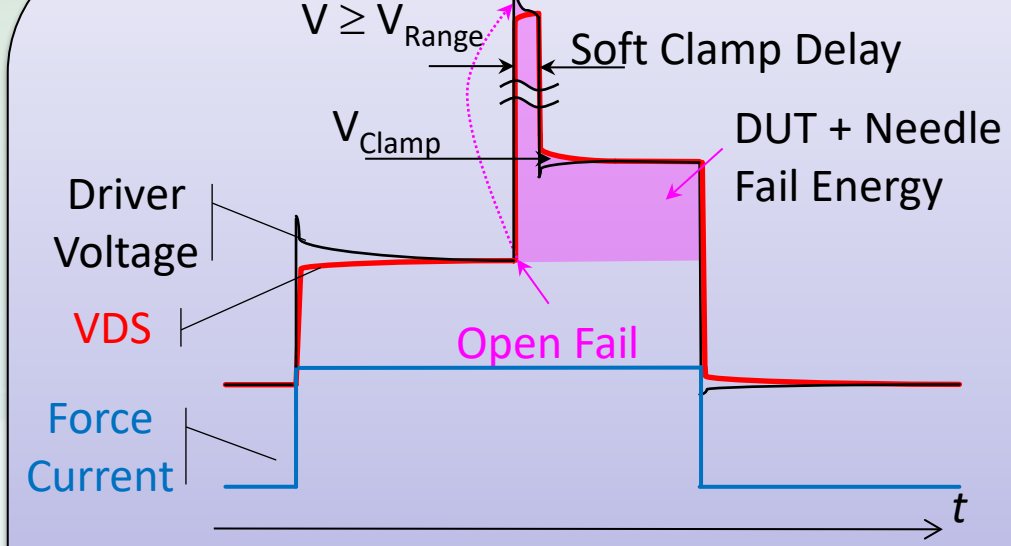
BVDSS / SOA Pulsing

- Most mixed signal ATEs allow for device & instrument commands to be interlaced well with pattern based control
- All tests that use the high power floating VI can now be integrated into one force voltage (no force I needed) sequence, with the DUT/FET state controlled by communication (or gate control) without spikes or crossovers
- Native VI capabilities can also be retained

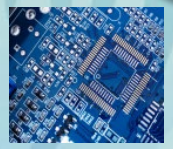
High power slow response conditions are eliminated, even in failure modes



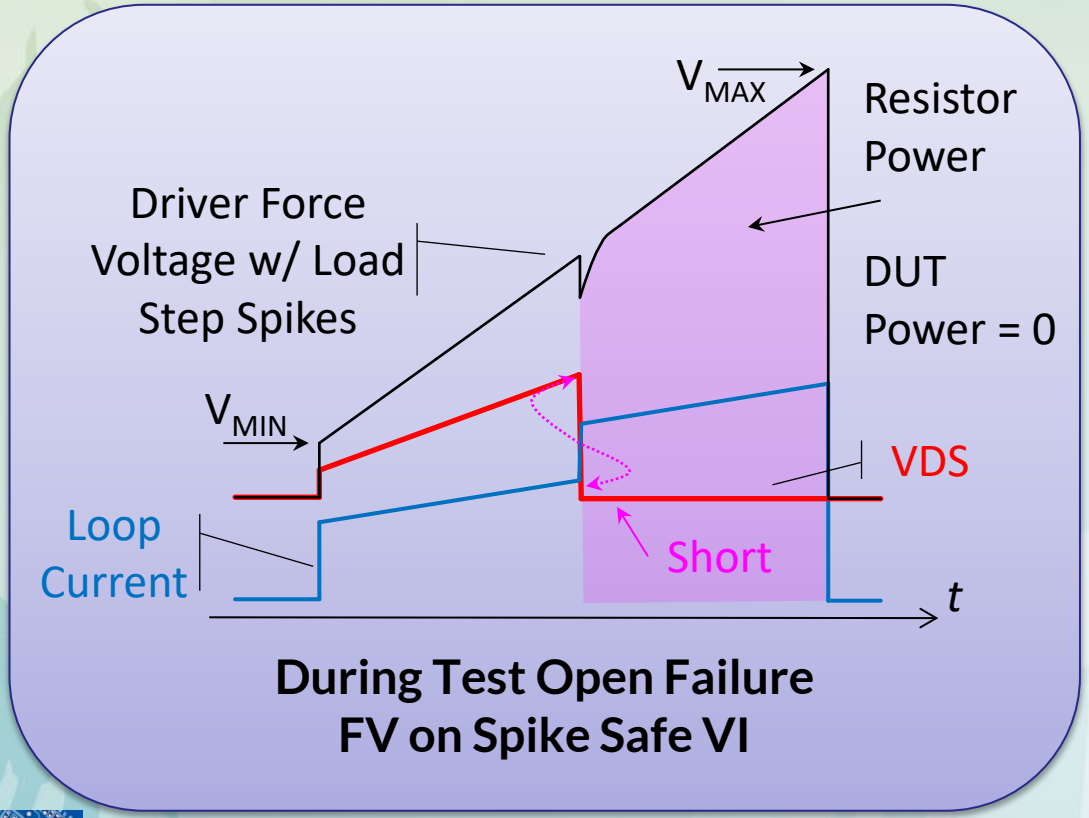
During Test Open Failure
FV on Spike Safe VI



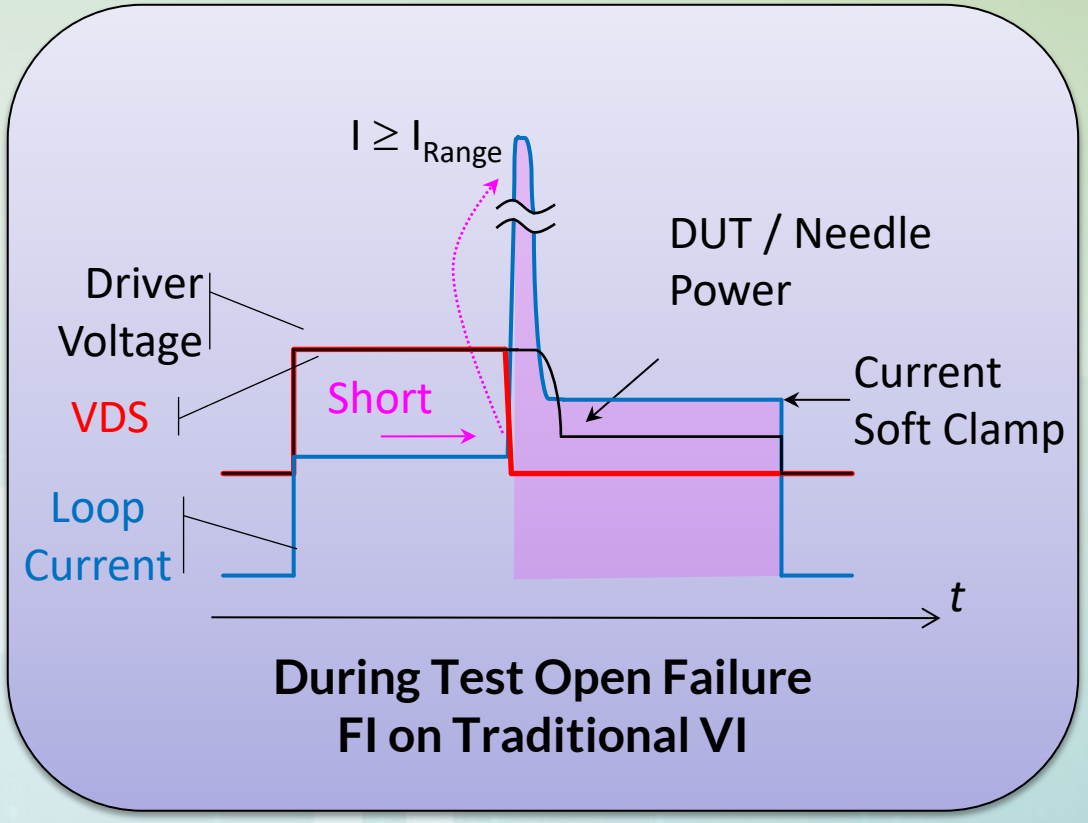
During Test Open Failure
FI on Traditional VI



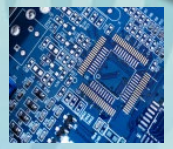
..and the resistor instantly starts dissipating power in case of a short.



During Test Open Failure
FV on Spike Safe VI



During Test Open Failure
FI on Traditional VI

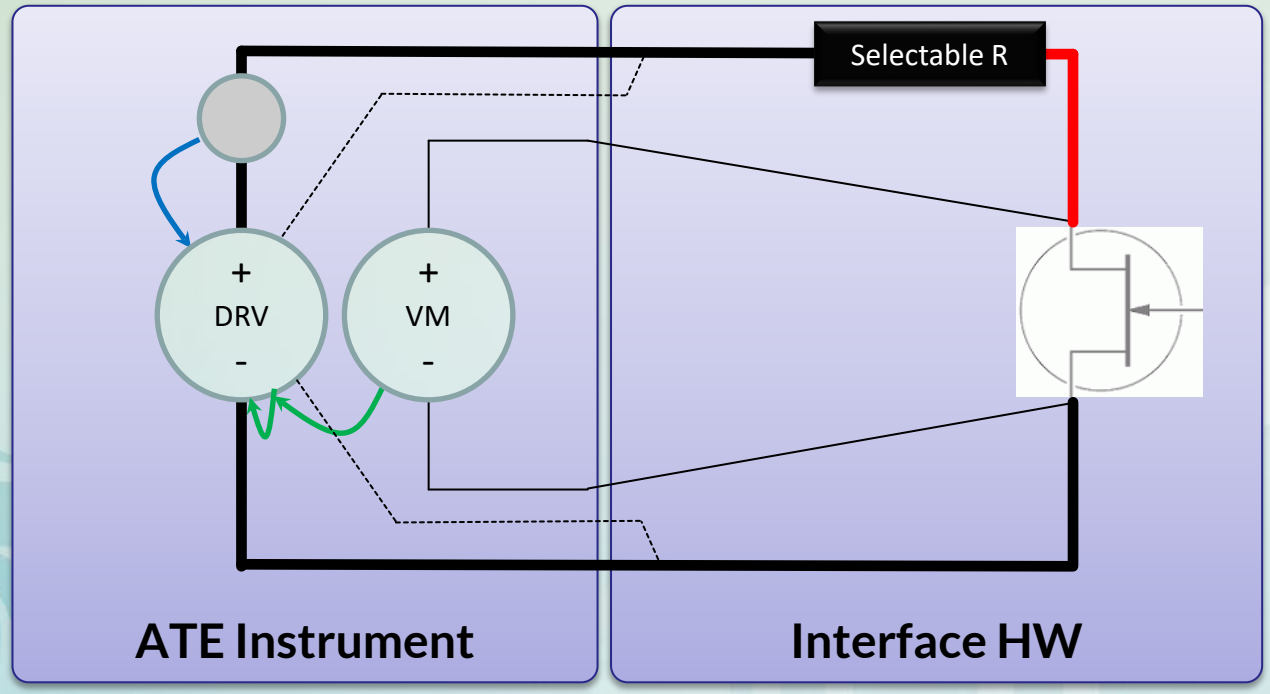


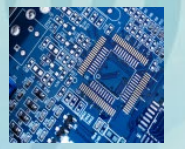
Design constraints

- Accuracy or calibration of the resistor is not needed
  - The design allows all V & I measurements to be independent of the value of the ballast, as long as the range corner conditions are met
  - Ballast value selection is intended to establish operating ranges for the DUT i.e. a 1A LDO Pass FET rDS-On Test would have an R value different from a 10A Valve FET SOA Test
- Power considerations
  - Worst case power in the path is now much lower & deterministic (good for probe card / hardware design margins)
  - Resistor is energized on a low duty cycle and can be sized accordingly.
- Resistor Selection

A choice of values is needed for in-instrument design, to suit diverse power & voltage ranges of use.

The design can be implemented on existing ATEs





= Ammeter + DRV - = Driver + VM - = Voltmeter

ATE Implementations

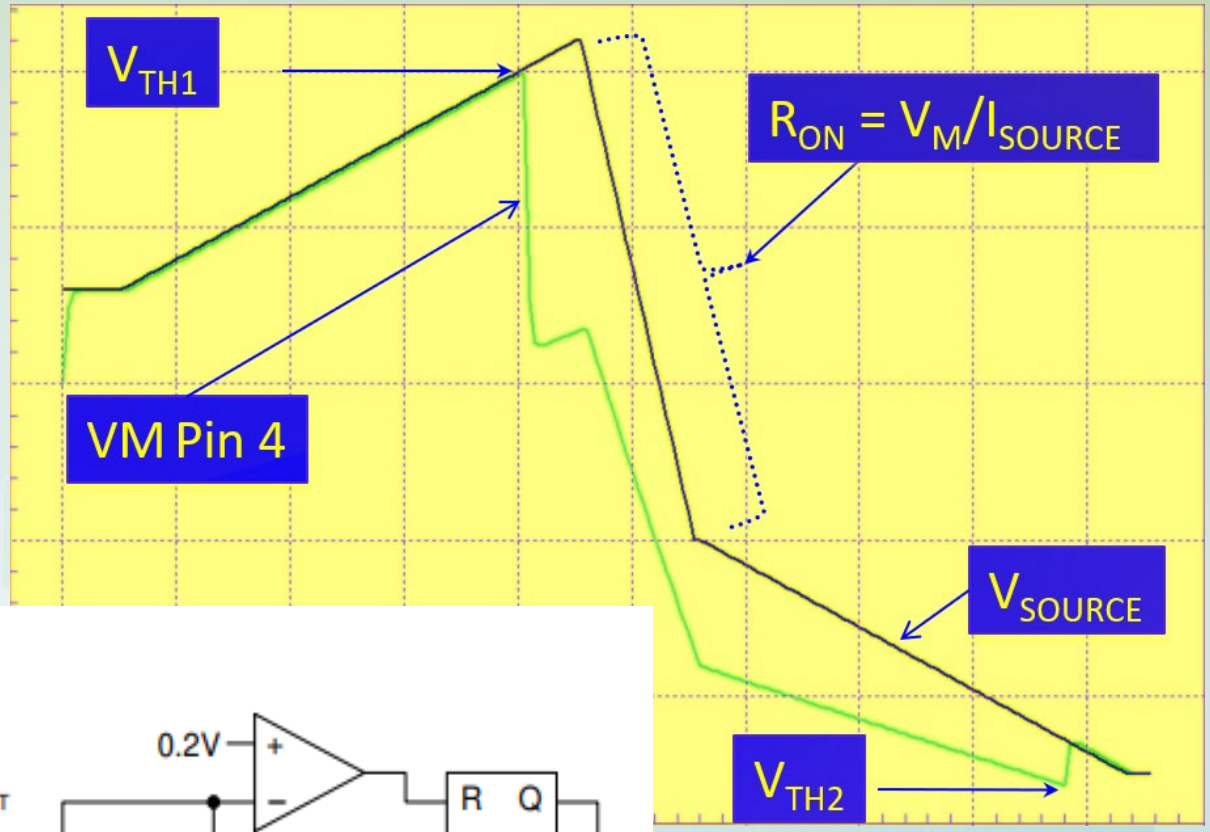
If V/I has a driver mode, implementation is straightforward as shown alongside (Solid Wire Lines)

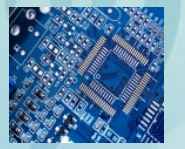
ATE's not featuring a driver mode will need to use a voltmeter or an extra VI as meter (Dashed lines added)

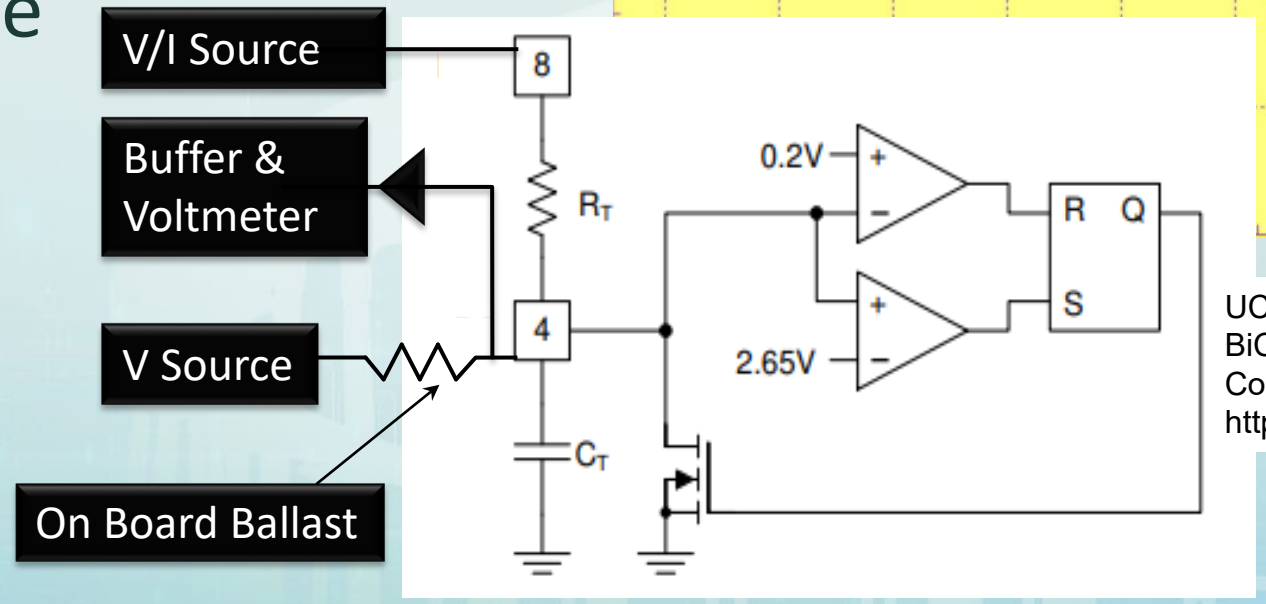
Either ways, needles are protected due to peak current reduction

and be injected in with other tests..

- Test / Measure V_{TH1}
- Test / Measure R_{ON} (FET rDS-ON)
- Test / Measure V_{TH2}
- Total Test time Reduced 90%

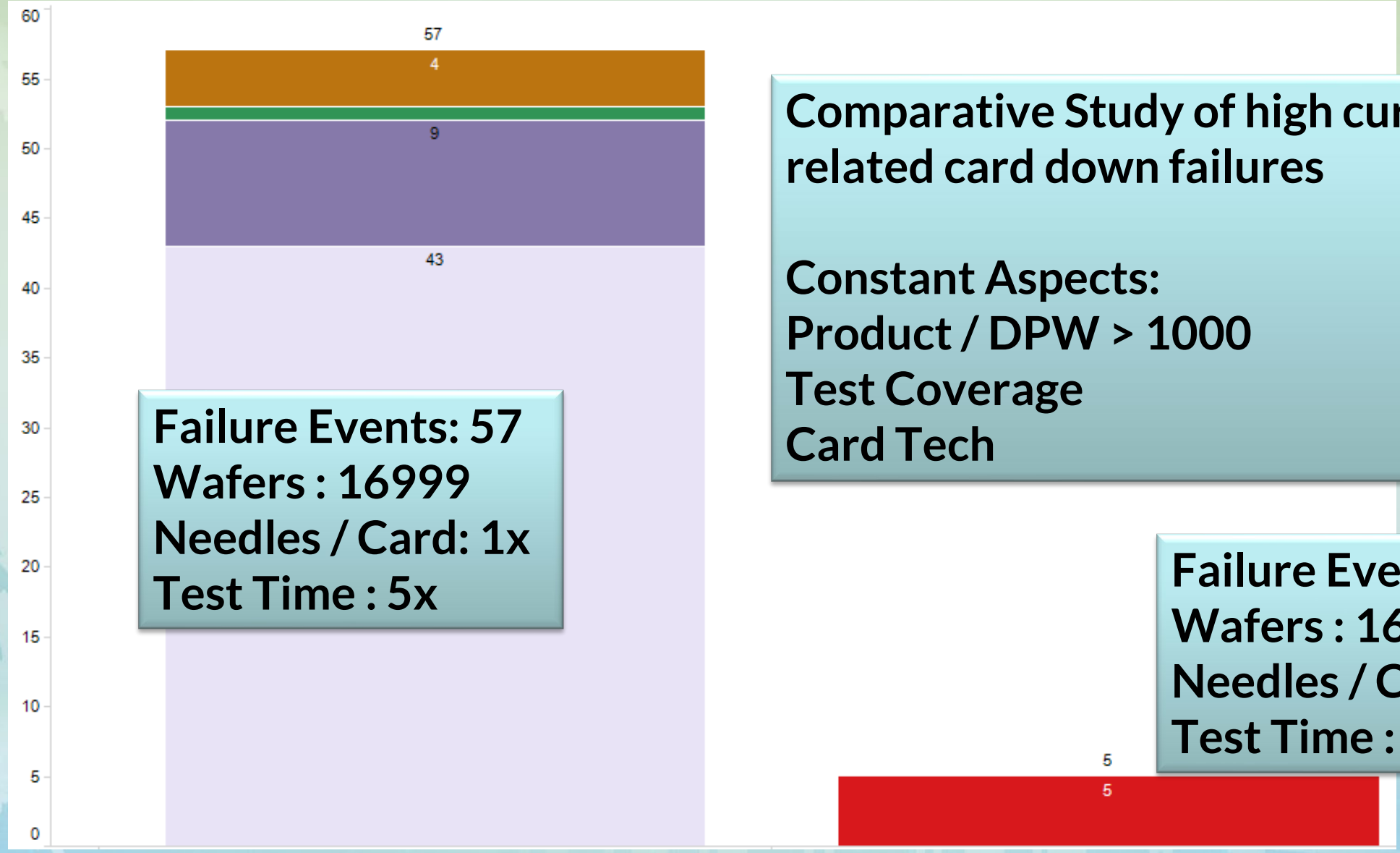






UCC280x-Q1 Low-Power BiCMOS Current-Mode PWM Controllers
https://www.ti.com

Card Failure Comparative Data



Failure Events: 57
Wafers : 16999
Needles / Card: 1x
Test Time : 5x

Comparative Study of high current related card down failures

Constant Aspects:
Product / DPW > 1000
Test Coverage
Card Tech

Failure Events: 5
Wafers : 16735
Needles / Card: 3x
Test Time : 1x

Summary & Acknowledgements

- A robust test design intended to reduce un-intentional high current events and related probe failures is presented
- Adaptation of the design to protect needles used with existing slower feedback based clamp instruments and the tradeoffs are discussed
- While alternative approaches to forward looking instrument designs are now available from TI, these are not discussed in this presentation.
- Engineers from across TI's Test & Manufacturing communities have supported the data shown in this presentation